

EE155/255 Green Electronics

Power Circuits
10/4/17

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Computer Systems Laboratory
Stanford University

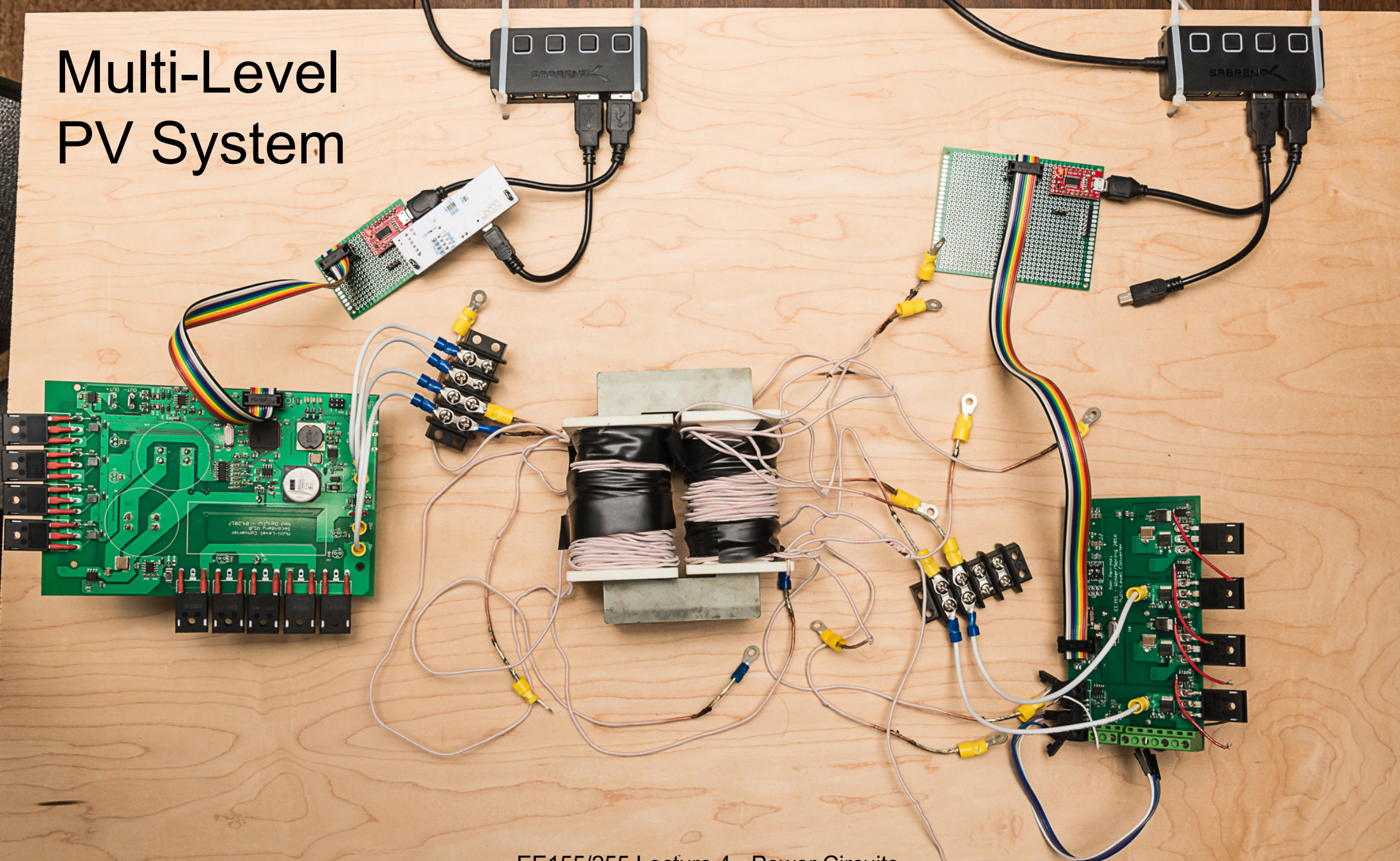
Course Logistics

- HW2 due Monday 10/9
- Lab groups have been formed
- Lab1 signed off this week
- Lab2 out

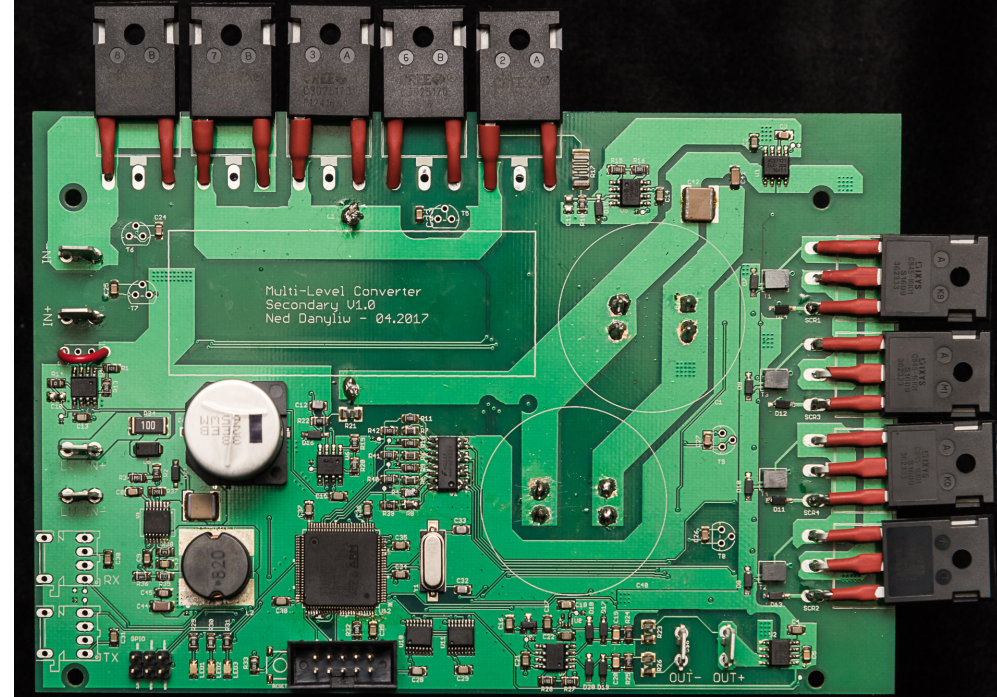
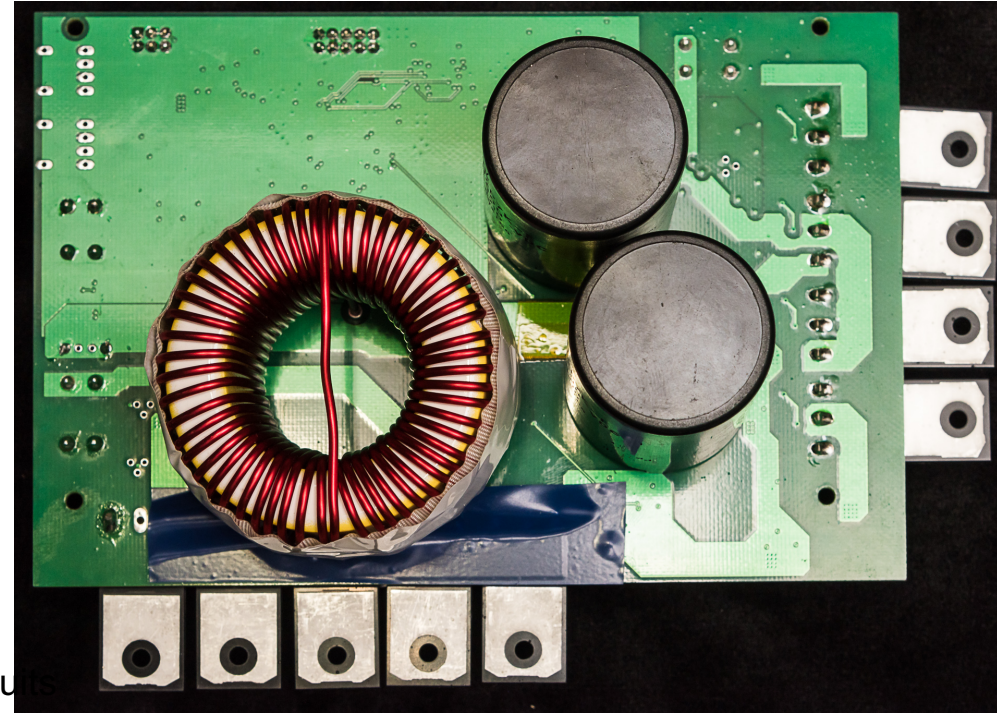
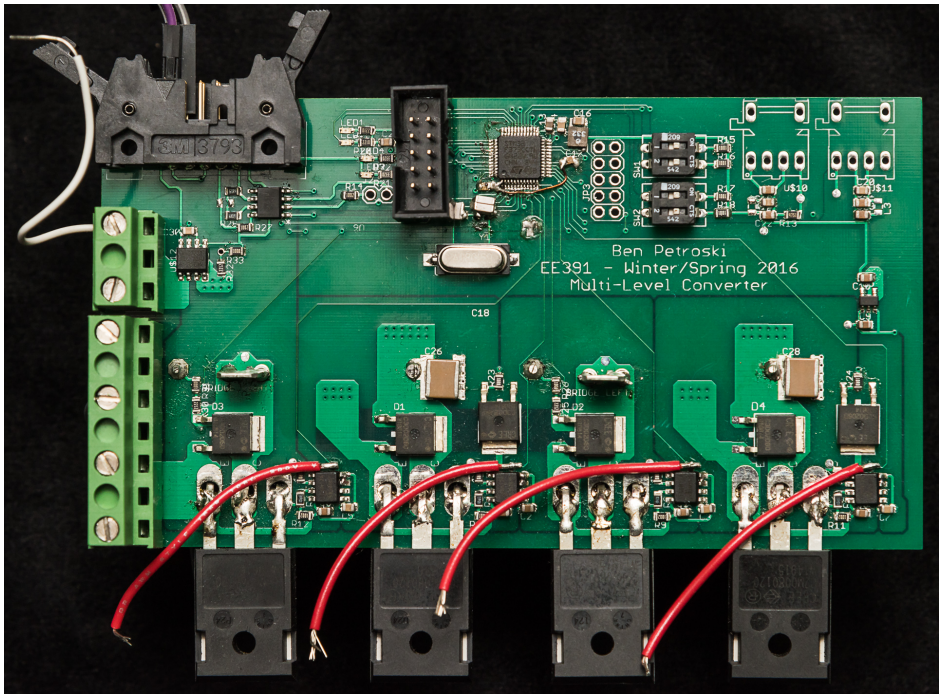
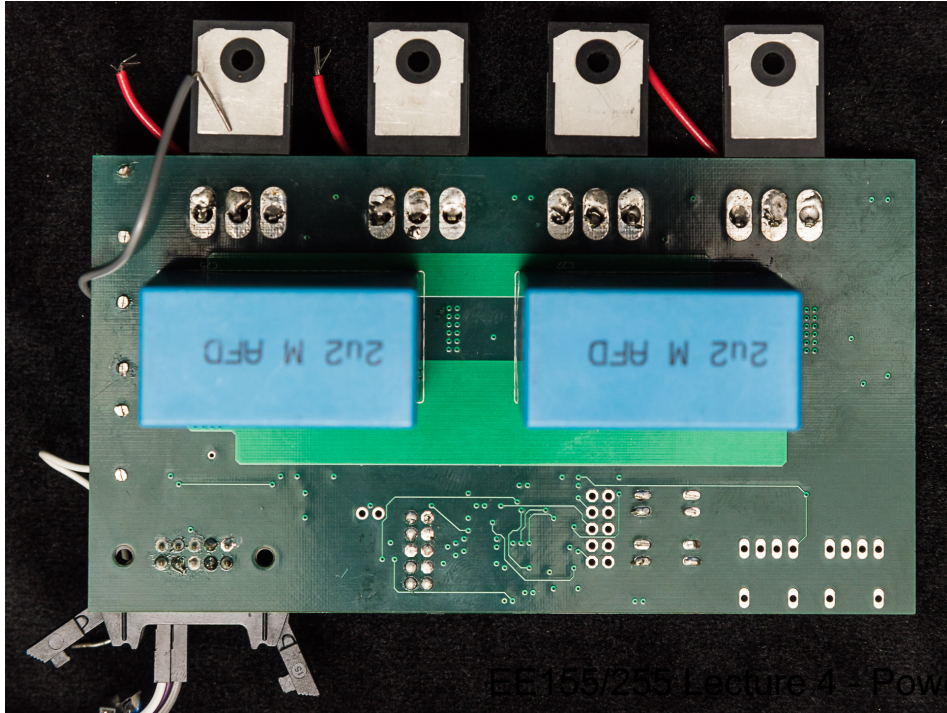
Course at a Glance

No	Date	Topic	HW out	HW in	Lab out	Lab ck	Lab	HW
1	9/25/17	Intro (basic converters)	1		1		Intro to ST32F3	Periodic Steady State
2	9/27/17	Embedded Prog/Power Elect.						
3	10/2/17	Power Electronics - 1 (switches)	2	1	2	1	AC Energy Meter	Power Devices
4	10/4/17	Power Electronics - 2 (circuits)						
5	10/9/17	Photovoltaics	3	2	3	2	PV MPPT	Motor control Matlab
6	10/11/17	Feedback Control						
7	10/16/17	Electric Motors	4	3	4	3	Motor control - Lab/	Feedback
8	10/18/17	Isolated Converters						
9	10/23/17	Solar Day	5/PP	4	5	4	PS	Isolated Converters
10	10/25/17	Magnetics						
11	10/30/17	Soft Switching	6	5/PP	6	5	Magnetics	Magnetics and Inverters
12	11/1/17	Project Discussions						
13	11/6/17	Inverters, Grid, PF, and Batteries		6	P	6	Project	
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	12/15/17	Project webpage due						

Multi-Level PV System



Primary and Secondary PCBs



Course to Date

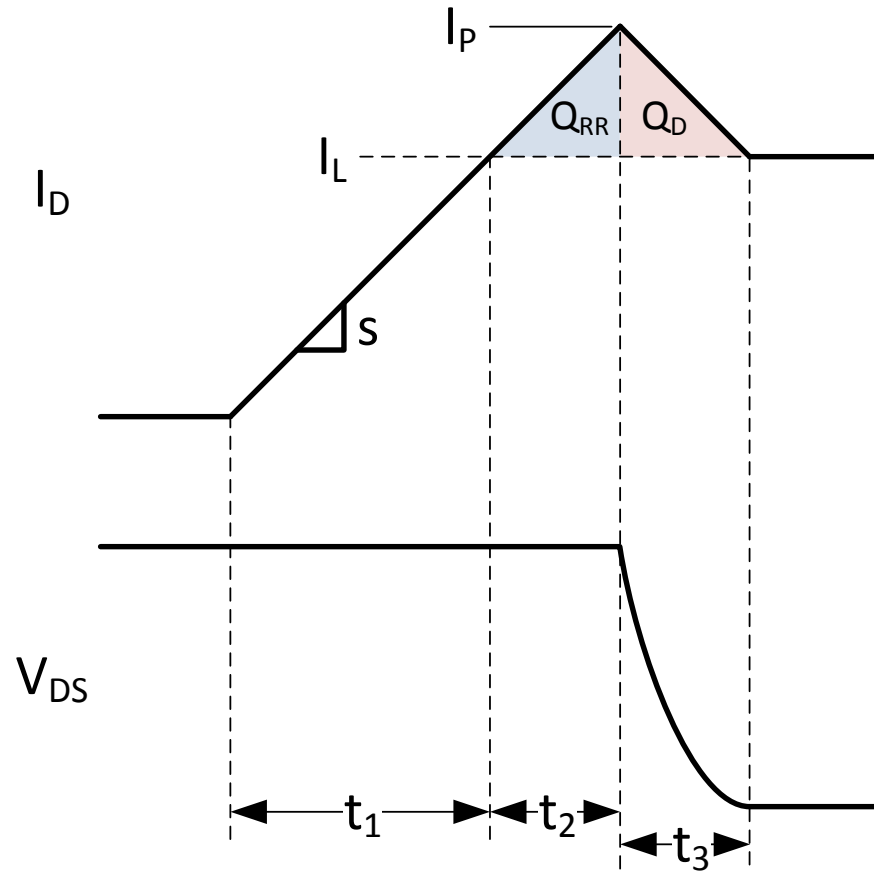
- We need sustainable energy systems
- At the core they are voltage converters
- Periodic steady-state analysis, buck and boost
- Intelligent control + power path
- Intelligent control done with event-driven embedded software
- Real devices have switching and conduction loss – and parasitics

Last Time

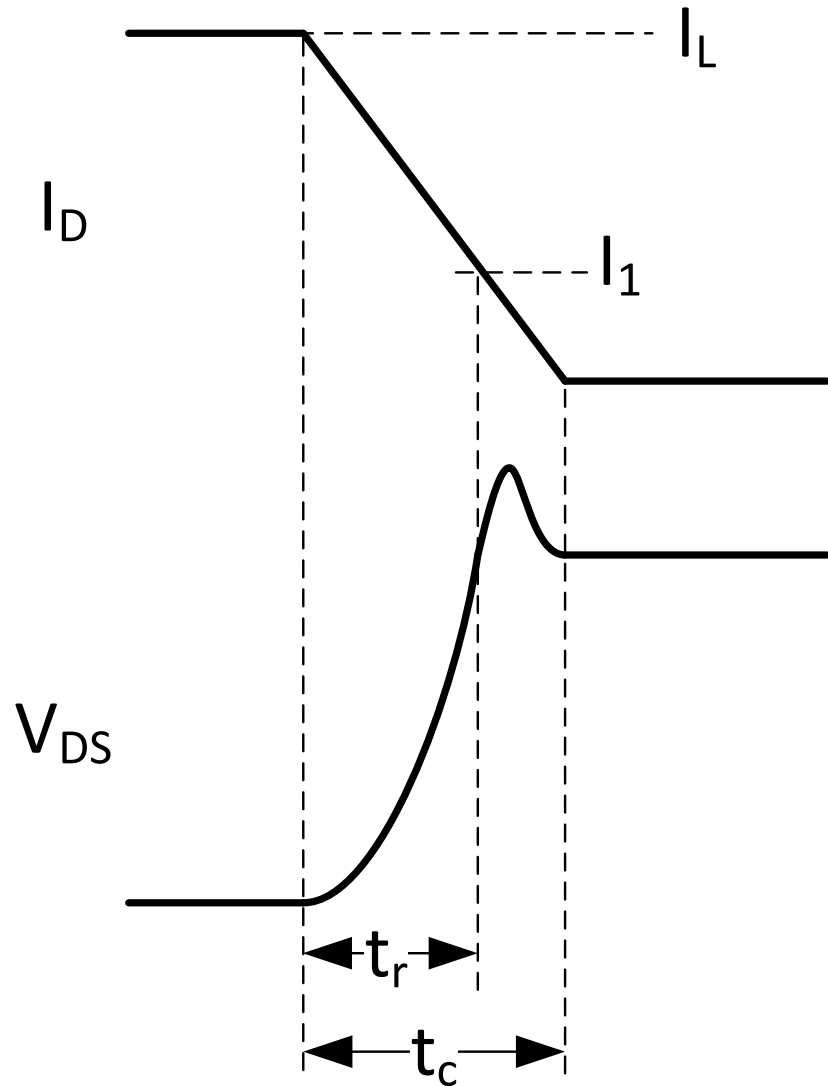
- DC and AC characteristics of MOSFETs, Diodes, and IGBTs
- Switches in pairs
- One switch does the work
- Turn on transient
- Diode reverse recovery
- Parasitics
- Gate drive and Miller capacitance

Turn-On and Turn-Off Loss

Turn-On Loss



Turn-Off Buck with Diode

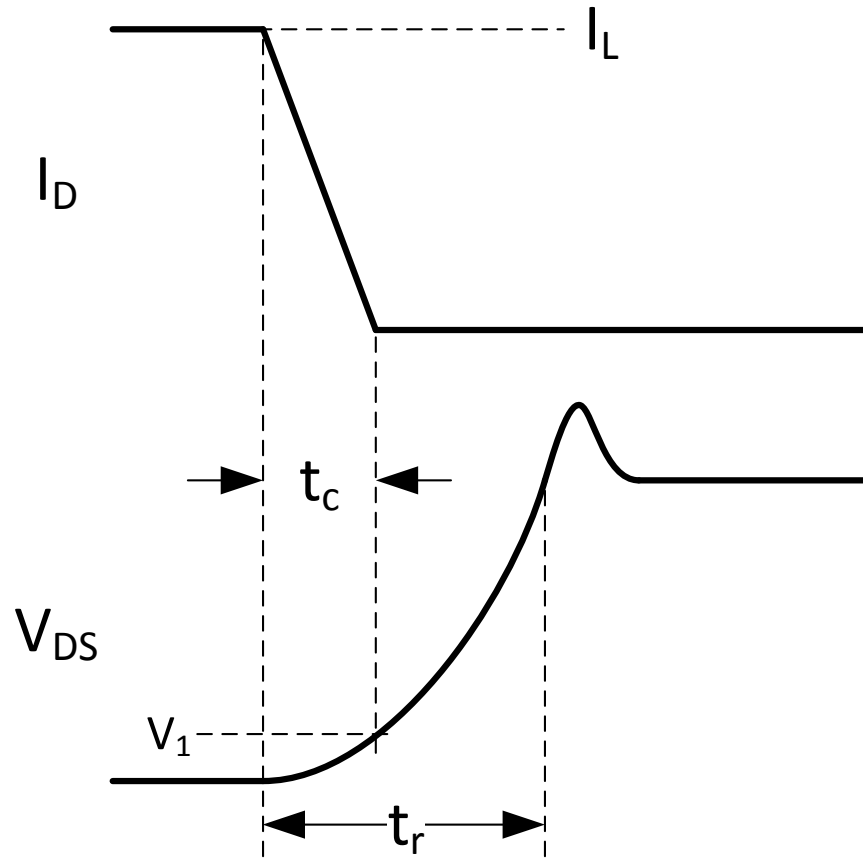


Excess current charges drain node.

Integrate to get switching energy

$$E = V_{DD} t_r \left(\frac{1}{6} I_L + \frac{1}{3} I_1 \right)$$

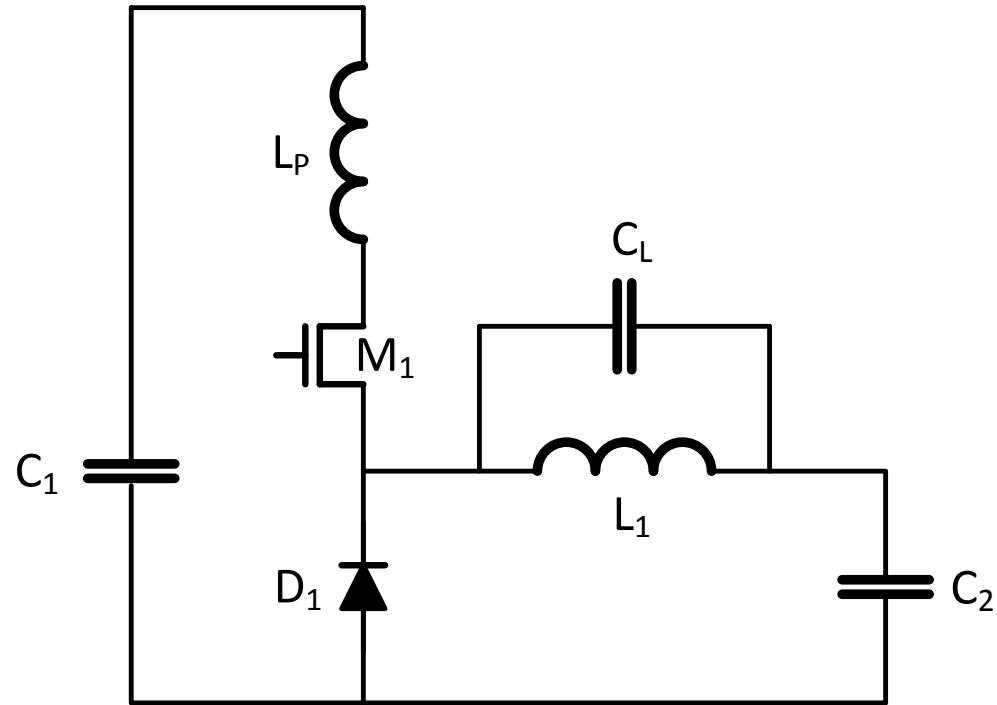
Turn-Off Buck with Diode



If current ramps faster than
voltage nearly ZVS

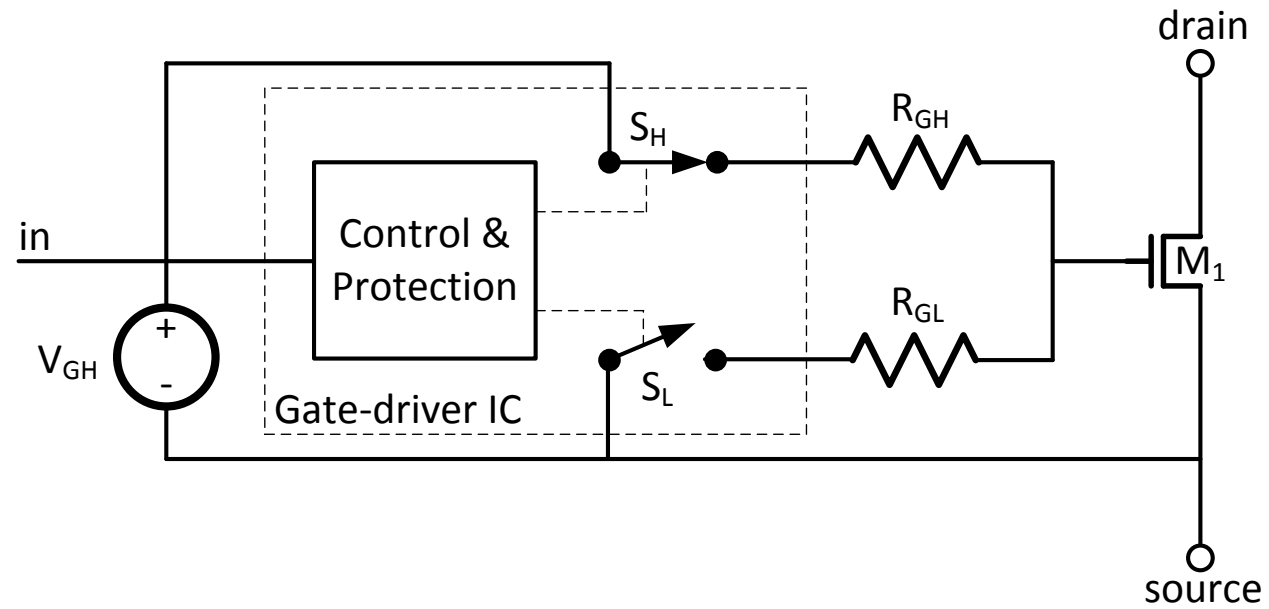
$$E = \frac{1}{6} V_1 I_L t_c$$

Parasitic Losses

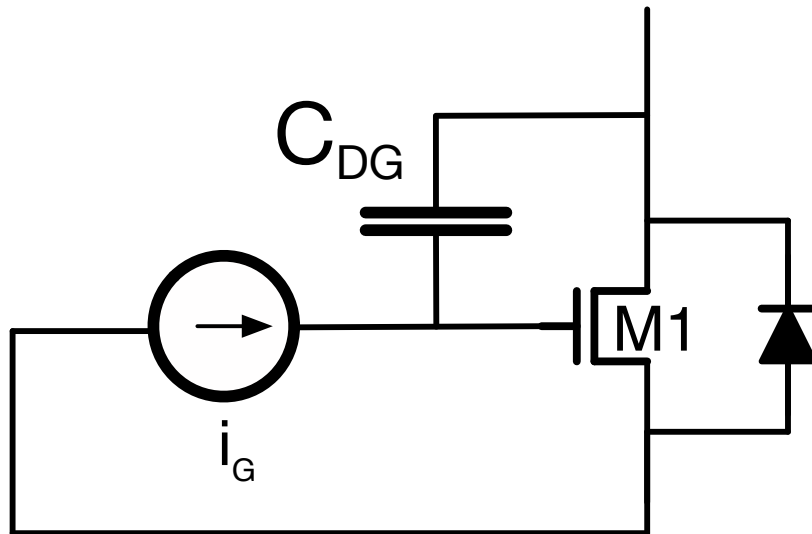


Gate Drive

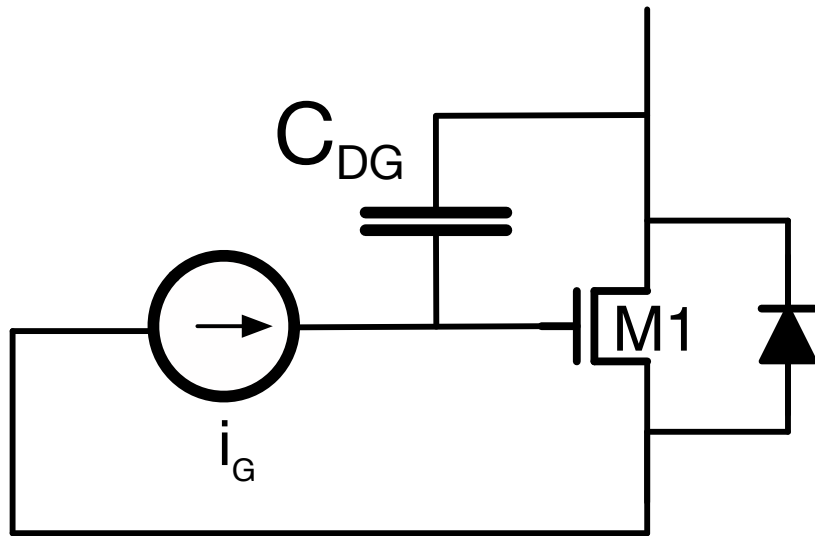
Gate Driver



Effect of Miller Cap on Rise Time



Effect of Miller Cap on Rise Time

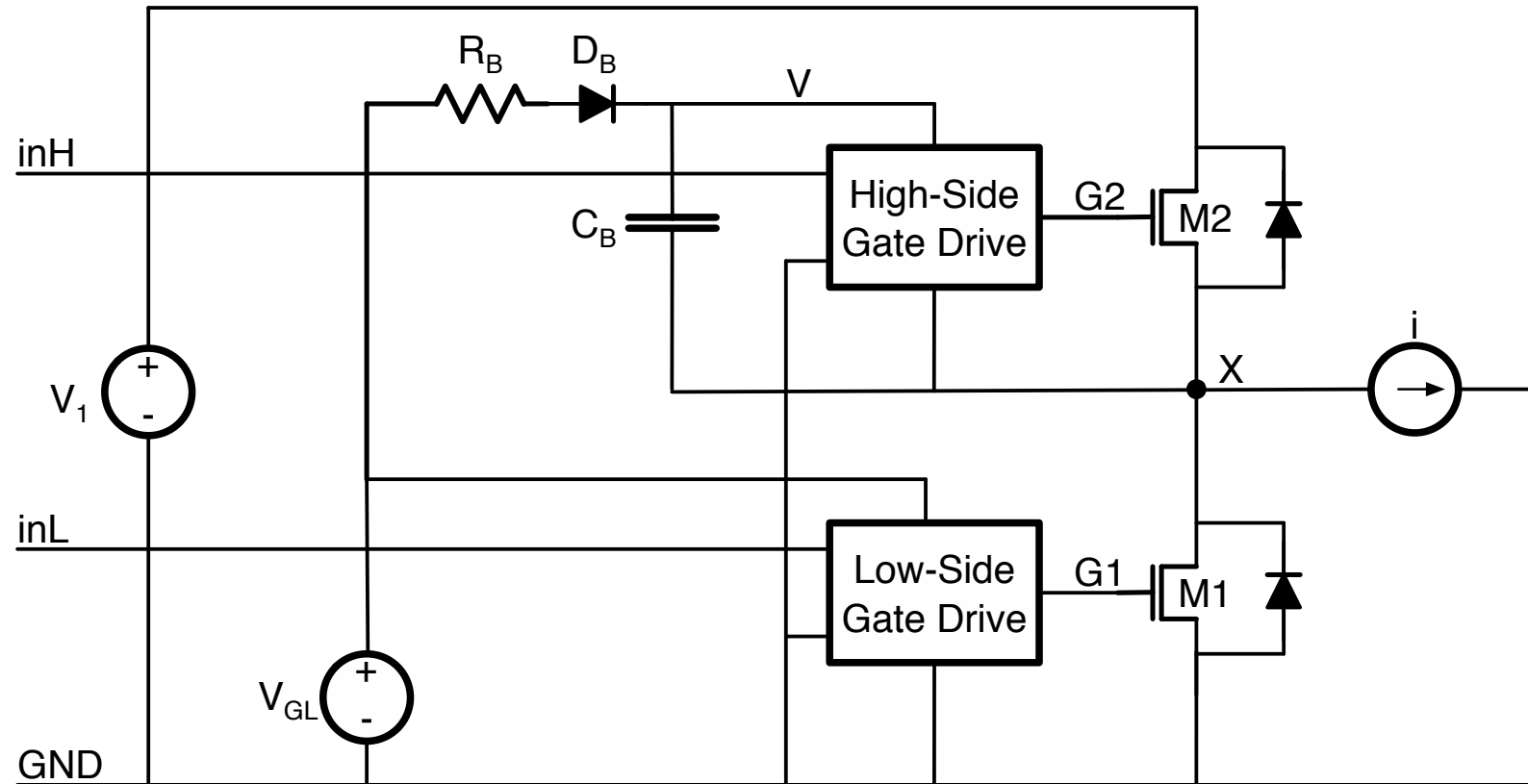


$$\frac{dV_D}{dt} = \frac{i_G}{C_{DG}}$$

$$\Delta t = \frac{\Delta V_D C_{DG}}{i_G}$$

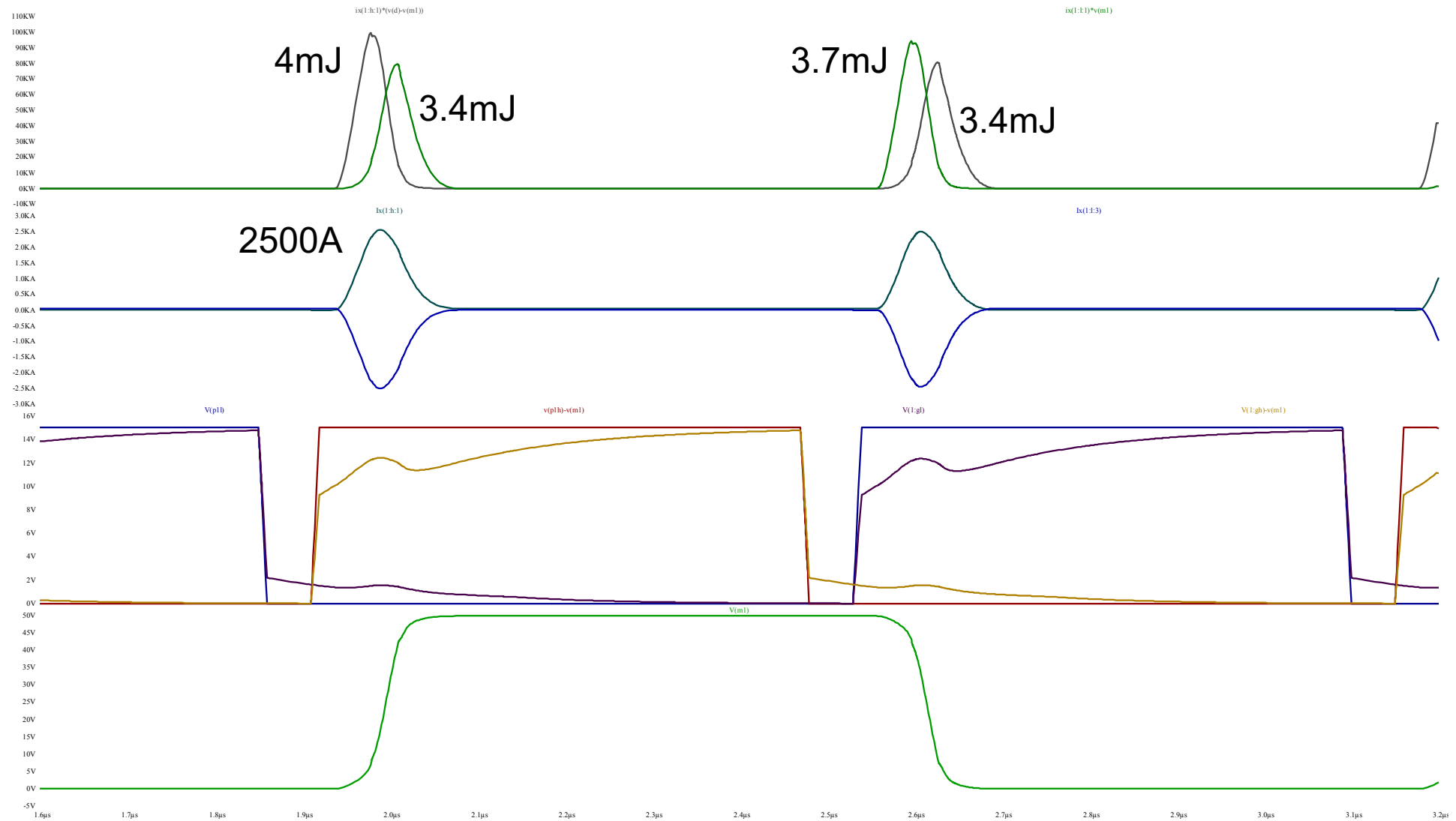
Example: $i = 0.5\text{A}$, $C = 100\text{pF}$, $\Delta V = 400\text{V}$

Bootstrap Supply

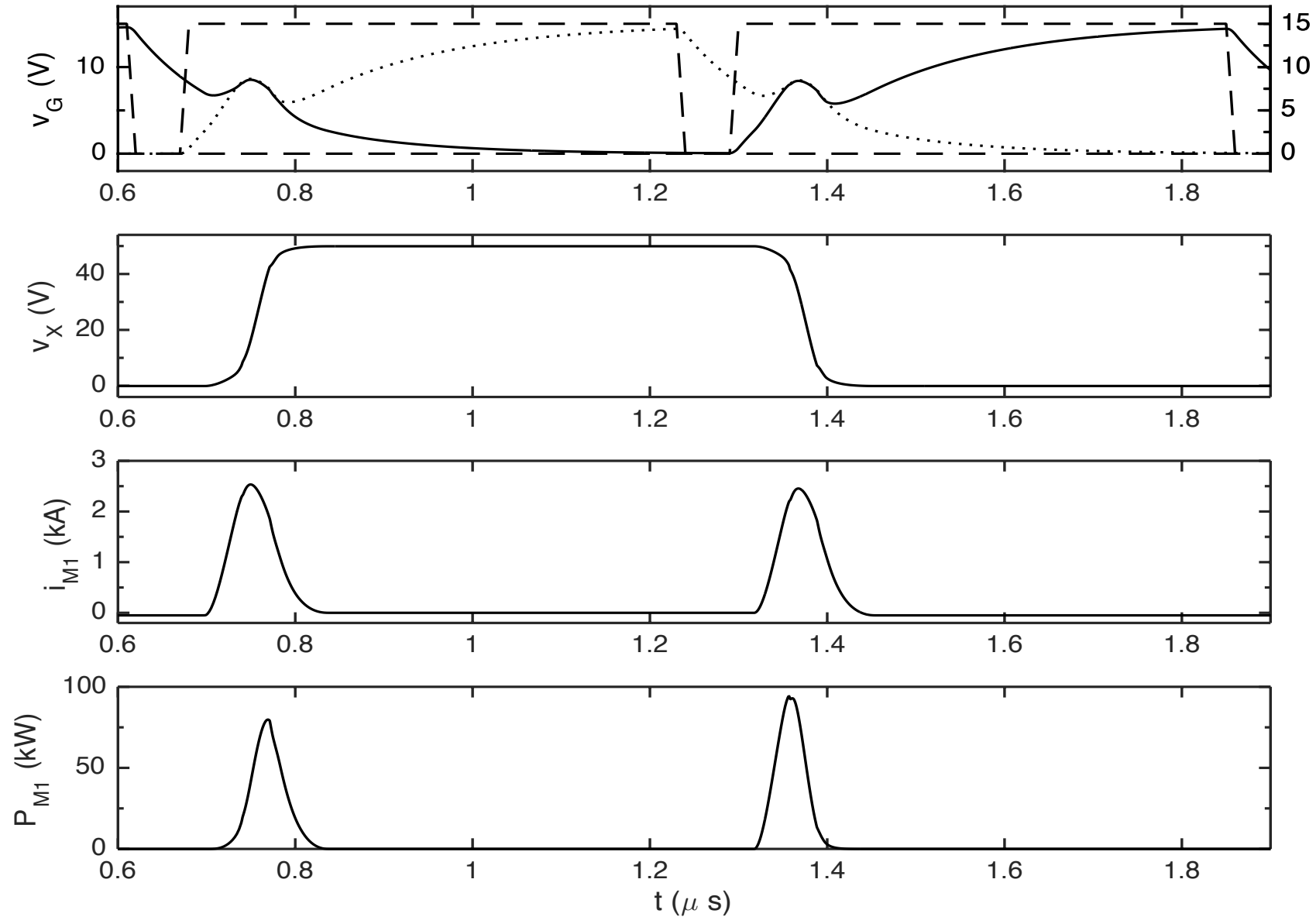


Dead Time

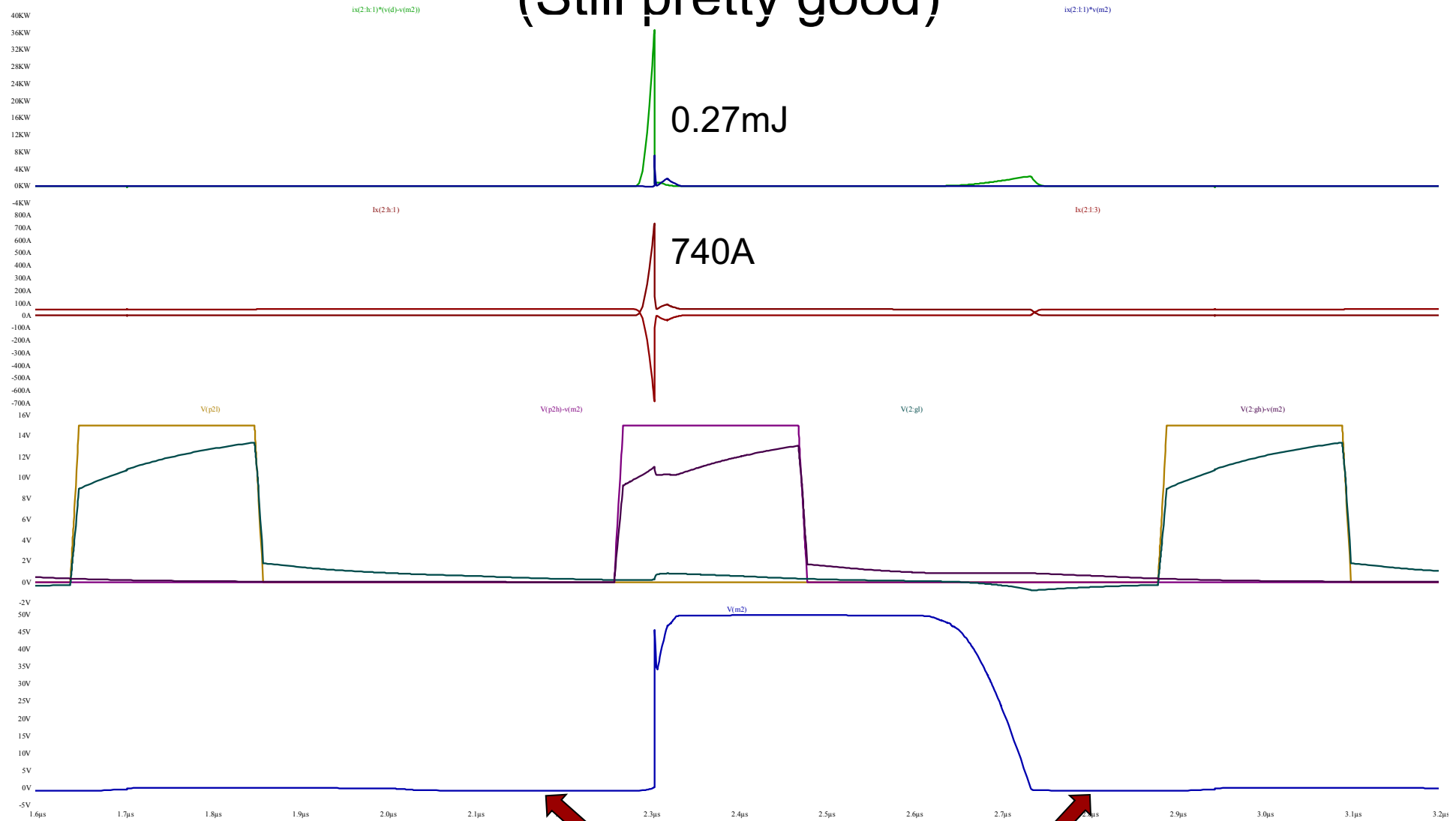
Too Little Dead Time (11.6kW loss)



The "Real" Gate Signal

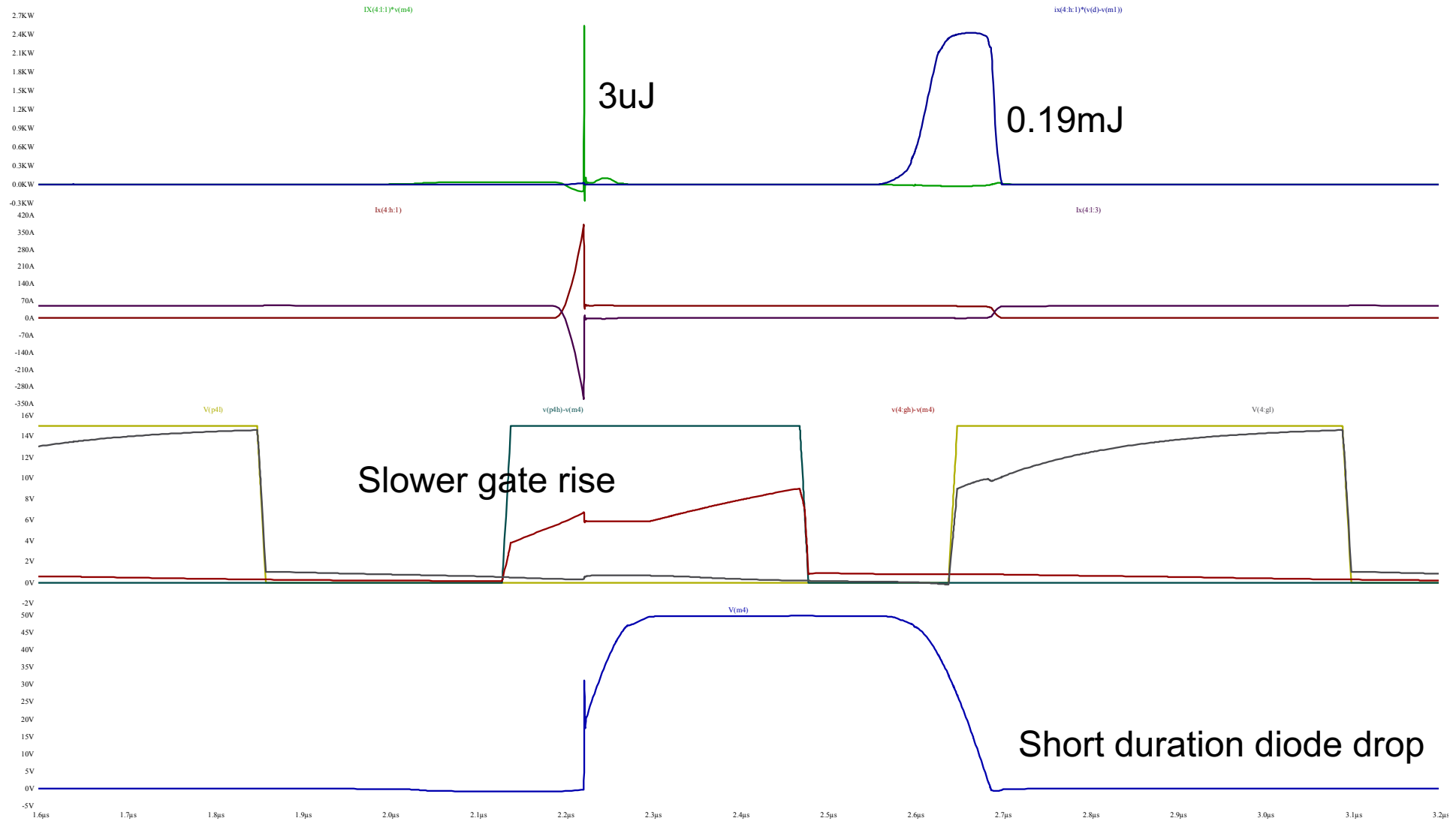


Too Much Dead-Time (340W loss) (Still pretty good)



700mV diode drop
EE155/255 Lecture 4 - Power Circuits

Just Right (310W loss)

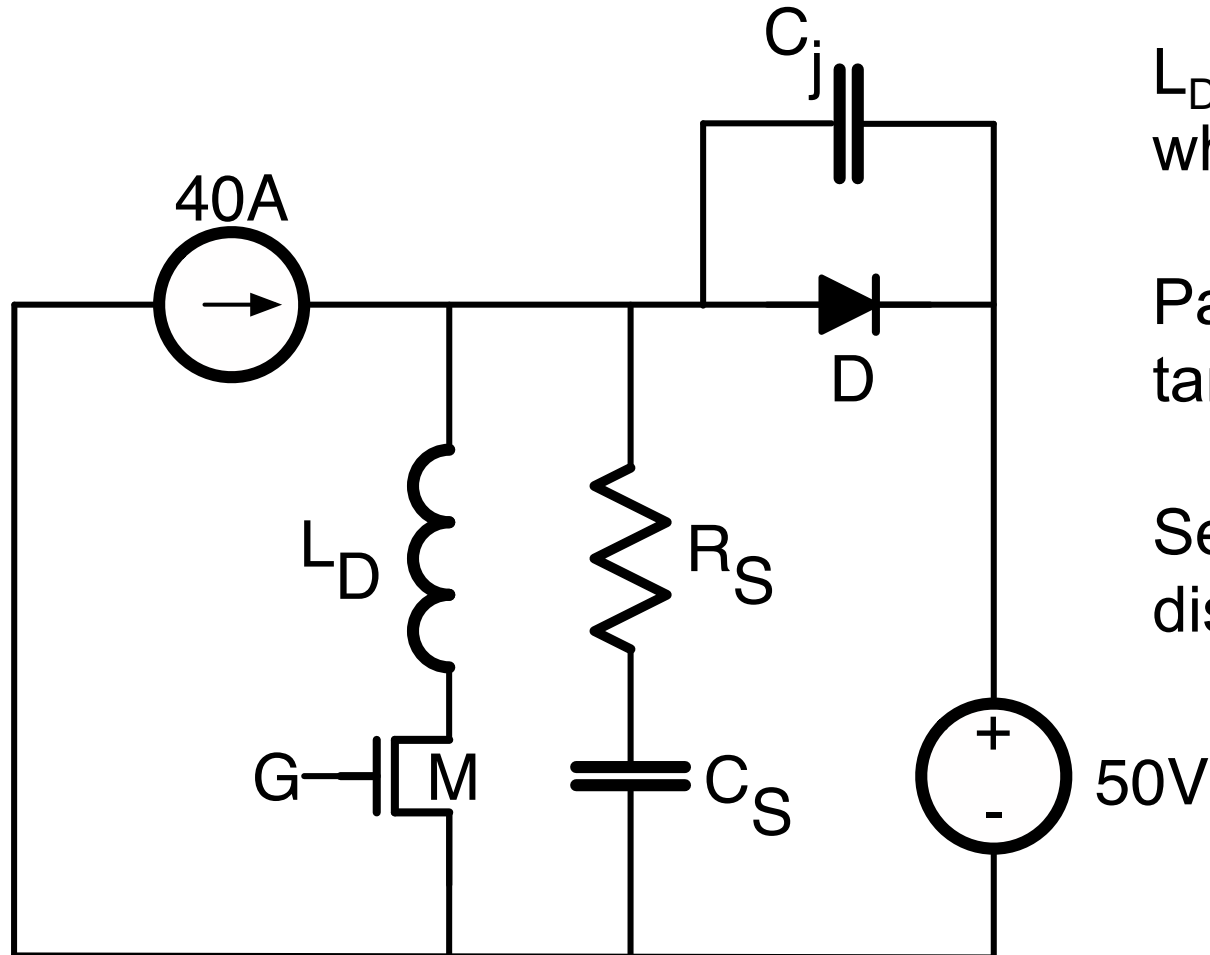


Conduction loss is $I^2R = 50^2 \times 1m \sim 25W$

Too much dead time is better than too little

Snubbers

Dampen Ringing Nodes

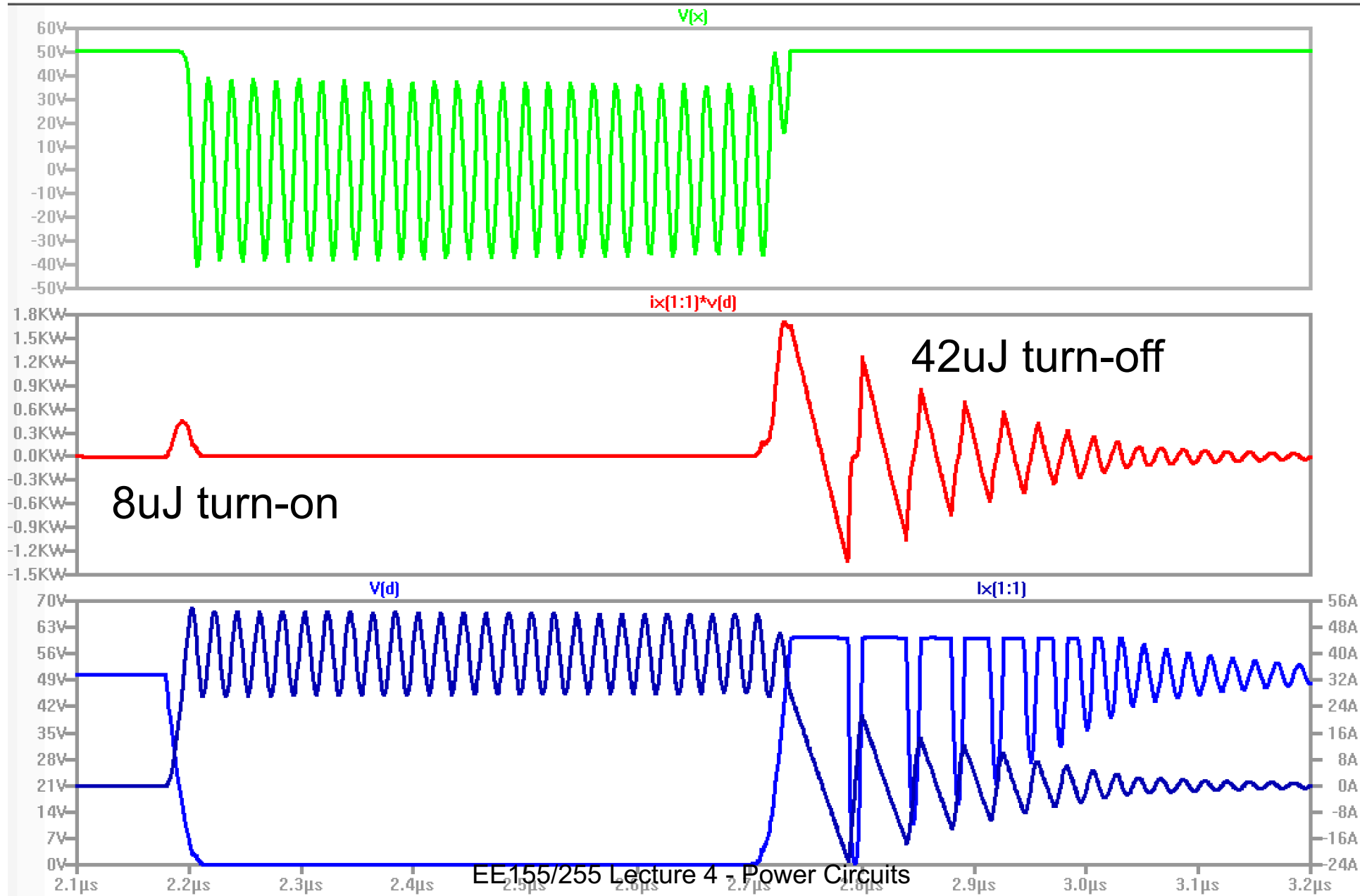


L_D and C_j resonate
when M is on

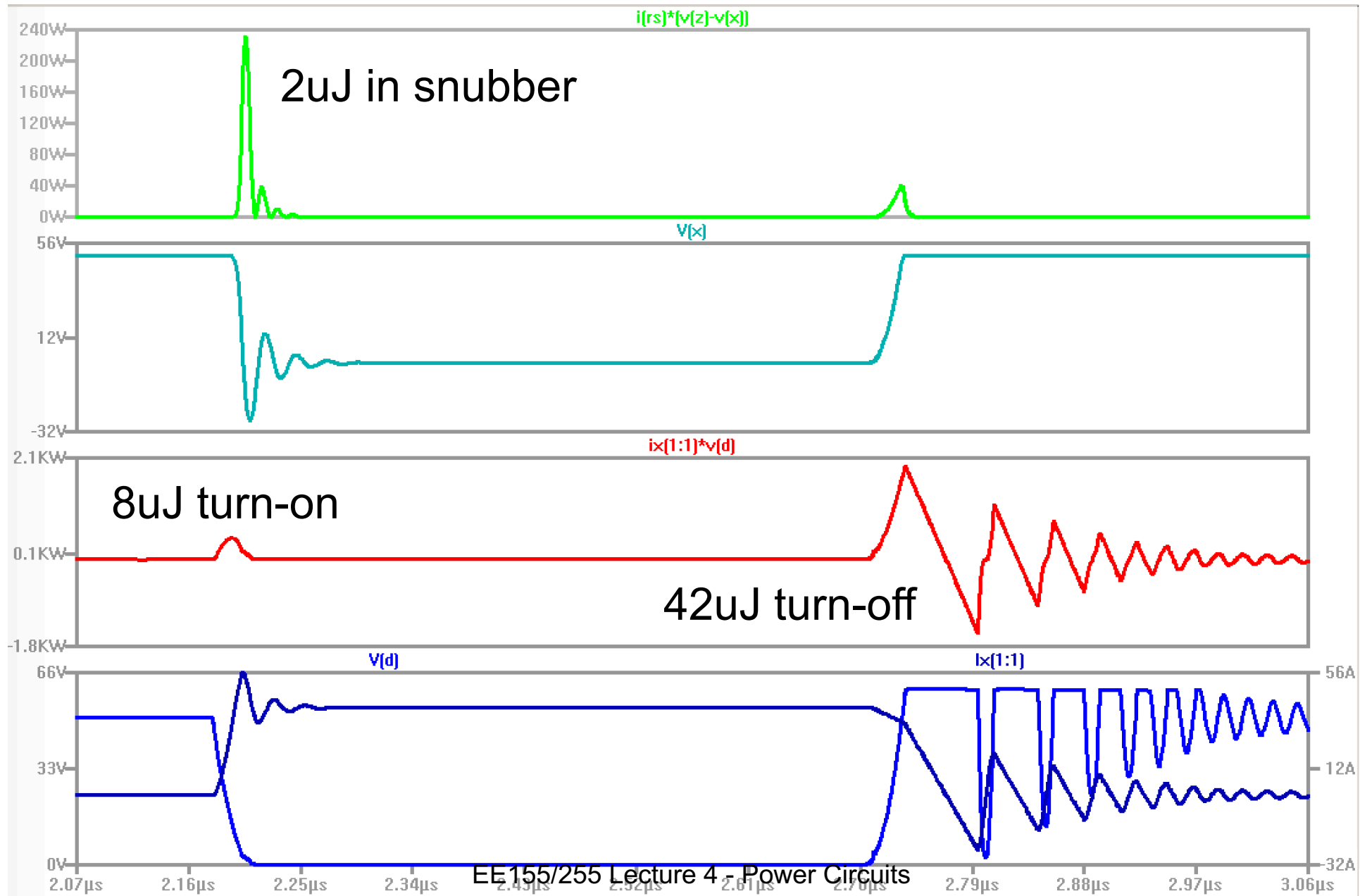
Parallel R_S dampens
tank

Series C_S limits
dissipation

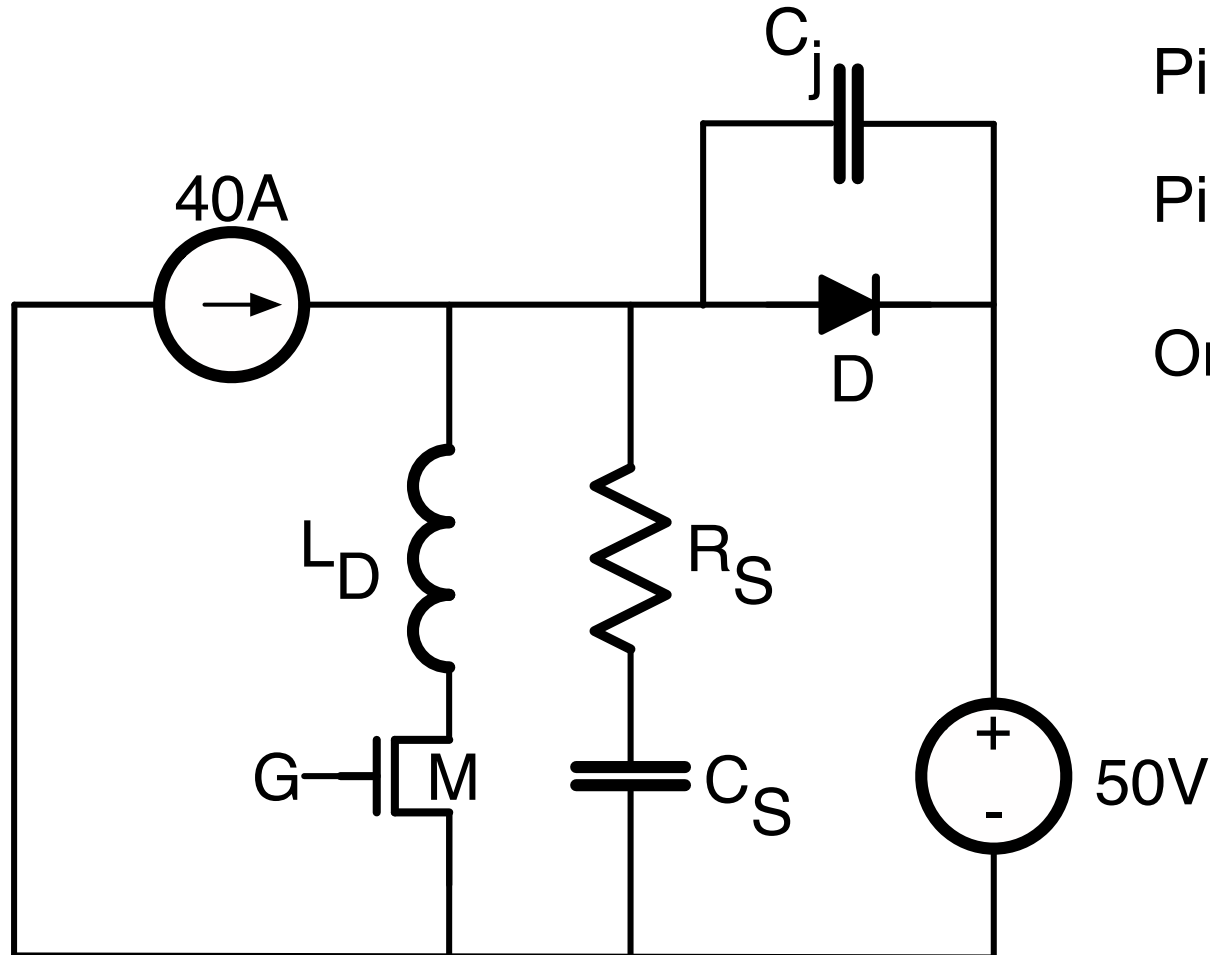
Inductance on Drain



With Snubber (1nF, 5Ω)



Design Procedure



Pick $R_S \sim 1/\omega C_j$

Pick C_S so

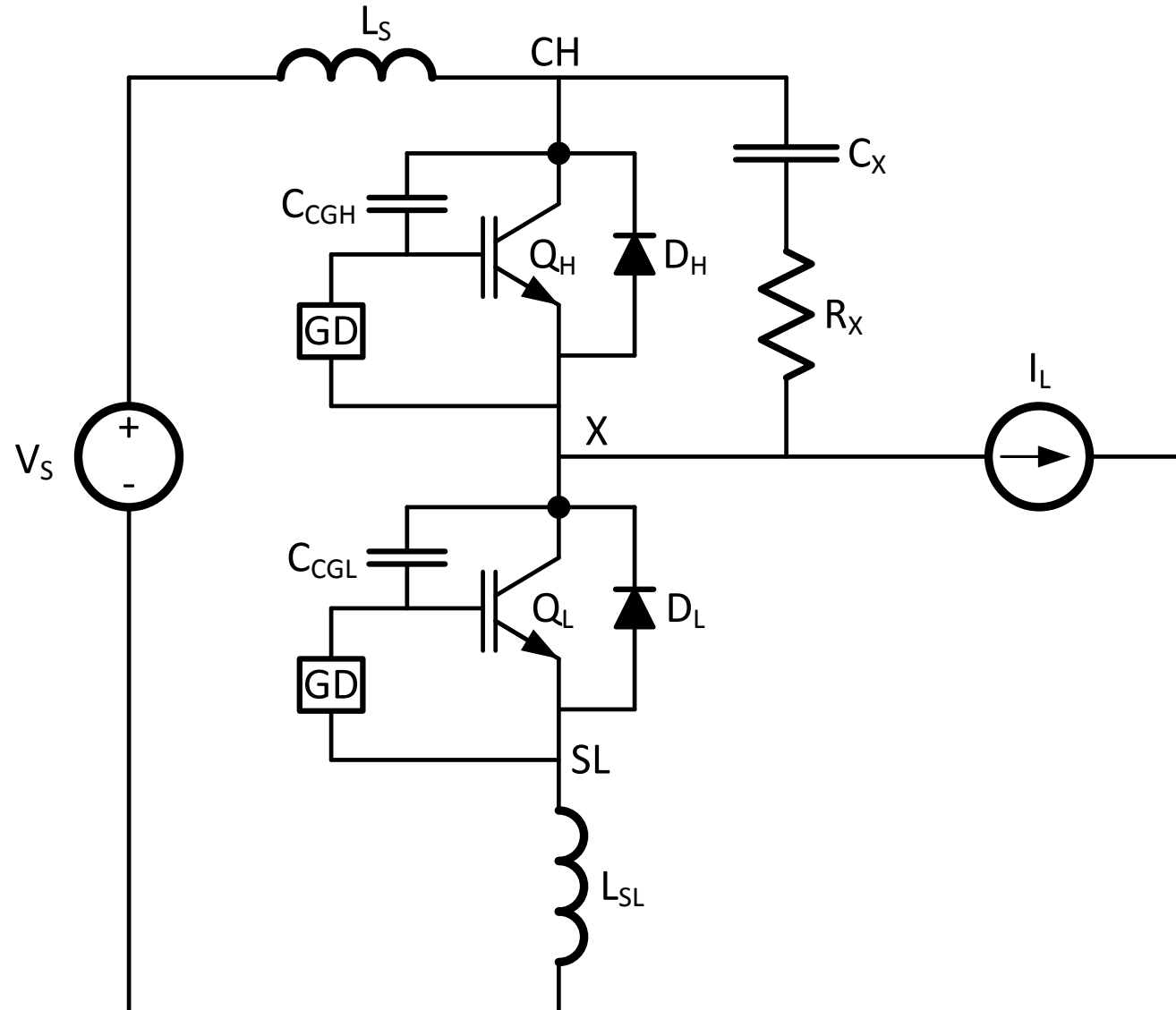
$$\tau \geq \pi/\omega$$

Or

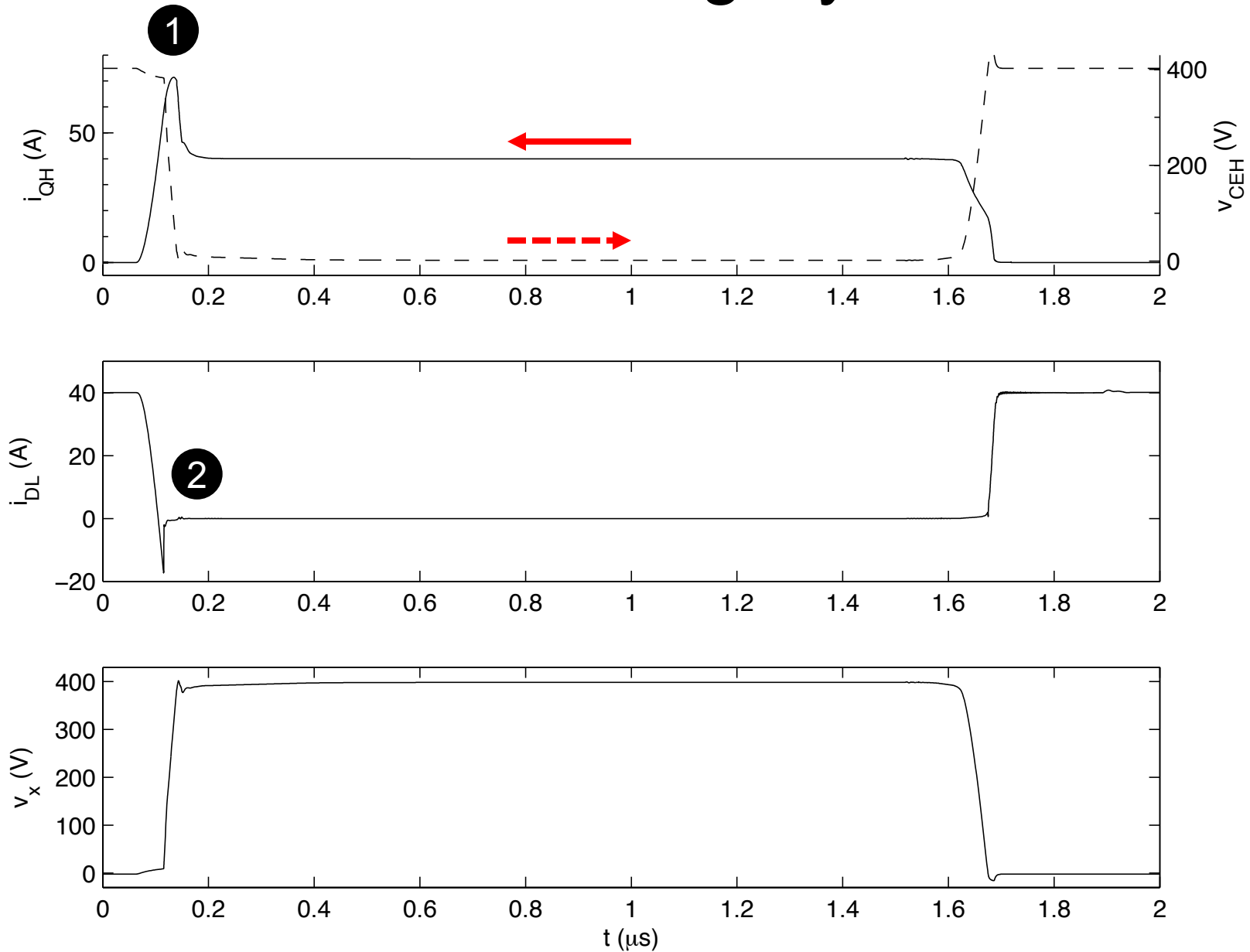
$$E_s = C_S V^2/2$$

Example Cycle

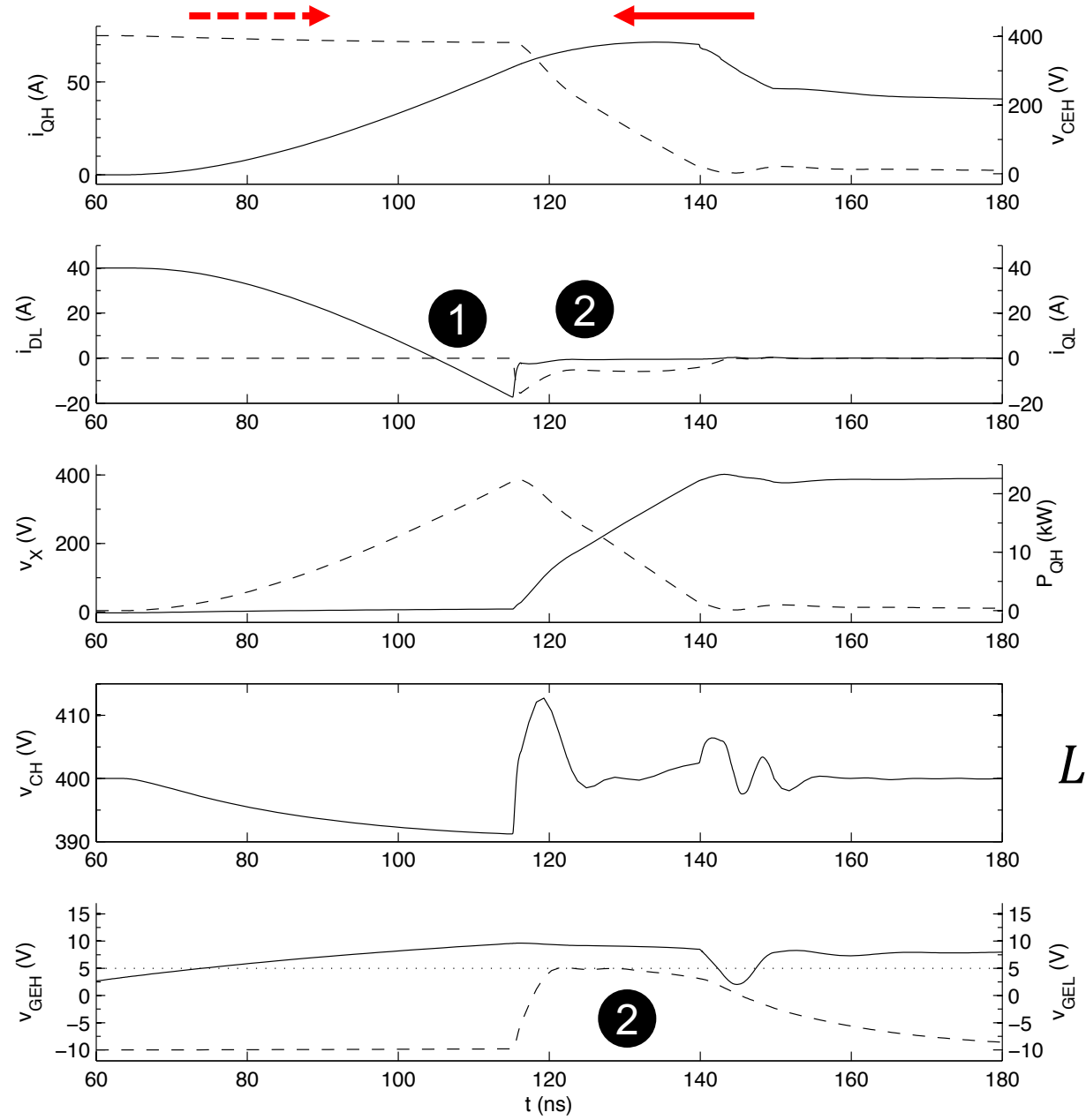
IGBT Half Bridge



One Switching Cycle



High-Side Turn On

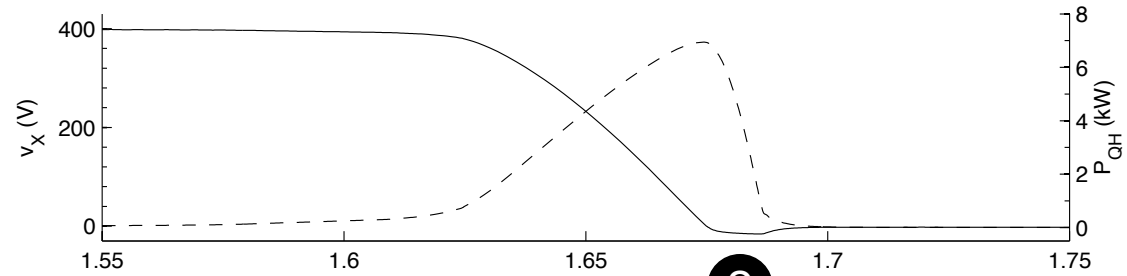
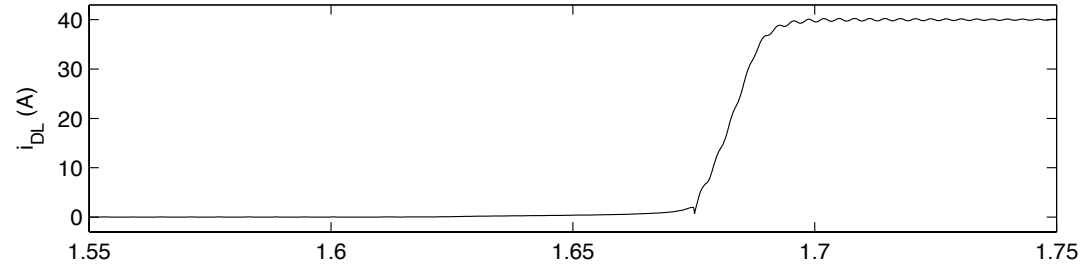
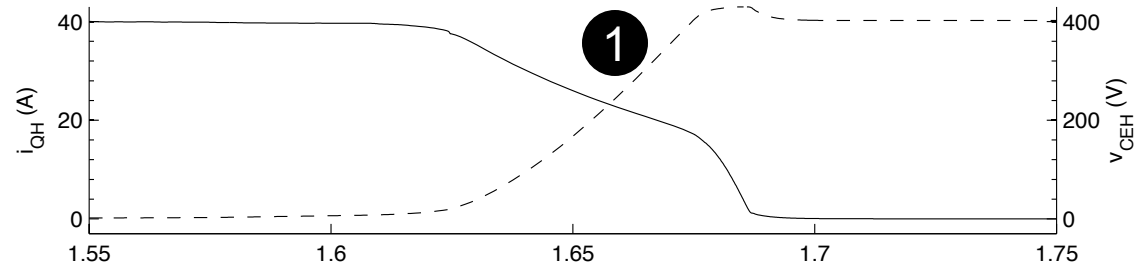


$$E \sim \frac{60ns \times 22kW}{2} = 660\mu J$$

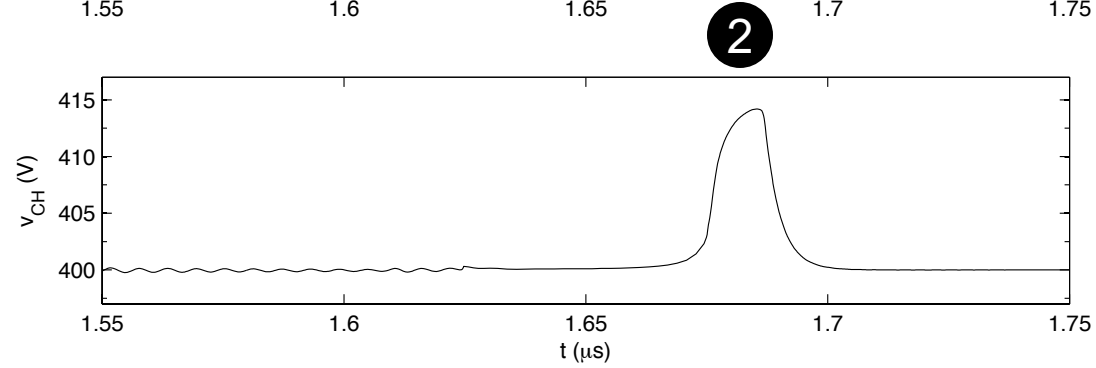
$$E = 773\mu J$$

$$L \frac{di}{dt}$$

High-Side Turn Off



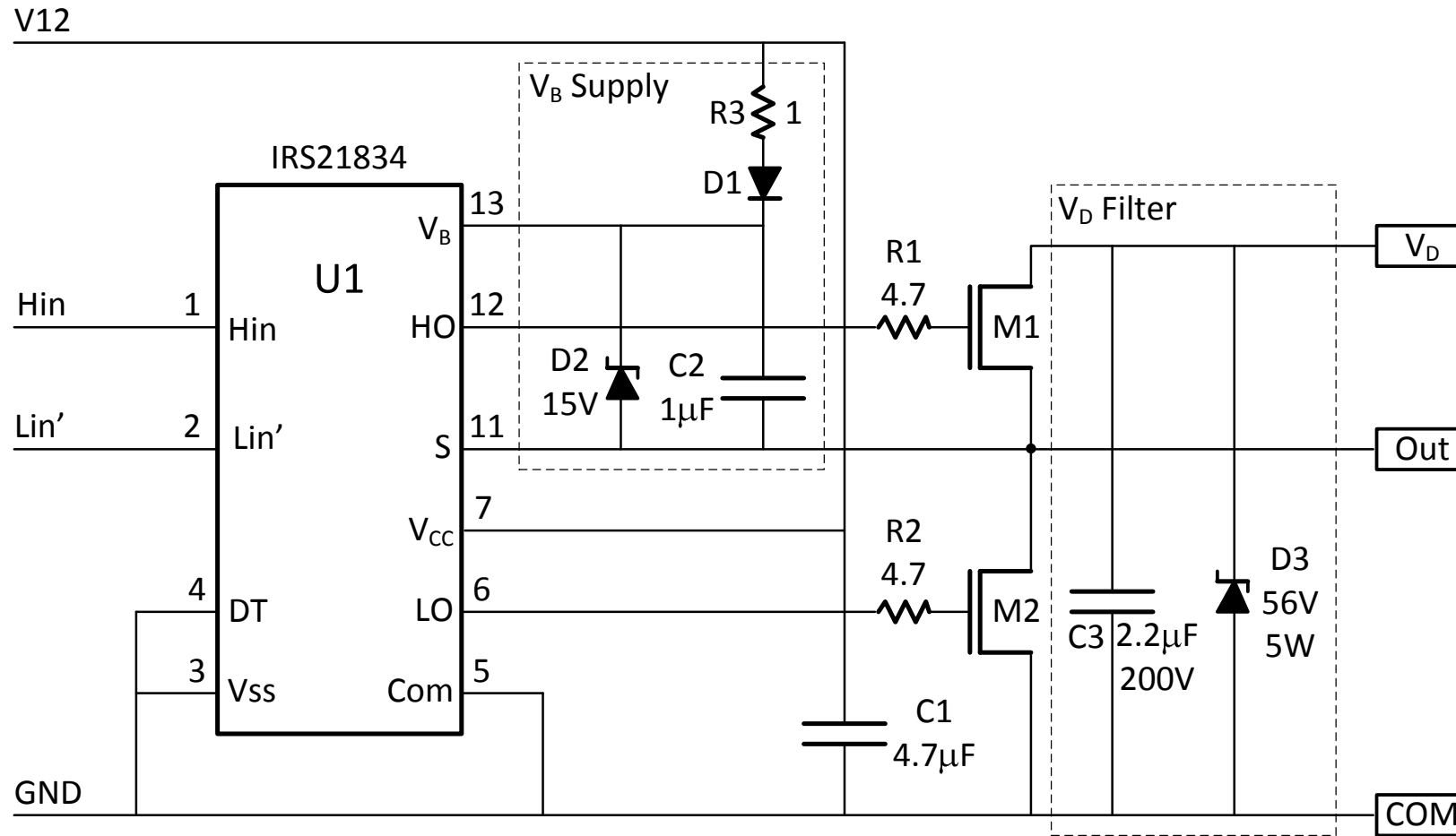
$$E = 230 \mu J$$



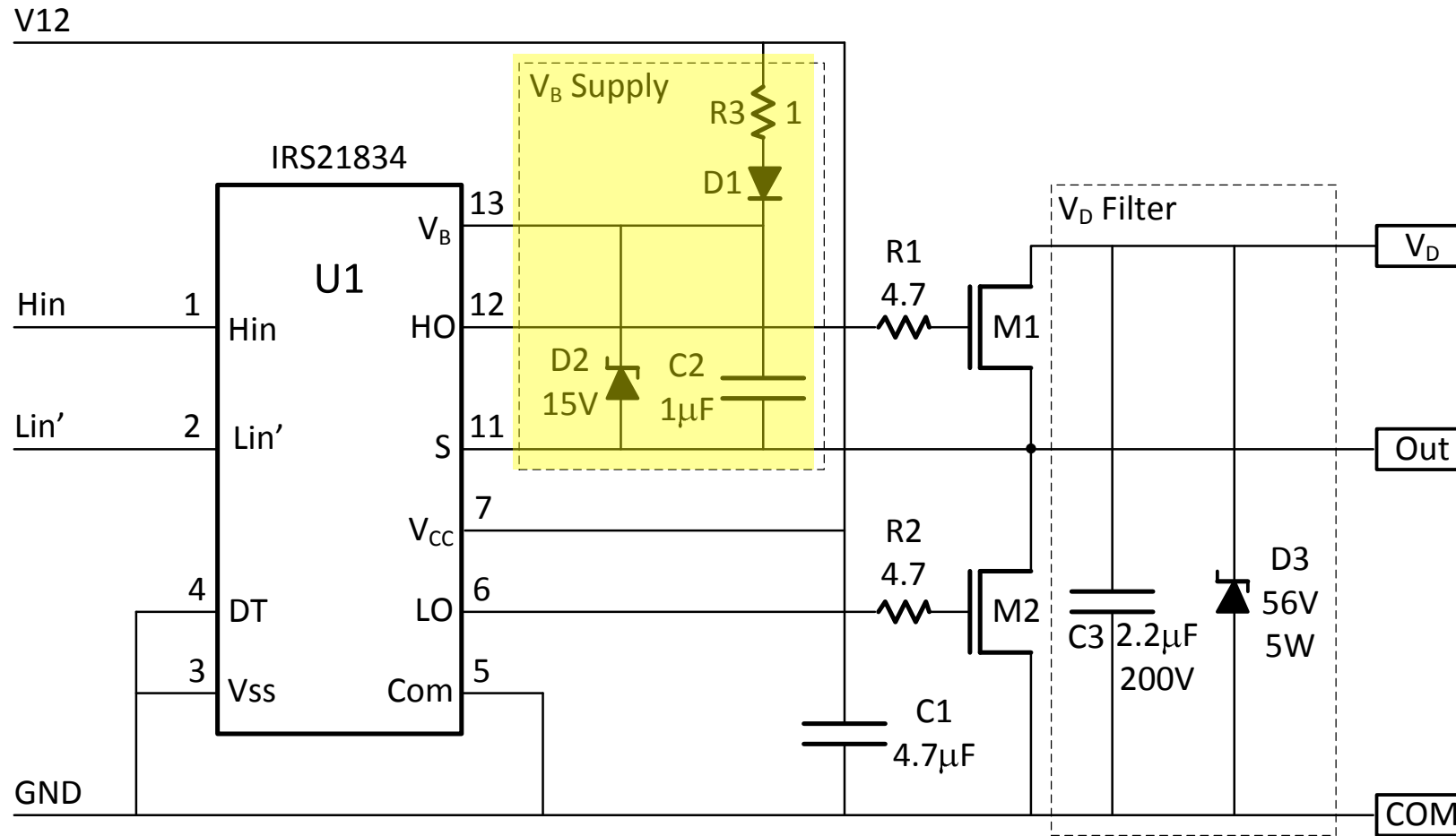
$$L \frac{di}{dt}$$

Lab Half-Bridge Module

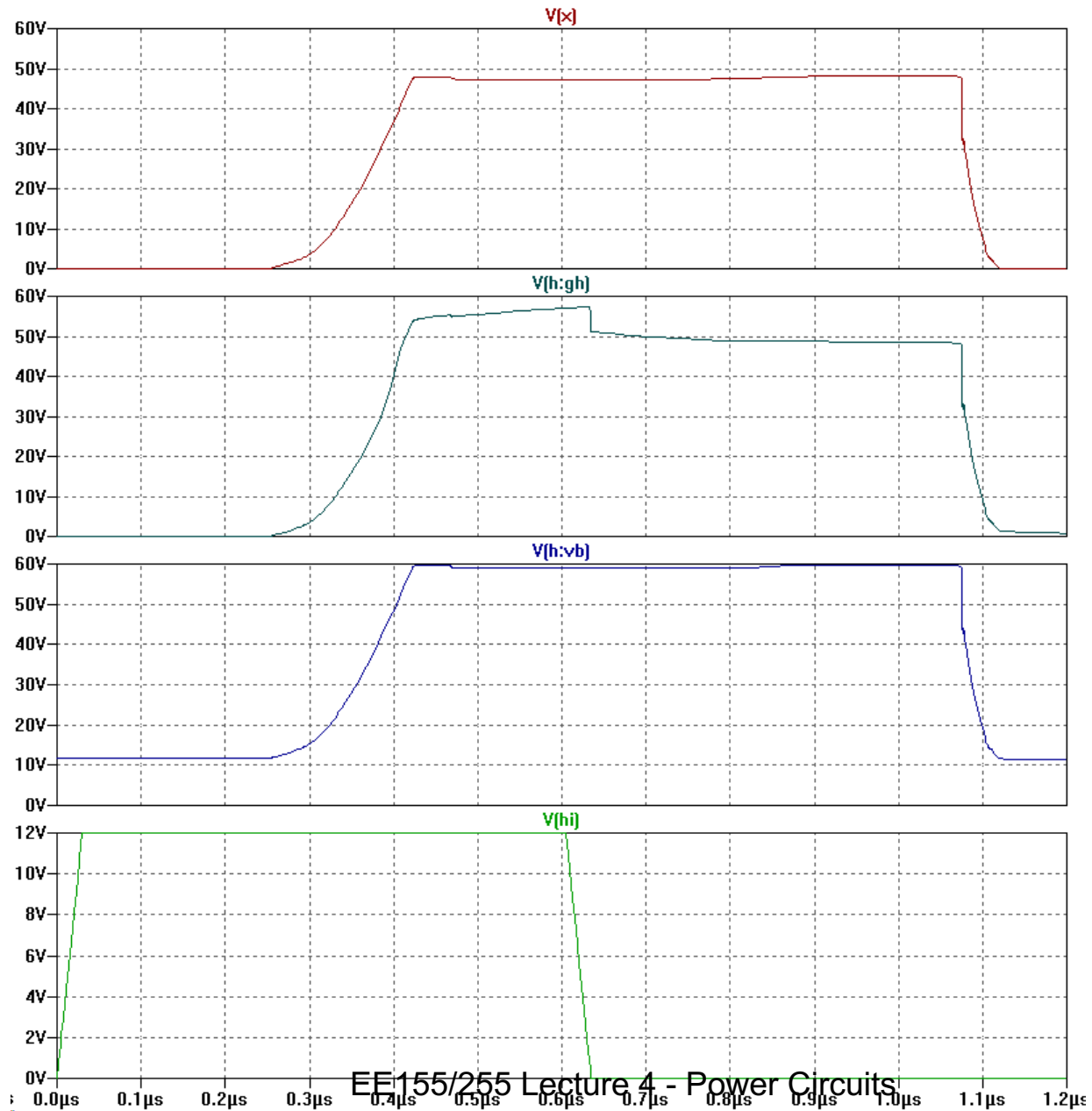
The Half-Bridge Module



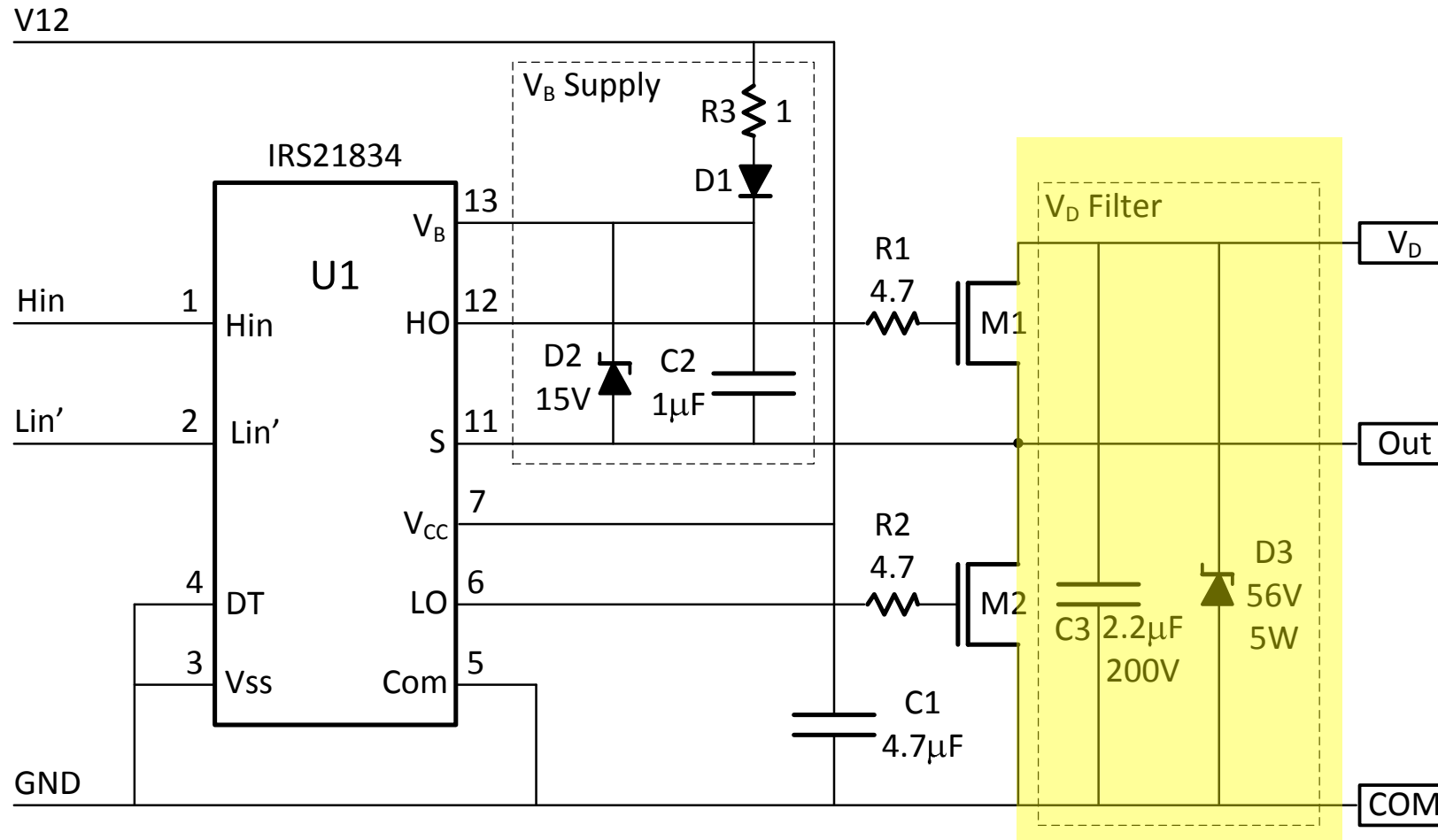
Bootstrap Supply



Bootstrap Supply

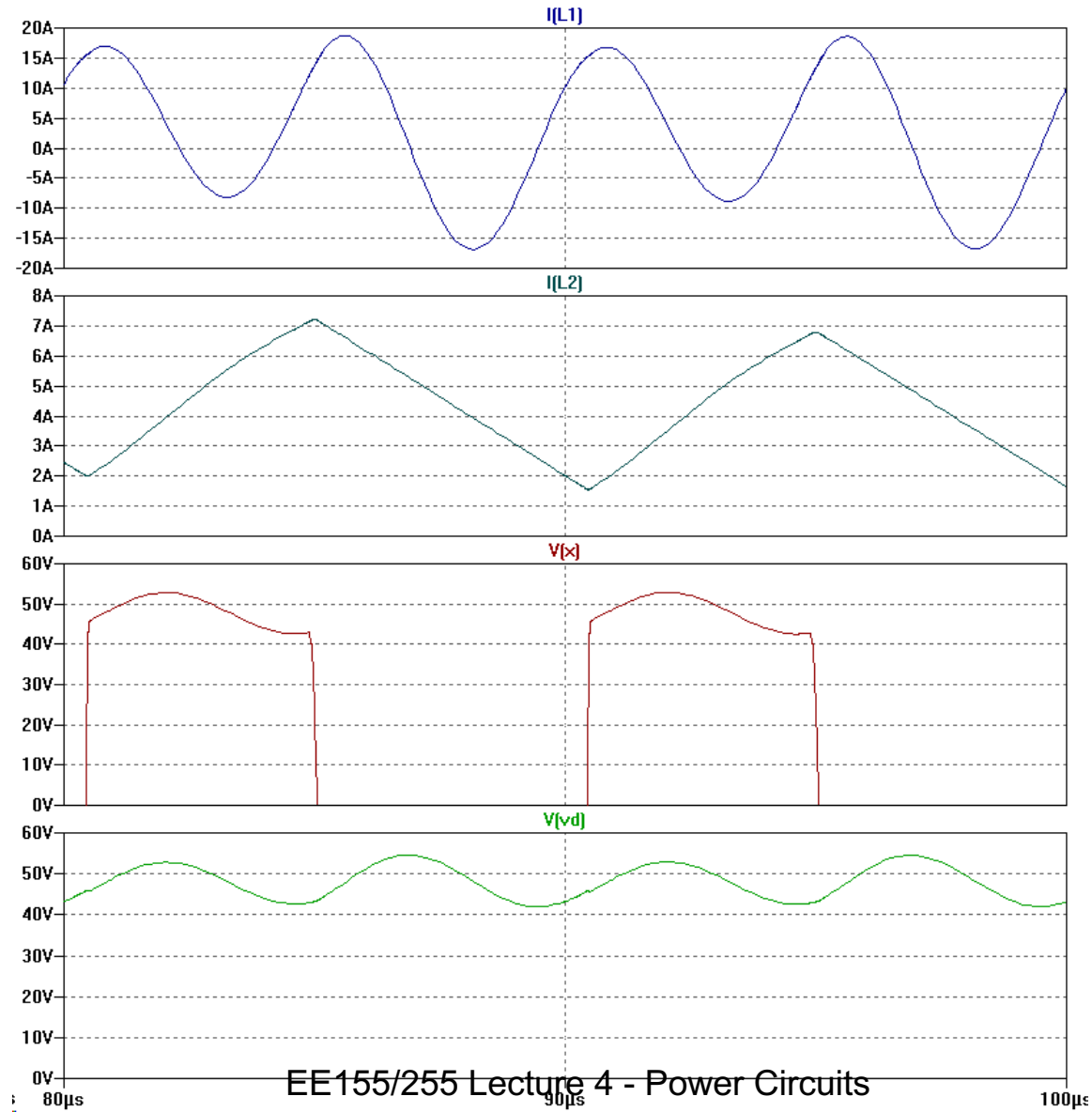


Drain Voltage Filter



Drain Voltage Filter

300nH Input Inductance



SPICE

SPICE Example – A Voltage Doubler

A Voltage Doubler

```
* Simple voltage "doubler"  
.include "gel.lib"  
.param td=100n tr=100n tf=100n tw=2.5u tcy=5u ncy=2  
.param l1=22uH c1=10uF r1=10
```

```
* call half-bridge subcircuit  
xhb vd mid g g 0 v12 gel_hb
```

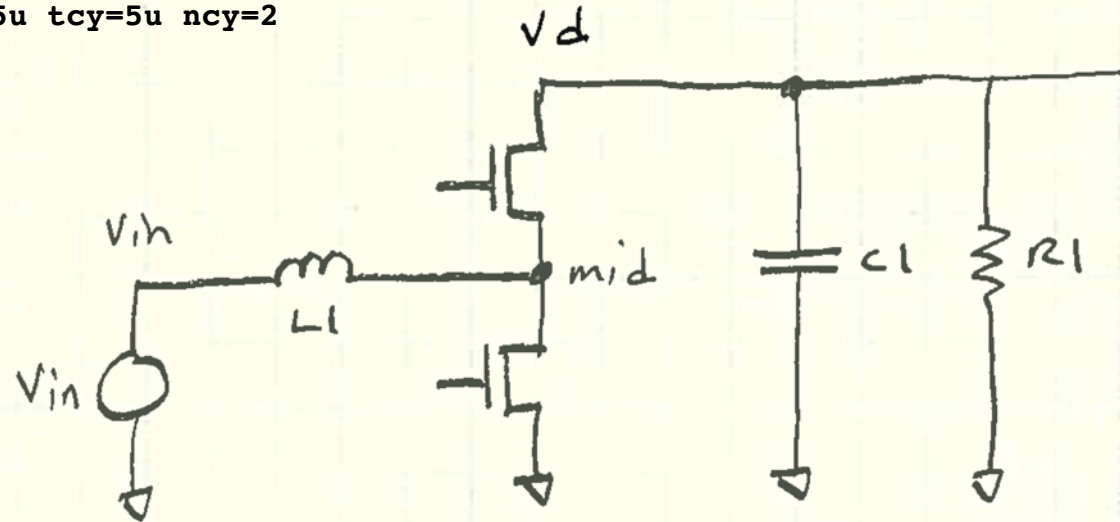
```
* circuit  
l1 vin mid {l1}  
c1 vd 0 {c1}  
r1 vd 0 {r1}
```

```
* supplies  
v12 v12 0 12  
vin vin 0 24
```

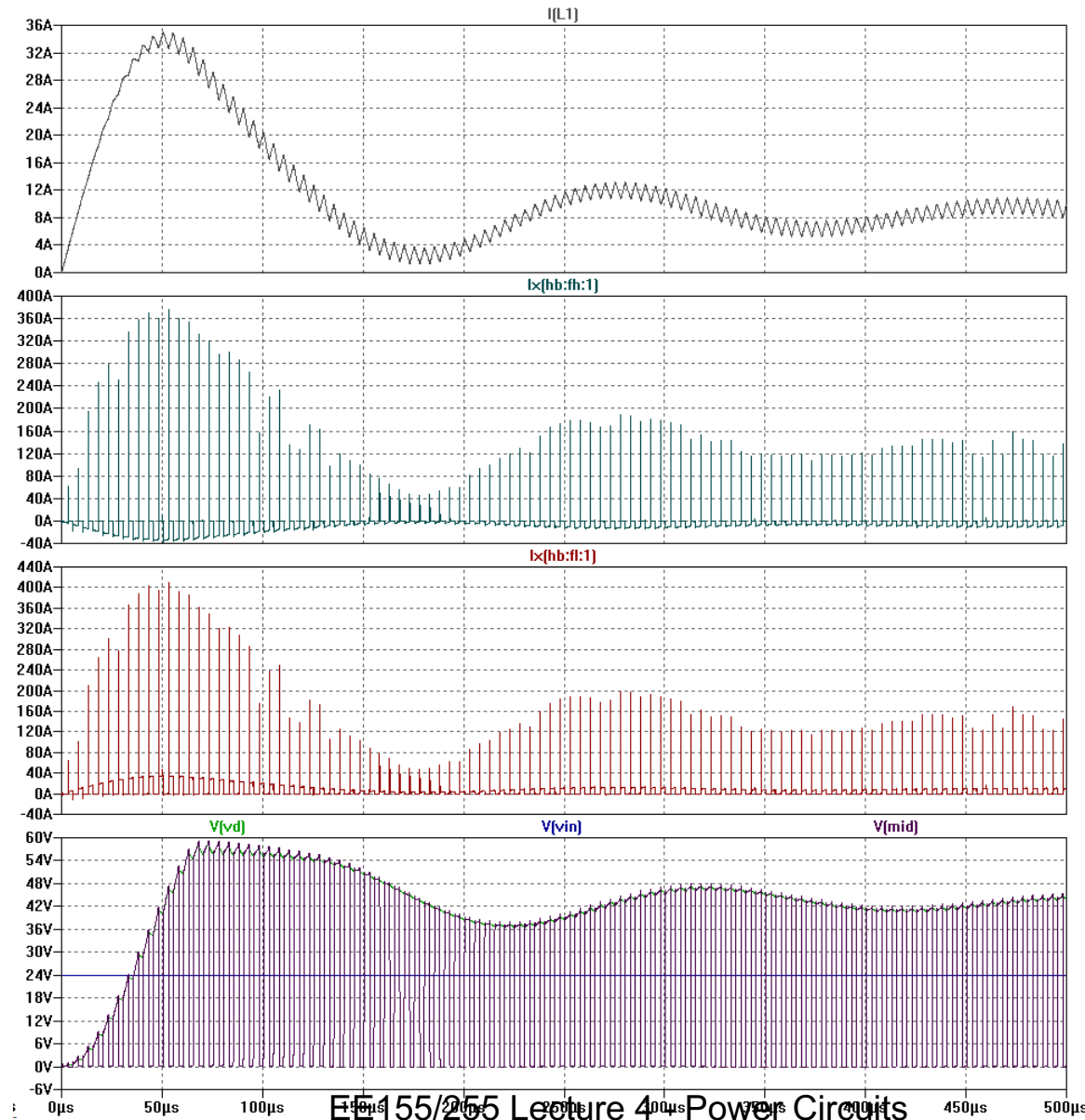
```
* stimulus  
VG g 0 PULSE(0 5 {td} {tr} {tf} {tw} {tcy} {ncy})
```

```
.ic i(l1)=9.2  
.ic v(vd)=42.8
```

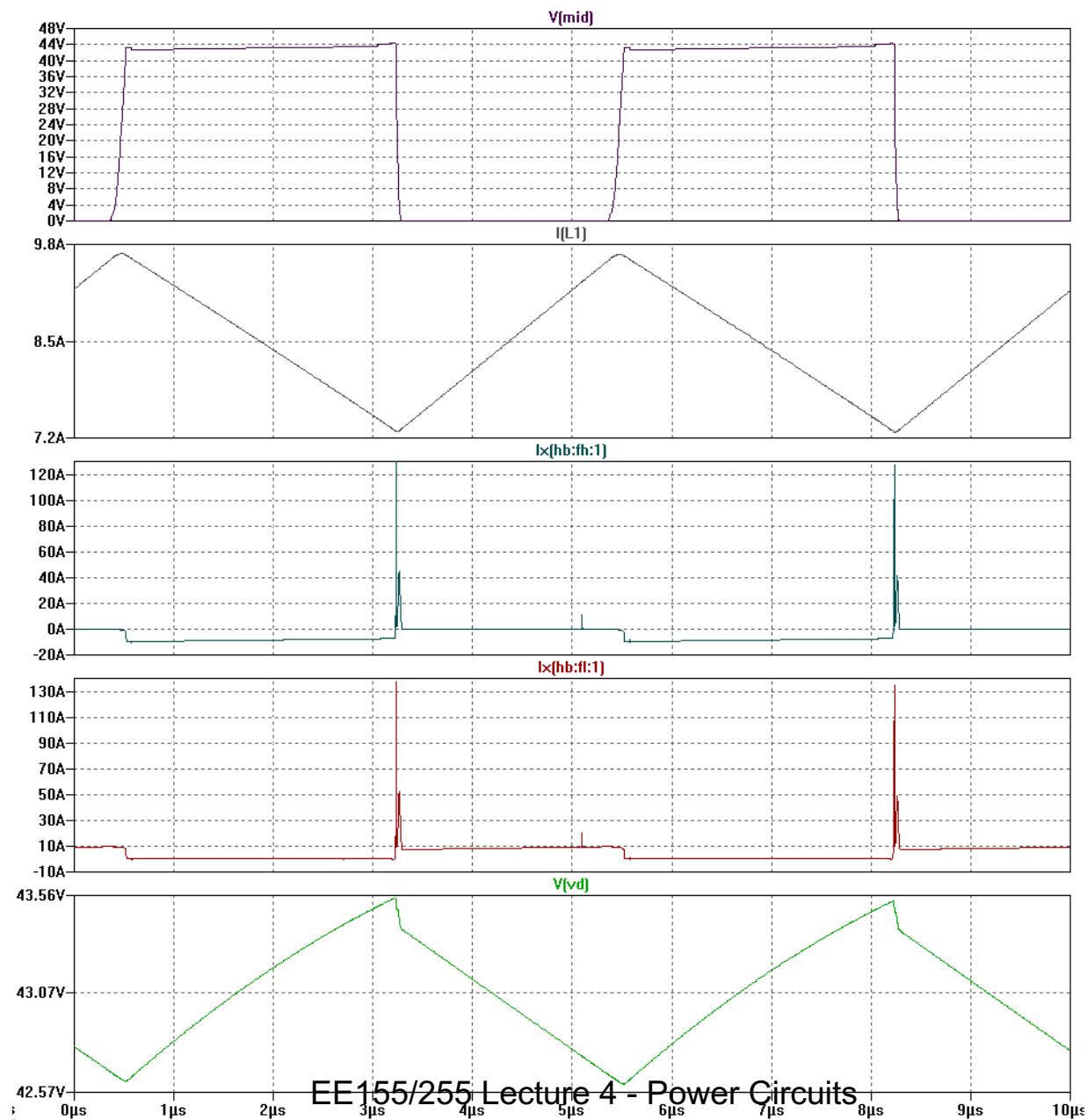
```
.tran {ncy*tcy}
```



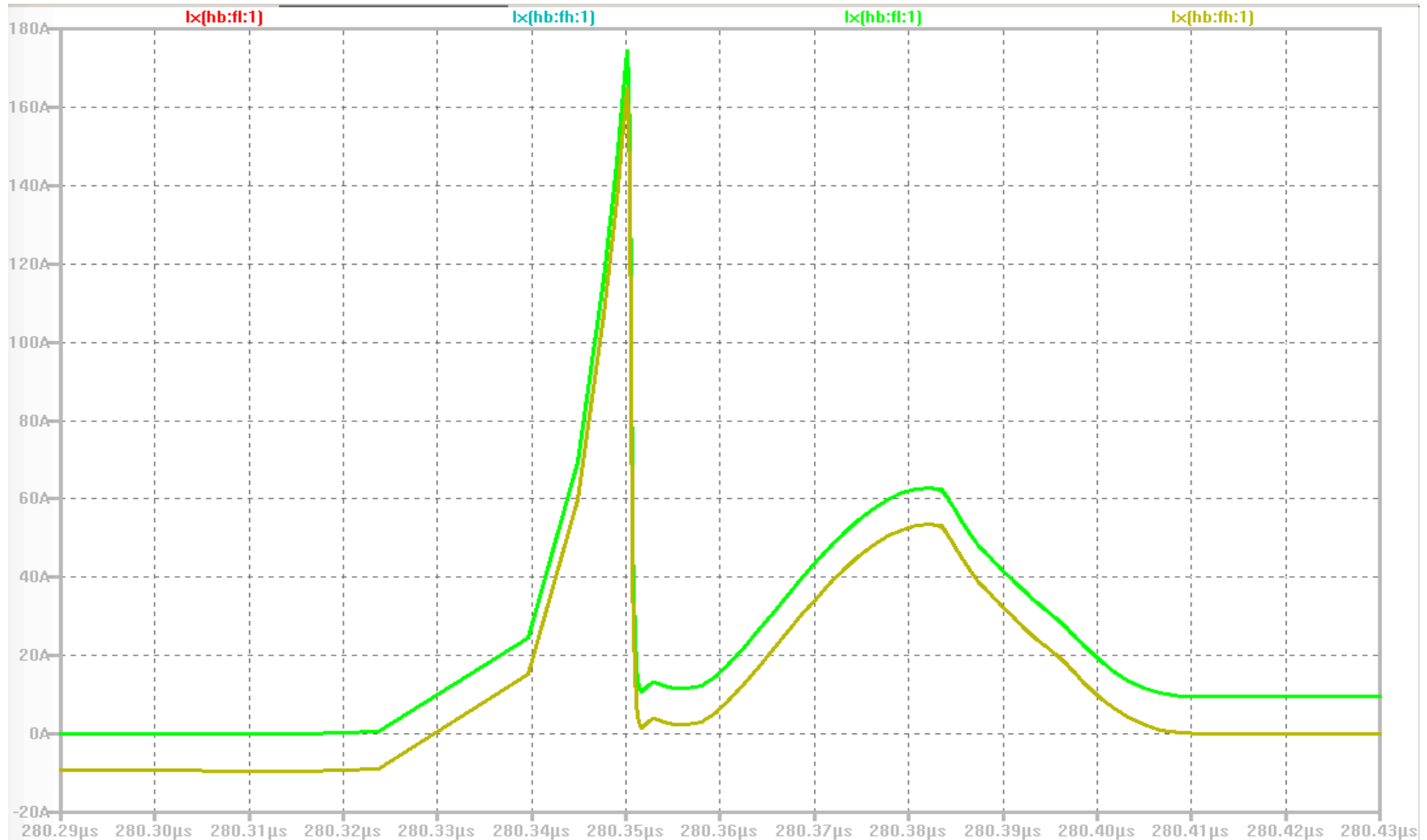
Turn-On Transient



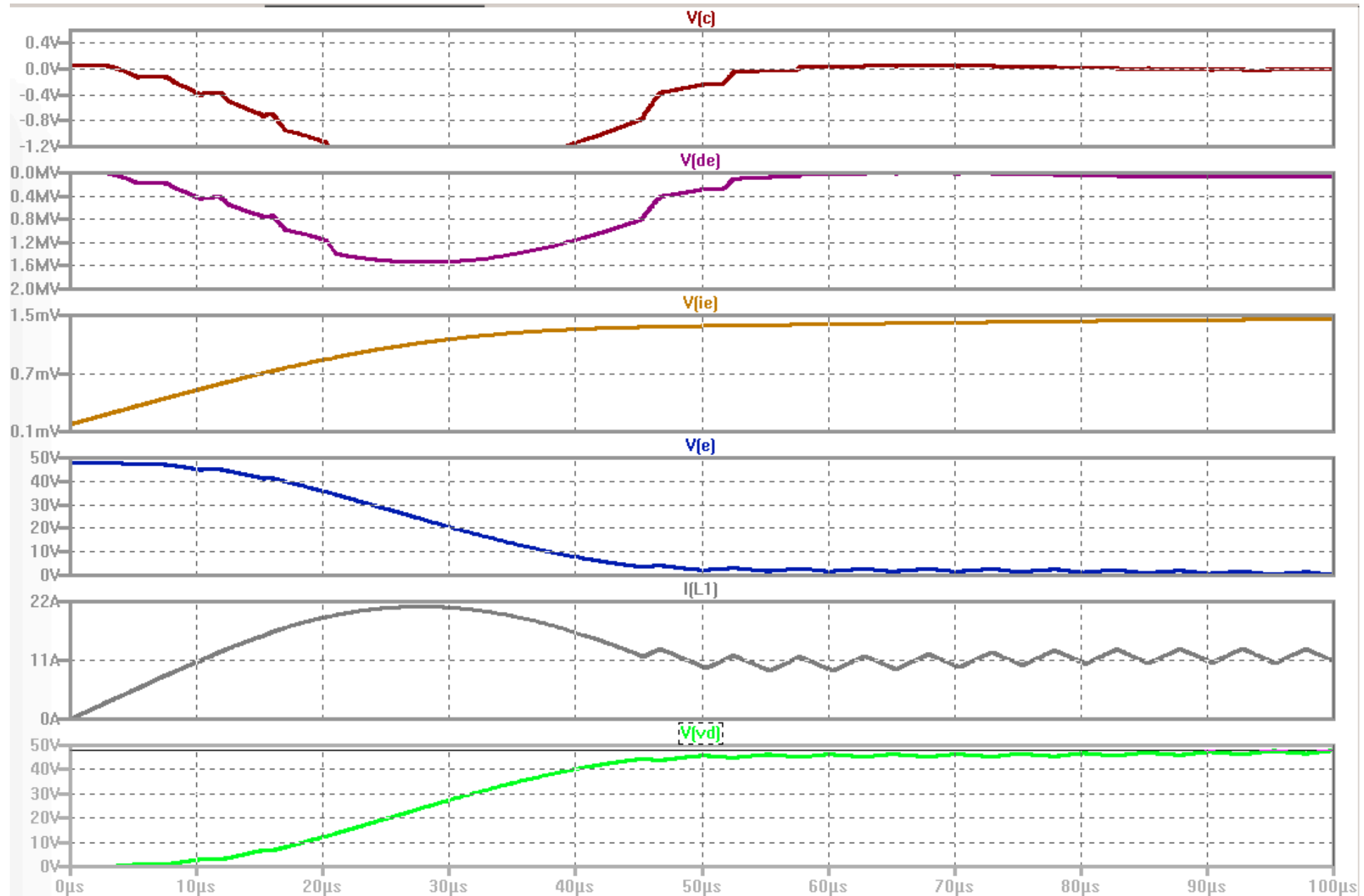
Steady State



Close up of Drain Current



With PID Control



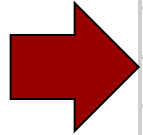
A Warning

- SPICE (or any simulator) is a ***Verification*** tool, not a ***Design*** tool
- Design your circuit first
 - Use Excel, Matlab, a calculator etc... to calculate component values
- Then simulate your circuit to check operation and fine-tune parameters
- Don't try to design your circuit using SPICE
- **Simulation is not a substitute for thinking**

Summary of Power Circuits

- Real switches have limitations
 - Conduction losses (R_{ON} for FETs, V_{CE} for IGBTs, Diode drop)
 - Switching losses (finite t_{on} , t_{off} , t_{rr})
 - With current source load, current ramps, then voltage falls
 - And voltage rises before current falls
 - May be dominated by reverse recovery time
 - Complicated by inductance
 - Parasitic L and C
- Power MOSFETs
 - Switch quickly, have linear I-V, integral diode
- IGBTs
 - Diode-like I-V, slower switching
- Diodes
 - Have reverse recovery time
- Switches operate in pairs
 - For one-way converters, one switch may be a diode
 - Synchronous rectification – make both switches FETs to reduce loss
 - Need “dead time” to avoid “shoot through” current
- Gate-drive circuits control rise and fall times
 - Supply Miller capacitance
- Bootstrap supply needed for high-side driver
- Snubbers dampen voltage and current transients
- Use SPICE as a **verification** tool, not a **design** tool

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