EE152 Final Project Report

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Summary

We set out to build a 1kW per channel Class “D” amplifier, consisting of interface and power stage modules. We succeeded in meeting our checkpoints of: (1) finalizing and sending out PCB’s to be manufactured; (2) open loop sound generation. While we did not implement a control law for the finished product as we had expected to, we feel that our efforts were well-spent on making the basic functionality of the amplifier more bulletproof, validating our hardware, experimenting with gate drives, and trying different filter values.

Statement of Work

We started our project by designing the power stage in LTspice. We focused on getting the power dissipation in our MOSFETs to a workably small level as well as experimenting with how to best condition our output voltage and current signals for feedback into our microcontroller. See Figures 1a and 1b.

We drew schematics, laid out two PCBs, and had them manufactured on a short turn. One PCB handles audio input, computer interface, and PWM generation. The other is a power stage featuring gate drive circuitry, MOSFETs, current sensing, voltage sensing, and temperature sensing. The latter sensing occurs over SPI. See Figures 2a and 2b.

We designed an inductor for the application, but were unable to receive the correct cores from Magnetics, Inc. before testing had started. Thus, we used a Coilcraft inductor that we sampled. However, a picture of the inductors (constructed, but not used on PCB) is in Figures 3. The expected power loss for the inductor we designed (0R42625UG core, 11 turns, 3.7mm gap, Figure 3b) is approximately 7.5W at a peak current of 40A and switching frequency of 200kHz.

We were able to build our device the weekend prior to checkpoint 2 and 11 days prior to the final presentation. During those 11 days we wrote basic code to get the circuit running and worked to eliminate sources of noise in the circuit. We were not able to build the second channel or implement feedback control, which were both part of the specification. However, we were able to run our circuit up to 90V (which is 5V above the maximum voltage we designed for) into an 8 ohm speaker, and we were able to generate an open loop waveform that was more accurate than our predictions.

Lessons Learned

We learned from simulation that:

- Dead-time generation in SPICE requires care and thought for best efficiency
- Diode and FET pairing is critical
- Measurement is a tough problem with such a large dynamic range

We learned from construction and testing that:

- The output LC filter has a large bearing on sound quality. A low frequency pole reduces switching noise on the output, but drastically affects frequency response of the system - a control loop would fix this. A higher frequency pole (created by removing capacitors) sounds better but has an electrically noisier output
- Isolated gate drive IC's may improve problems of switching noise returning to our MCU
- Gate drivers can easily be damaged (perhaps through over-voltage of GS nodes). Zener/TVS diodes should be used.
- By choosing to use a STM32F4Discovery development board to architecturally abstract away the problem of control hardware, we caused headaches for ourselves in terms of using "black boxes" with some amount of unknown behaviors.

Results

We succeeded in designing, building, and testing a Class "D" amplifier in approximately a month. Quick calculations from a FFT taken on our oscilloscope indicate a THD of <0.5%, but certainly less than the 1% design requirement. Given more time and more parts (we were fearful of damaging our two remaining gate drive chips), we would focus more on optimizing our switching frequency, dead time, gate drive speed, etc. Thus, we chose to focus our time on sound quality rather than improving and measuring efficiency. We do not expect to be disappointed by our efficiency numbers as no components became hot while playing loud music.

Continuing Work

We hope to build on our current work with the following improvements:

- Self contained power stage (AC to DC) so the circuit does not require lab power supplies
- Refine the power stage and eliminate conducted noise through the gate drives
- Design an FPGA based model predictive open loop controller
- Enclosure

We enjoyed working on this project and are looking forward to improving the design!

Appendix

Fig. 1a: Bridge of Power Stage

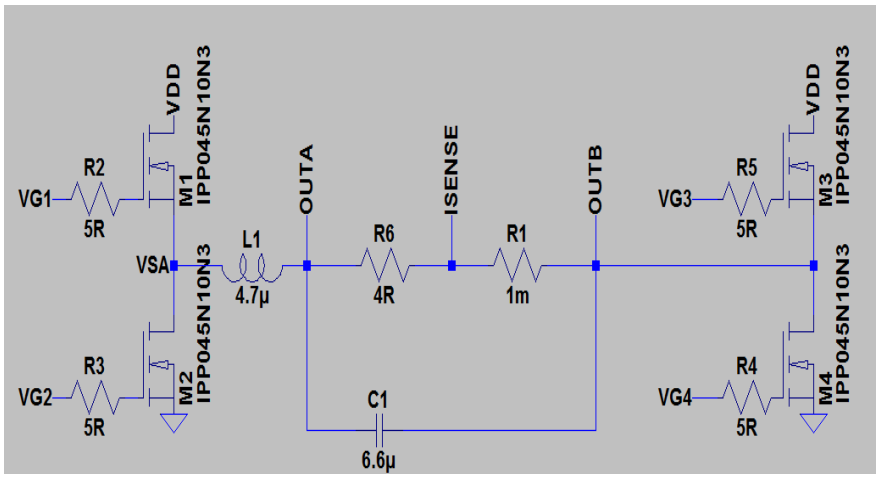

Fig. 1b: Output Ripple of Sine Wave

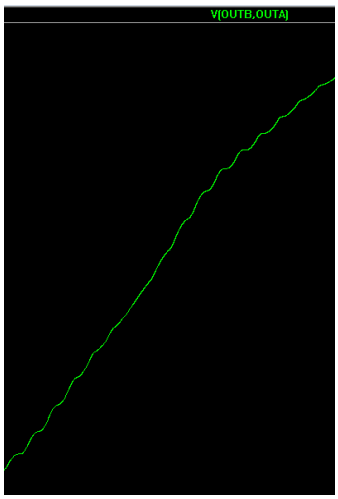

Fig 2a: Bridge of Power Stage

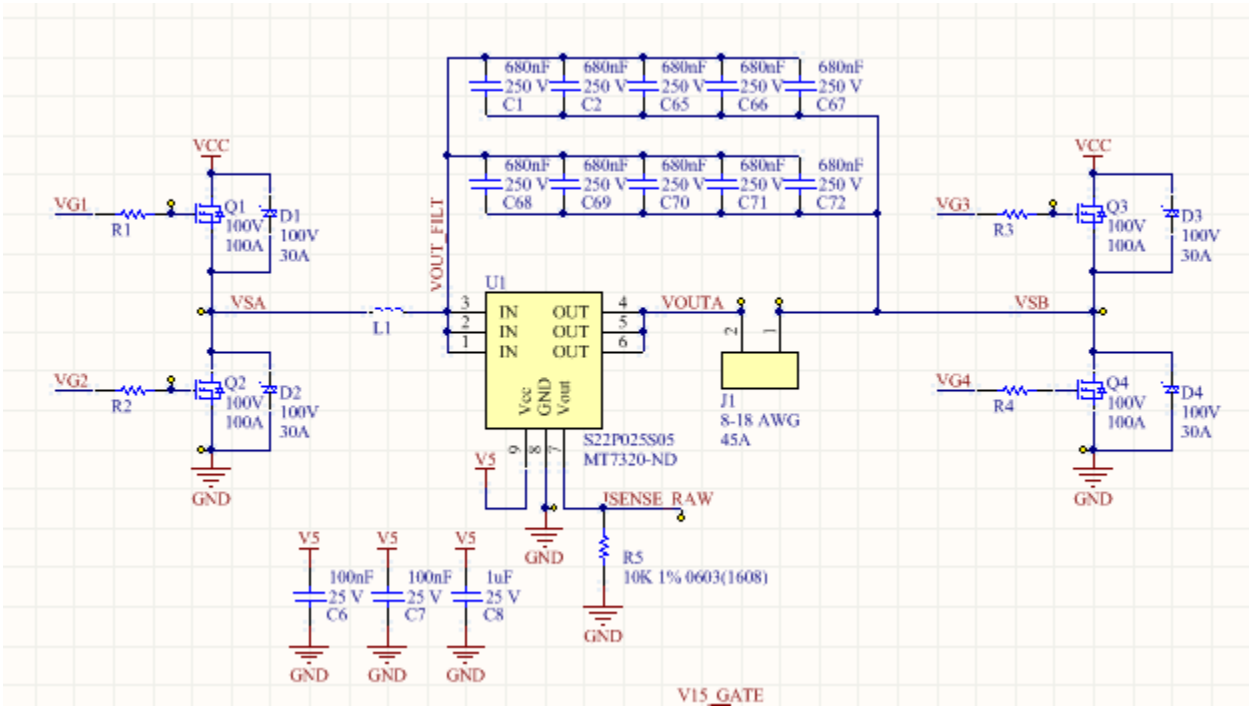

Fig 2b: Layout of Power Stage

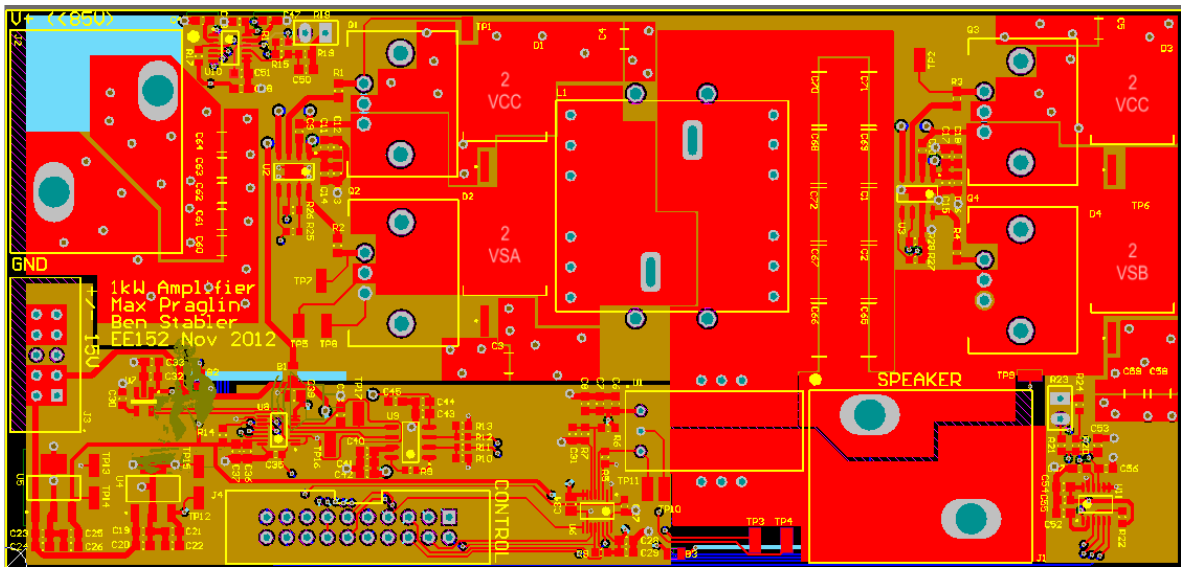

Fig 3: (left) Ferroxcube core (improperly gapped - what we had on-hand) and (right) Magnetics core (0R42625UG) inductor designed for this application

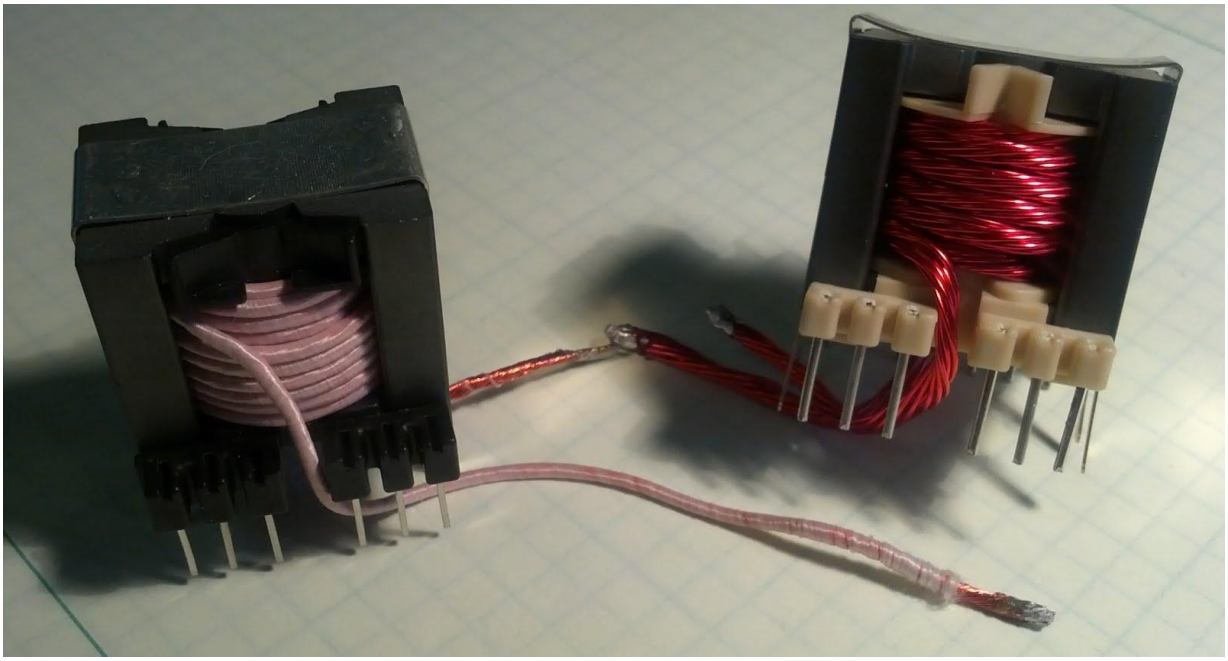

Fig 4: Constructed Power Stage

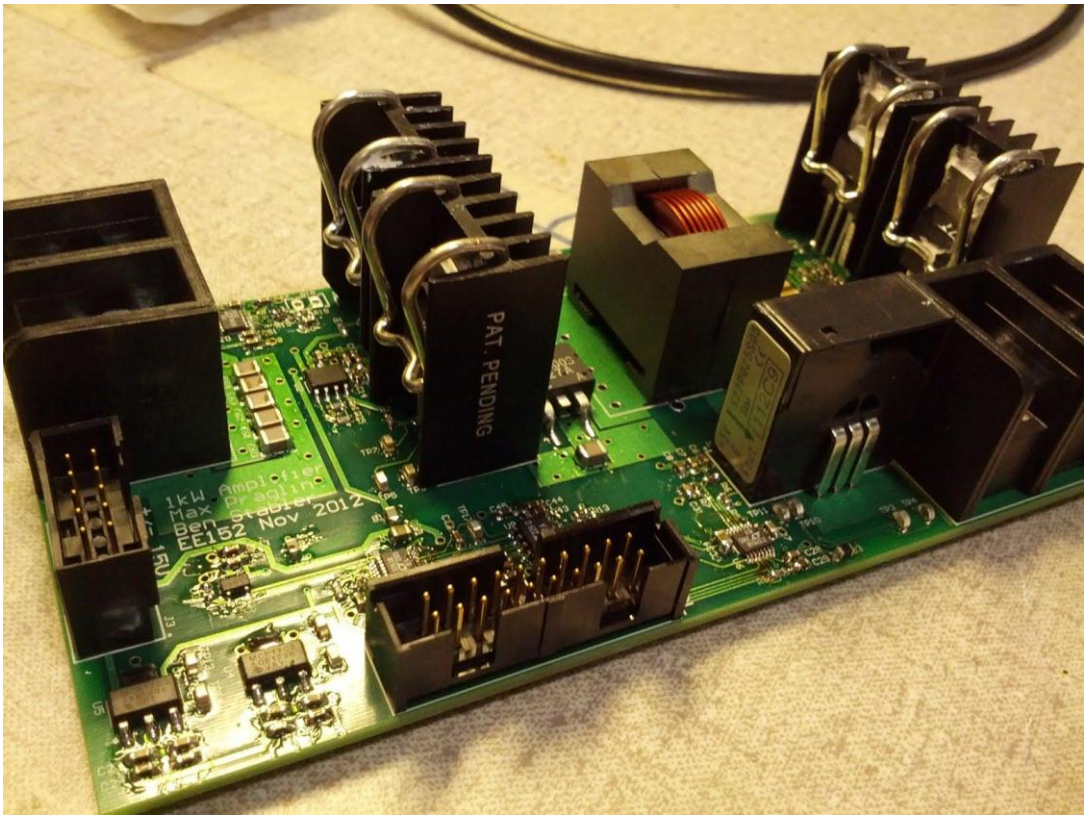

Fig 5: Testing with Differential Probes