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120V to 12V Full Bridge Converter

Summary

A full-bridge transformer was researched, analyzed, and simulated in SPICE to achieve an efficient converter architecture. We designed an AC to DC converter. Our desired power output was 1kW, giving us a current range of 8.3 to 83.3 A. We opted for the step-down from 120V to 12V due to its prevalence--it is a convenient and useful conversion, since these voltages are widely used.

The different facets of power losses were studied and subsequently addressed in order to improve efficiency from a baseline of 65% to 83%. Some critical improvements included a diodeless bridge as well as including a PFC stage. The synchronous rectification allowed us to eliminate the approximately 1.4V drop across the bridge. Soft-switching was an option as well, simply varying dead time to allow for some zero current switching. Finally, research was done to try to find parts with low parasitic resistances.

Optimization of transformer core was also crucial in lowering winding and core losses. There was a slight tradeoff between choosing a larger core for lower winding losses as opposed to one with lower core losses but higher winding losses. Bigger core results in larger core losses, while smaller core results in larger winding losses.

Finally, realistic parts and components were chosen to model the behavior as accurately as possible. The corresponding prices of each component were compiled and analyzed for cost-benefit analysis.

What We Did/What We Learned

We started off by considering different topologies of converters. One of the more straightforward approaches simply involved a buck converter. The benefits of such a design were twofold: fewer components, and potentially less power dissipated. The design would involve a rectifying stage and the buck converter itself. However, it was soon realized that a buck converter would not be a wise choice since it would involve components that needed to tolerate both high voltage (120V) and high current (83A) simultaneously. Furthermore, the grounds would not be isolated, and as such, the DC output's ground would be coupled to the AC signal, making it quite unsafe. Consequently, it was decided that a full-bridge transformer topology would be most appropriate.

After designing a basic prototype, we were seeing a power efficiency of 65.4% and power factor of 0.77. It was apparent that synchronous rectification was necessary. The diodes were giving us a 1.4V drop the significantly degraded our performance, particularly on the low voltage

side.

In addition to replacing the diodes, a PFC stage was added in. The use of non-linear components will largely affect the current waveform. As such, a PFC stage will help to bring the power factor closer to 1. Even within the PFC stage, we decided to replace the diode with a MOSFET. We learned, however, that most of our power losses were coming from poorly chosen components. It was thus necessary to find more efficient substitutes.

For the transformer stage, optimizing the core was a game of optimizing power loss between the core and the windings. A larger core would reduce the winding losses, but would also increase the core losses. On the other hand, the smaller core would be a cheaper alternative. However, choosing a bigger core would prevent saturation from occurring too quickly. It was also necessary to choose an appropriate wire gauge. Too thin and we would not be able to support our switching frequency of 200kHz. It was thus necessary to use many strands of a thinner gauge wire in order to efficiently utilize the copper in the wire. In essence, it was necessary to have a radius smaller than the skin depth. Thus, a wire gauge of 29 was chosen.

We opted to keep the diodes on the first rectifying stage, thinking that a 1.4V drop on the high voltage side would not be too significant of a loss. We made a reasonable assumption that the difference between the drop from the diodes and that of the switching and conduction loss due to 4 MOSFETs would be negligible.

In simulating our design, we learned that the SPICE default devices are not always your friend! Choosing real components, even if they weren't efficient, drastically changed our model behaviour. Moreover, we found that planning for and allowing for dead time was an important factor in reducing unwanted spikes in current and/or voltage. With switching frequency, there seemed to be a narrow range for which we could actually switch. As such, we opted to not delve too deep into trying to figure out switching frequency. In dealing with MOSFETs turning on and off, it was important to keep track of where your source node was, in relation to the rest of the circuit. In practice, it is often necessary to use special chips to drive the top-side MOSFETs in an H-bridge.

Key Results

Before optimization:

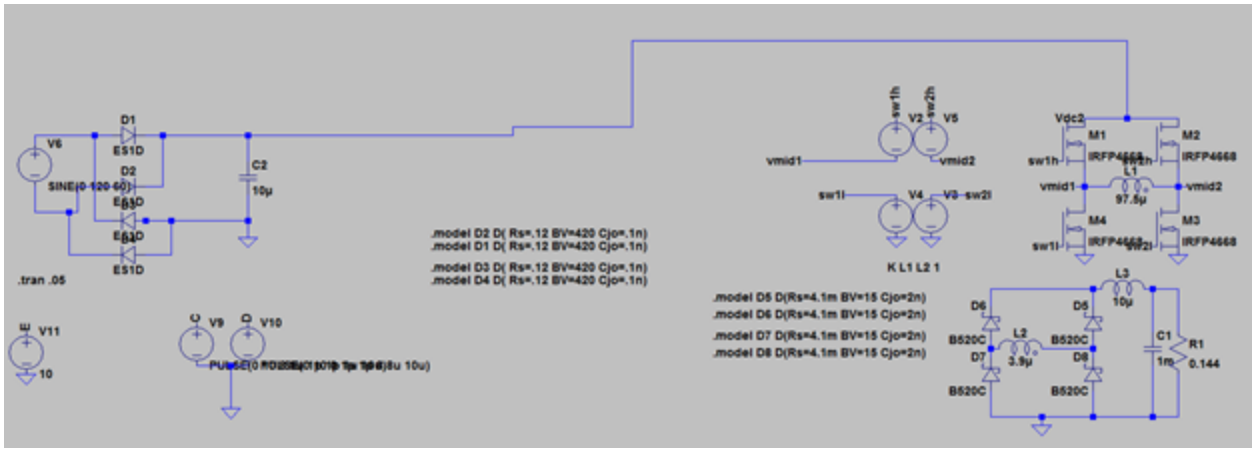

Figure 1 - Basic transformer prototype

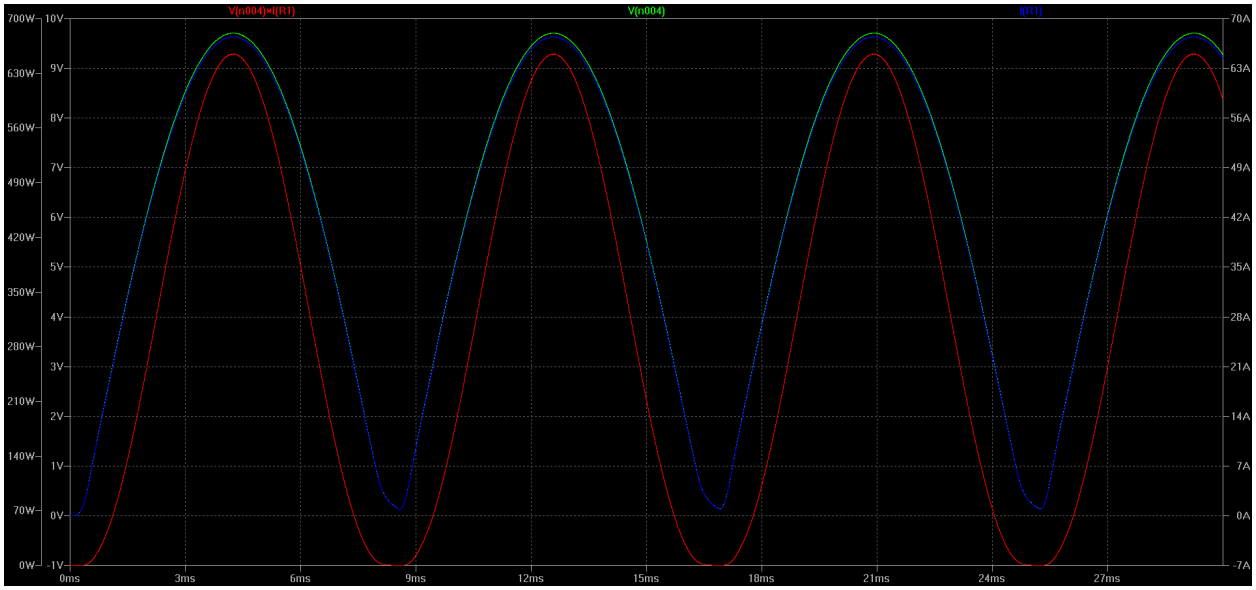

Figure 2 - Output waveform for basic transformer prototype.

	Average	RMS	Peak
V (volts)	5.932	6.7518	9.7
I (amps)	41.195	46.888	67.42
P (watts)	316.58	244.368	654.6

PF = .771
Efficiency = 65.46%

After optimization:

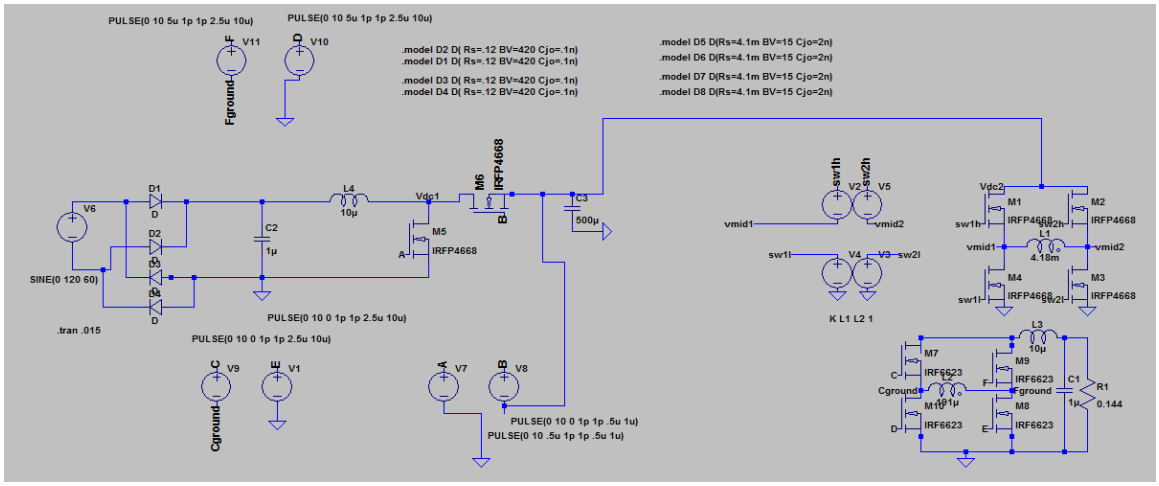

Figure 3 - Final schematic, with PFC stage, diodeless bridge, and optimized components.

	Average	RMS	Peak
V (volts)	6.925	7.757	10.73
I (amps)	48.091	53.87	77.96
P (watts)	333.03	418.03	836.45

PF = 0.7966
Efficiency = 83.64%

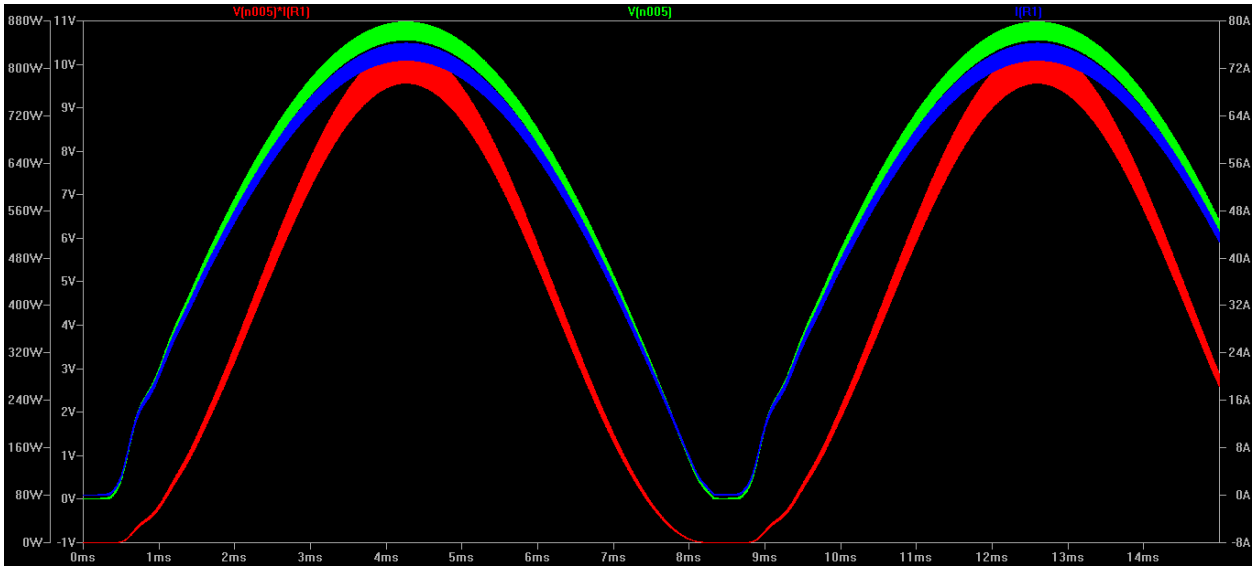

Figure 4 - Waveform of converter after optimization.

In an attempt to correct for the non-DC signal we were seeing, we tried to increase the capacitance on C3. However, this only resulted in a significant loss in metrics. In addition, only when we utilized capacitance values in the tens to hundreds of milliwatts were we able to see any sort of steady DC signals.

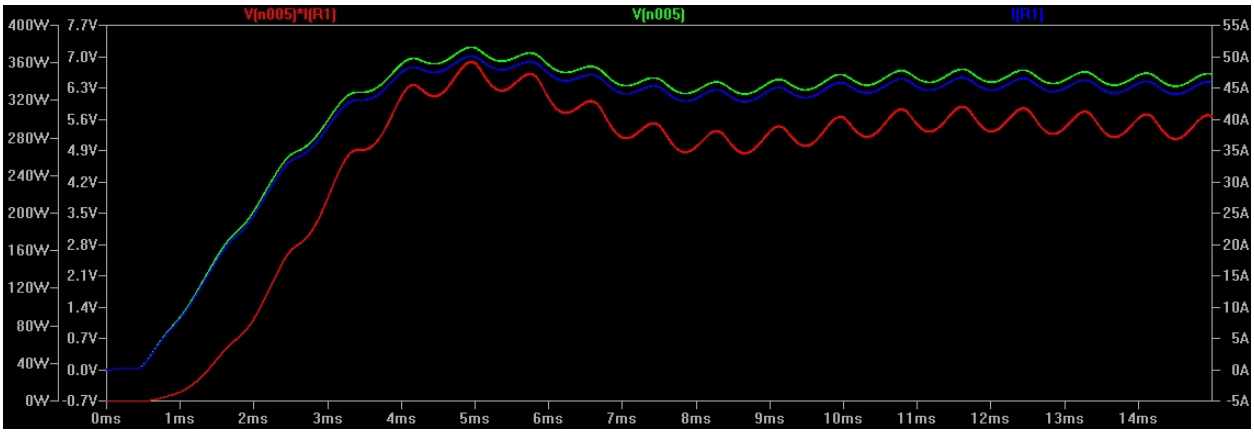

Figure 5 - Rectified waveform, with power measurements. Efficiency at 30%.

List of parts

Because we wanted our model to be as realistic as possible, we used components in our simulation that modeled existing parts. This made our model behave a lot more like a real circuit, and we hoped this would make our efficiency analysis model the losses more accurately.

Basic prototype

	Part Number	Price	Total Units Required	Total cost
Diodes	ES1D	0.49	4	1.96
	B520C	0.74	4	2.96
MOSFETs	IRFP4668	5.15	6	30.9
	Core ferrite E42/21/15	2.46	1	2.46
			Total	38.28

Optimized prototype:

	Part Number	Price ($)	Total Units Required	Total cost ($)
Diode	S10D	0.66	4	2.64
MOSFETs	IRFP4668	5.15	6	30.9
	IRF6623	3.16	4	12.64
Large Capacitor	TC4990	18.07	1	18.07
Core ferrite	E42/21/15	2.46	1	2.46
			Total	66.71

The optimized design gave us a 27.7% increase in efficiency. The cost increase, however, was at 75%. It is suggested to have a more in depth research into how each stage might have contributed to the cost as well as how each stage might have contributed to efficiency increase. However, it can argued that the energy savings outweigh the initial upfront cost of the system.

In the end, we were able to achieve our goal of at least 80% efficient converter. We did not, however, have sufficient time to actually carry out our design.

Next Steps

The next steps that we'd like to take would be to order the parts and have the circuit laid out in hardware. This would involve some more detailed analysis on the gate controllers and how to effectively control the switching of the several MOSFETs in our circuit. We would also like to figure out the reason why achieving a DC signal was difficult to achieve in our simulation. Finally, including soft-switching effectively would be our next goal.