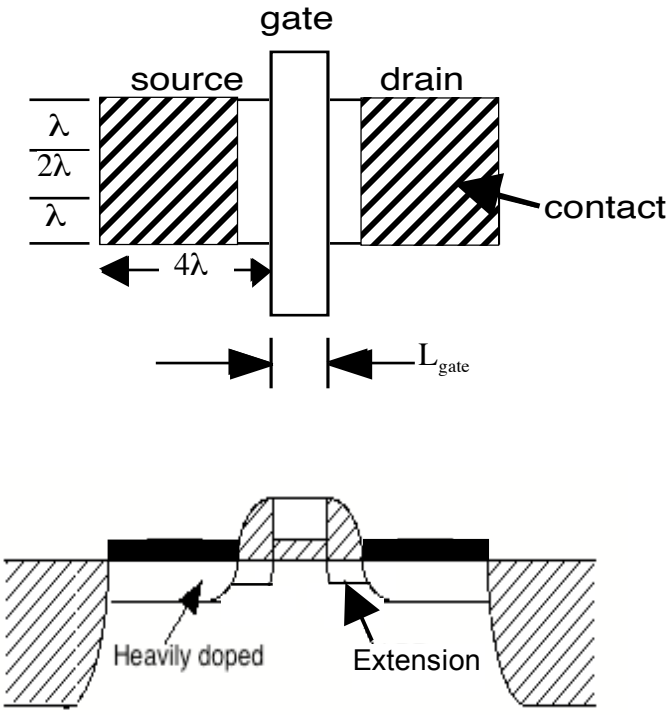
EE311 - Spring 2006
PROBLEM SET #4
Assigned: Wednesday, April 26, Due: Wednesday, May 3

PROBLEM 1



NMOS transistors with W = 4λ are designed using λ design rules as shown in the figure above schematically. For various technology nodes, extension sheet resistance, spacer thickness, deep source and drain junction depth, and specific contact resistivity are given in the Table I. Assume the deep source and drain are doped homogeneously at a density of 5e20 cm^{-3}.

Table I

Year **(Technology node = 2λ)**	2007 (65nm)	2010 (45nm)	2013 (32nm)
L_{gate} (nm)	32	22	16
EOT (nm)	1.2	1.0	0.9
V_{DD} (V)	0.9	0.8	0.7
V_T (V)	0.29	0.27	0.25
Extension sheet resistance (ohm/sq)	360	390	440
Spacer thickness (nm)	28	19	15
Deep source and drain x_j (nm)	28	19	15
Specific contact resistivity (ohm-μm^2)	11	6.4	3.8

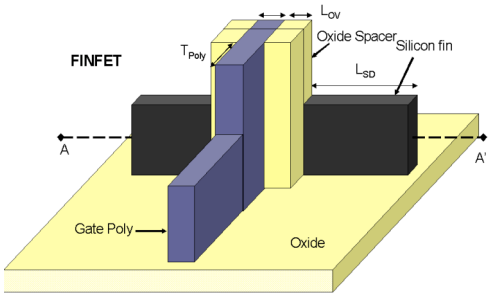
a) Calculate the extension, deep source/drain, and contact resistance of the junctions. Plot the total resistance (with breakdowns of the three components) vs. technology node.

b) I_{on} of an MOS transistor is generally derived assuming no parasitic resistance in source and drain. In reality there can be appreciable resistance due to shallow junctions and contacts. How does the presence of the finite resistance in source and drain impact the value of I_{on}? Calculate the change in I_{on} (with & without series resistance) vs. technology node. Use the velocity saturation model:

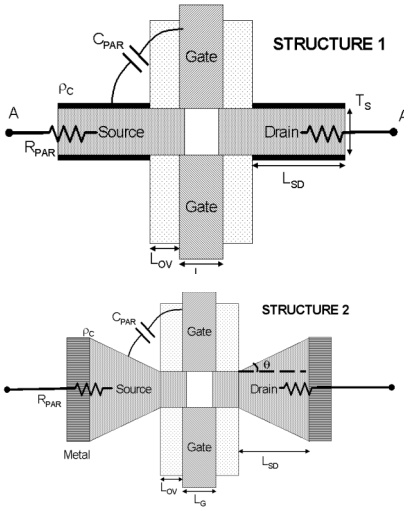
$$I_{ds} = \frac{W v_{sat} C_{ox} (V_{gs} - V_t)^2}{(V_{gs} - V_t) + \frac{2 v_{sat} L_{eff}}{\mu_{eff}}}$$

where μ_{eff} = 0.03 m^2/Vsec and v_{sat} = 8x10^4 m/sec

Problem 2: Effect of Source/Drain morphology on Transistor Performance



In thin film devices, the ON current in the device is severely limited by the parasitic resistance in the source and drain (SD) regions. The adjoining figure shows a highly simplified version of the FINFET. Struture1 is the cross section of this device along AA'. This structure has a high resistance due to current flowing in such a thin Si film. To mitigate this effect, a flared SD has been suggested as in structure 2. However, structure 2 has a higher gate-source capacitance than structure 2 which makes it slower. You will need to choose the best structure by trading off current for capacitance. For this problem, assume the following parameters for the transistor. For all parts vary θ; the angular spread at the source in structure 2 from 10° to 40°.



Gate length L_G=20nm
Si body thickness T_S= 10nm
Oxide thickness T_{OX}=1.2nm
Specific contact resistivity ρ_C = 1e-7 Ω-cm^2.
Maximum SD doping N_{SD} = 1e20 cm^{-3}.
Maximum SD length L_{SD} =2*L_G.
Thickness of the Poly T_{Poly} = 50nm
Channel Width W=1μm.

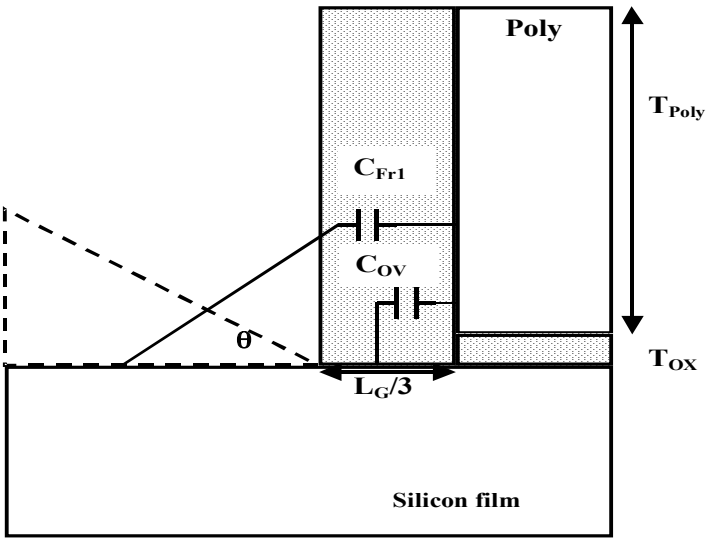
(a) Calculate the resistance (R_{PAR}) of the Source region in structure 1and structure 2. Vary the angle of fan-out (θ) in structure2 from 10° to 60°. ($R_{PAR} = R_{DOPEDSI} + R_{CONTACT}$). There is an additional component in structure 2 due to current spreading from a thin film into a wider region. We will neglect it here, as we are using small angular spreads at the source.

(b) Calculate the effective ON current (I_{ON}) for the structures. Use the ballistic model for the maximum ON current. Use V_{DD}=1V and V_{TH}=0.4V. Assume that the V_{TH} of the device does not change with external resistance at the Source. Remember there are two transport channels in this device.

$$I_{ON} = 2WC_{OX}\left(V_{GSeff} - V_{TH}\right)v_i$$

Use v_i= 1.3e+7 cm/sec.

(c) Calculate the net gate capacitance in these structures. Use ε_{eff}=5



$C_G = C_{OXl} + C_{OV} + C_{Fringe}$

$$C_{OV} = \varepsilon_{OX} W \ln\left[1 + \frac{L_G}{3T_{OX}}\right]$$

$$C_{Fringe} = \frac{\varepsilon_{OX} W}{\frac{\pi}{2} - \theta} \ln\left[1 + \frac{T_{Poly}}{\left(\frac{L_G}{3}\right)}\right]$$

$$C_{OXl} = \frac{\varepsilon_{OX} W L_G}{T_{OX}}$$

(d) The intrinsic device delay is a parameter used to compare devices given by:

$$\tau_D = \frac{C_G V_{DD}}{I_{ON}}$$

Find the angle at which structure2 has a lower intrinsic delay than structure1.

(You can use the bulk resistivity of Si doped at 1e20 cm^{-3} N doping for calculating the resistance contribution due to the doped regions. For 1e20 cm^{-3}, the resistivity is 0.8mΩ-cm.)