Outline

• Interconnect scaling issues
• Polycides, silicides and metal gates
• Aluminum technology
• Copper technology

Wire Half Pitch vs Technology Node

ITRS 2002

Ref: J. Gambino, IEDM, 2003

Narrow line effects
Interconnect Scaling Scenarios

- **Scale Metal Pitch with Constant Height**
  - R, C_s, and J increase by scaling factor
  - Higher aspect ratio for gapfill / metal etch
  - Need for lower resistivity metal, Low-k

- **Scale Metal Pitch and Height**
  - R and J increase by square of scaling factor
  - Sidewall capacitance unchanged
  - Aspect ratio for gapfill / metal etch unchanged
  - Need for very low resistivity metal with significantly improved EM performance

Why Copper?

Low ρ (Resistivity)

<table>
<thead>
<tr>
<th>Metal</th>
<th>Bulk Resistivity [µΩ·cm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ag</td>
<td>1.63</td>
</tr>
<tr>
<td>Cu</td>
<td>1.67</td>
</tr>
<tr>
<td>Au</td>
<td>2.35</td>
</tr>
<tr>
<td>Al</td>
<td>2.67</td>
</tr>
<tr>
<td>W</td>
<td>5.85</td>
</tr>
</tbody>
</table>

Cu is the second best conducting element

\[
RC = \frac{p}{t_M} \cdot \frac{L^2}{t_{ILD}}
\]

Calculations assume longest interconnect in the chip controls delay
Cu Has Excellent Reliability

<table>
<thead>
<tr>
<th></th>
<th>Al</th>
<th>Cu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Melting Point</td>
<td>660 ºC</td>
<td>1083 ºC</td>
</tr>
<tr>
<td>$E_a$ for Lattice Diffusion</td>
<td>1.4 eV</td>
<td>2.2 eV</td>
</tr>
<tr>
<td>$E_a$ for Grain Boundary Diffusion</td>
<td>0.4 – 0.8 eV</td>
<td>0.7 – 1.2 eV</td>
</tr>
</tbody>
</table>

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Why Cu and Low-k Dielectrics?

- Better electromigration resistance, reduced resistivity and dielectric constant results in reduction in number of metal layers as more wires can be placed in lower levels of metal layers.

$$RC = \frac{\rho}{t_M} \cdot \frac{L^2 \varepsilon_{ILD}}{t_{ILD}}$$

Ref: M. Bohr, IEDM 1995.
**Problem: Copper Diffusion in Dielectric Films**

Cu atoms ionize, penetrate into the dielectric, and then accumulate in the dielectric as Cu+ space charge.

**Copper Diffusion in Dielectric Films**

Bias temperature stressing is employed to characterize behavior
- Both field and temperature affect barrier lifetime
- Neutral Cu atoms and Cu ions contribute to Cu transport through dielectrics

Ref: A. Loke et al., Symp. VLSI Tech. 1998

*Silicon nitride and oxynitride films are better barriers*
Solutions to Problems in Copper Metallization

- Fast diffusion of Cu into Si and SiO₂
- Poor oxidation/corrosion resistance
- Poor adhesion to SiO₂

Diffusion barrier/adhesion promoter

Passivation

- Difficulty of applying conventional dry-etching technique

Damascene Process

Barriers/Linears

Must be removable by CMP & not enhance corrosion

Thickness limited by:
- Line resistance goals
- Copper fill capability

Must have good adhesion to insulator and copper.

Space for wire

Thickness and resistivity important to via resistance

Low contact resistance to copper required
Materials for Barriers / Liners

- Transition metals (Pd, Cr, Ti, Co, Ni, Pt) generally poor barriers, due to high reactivities to Cu <450° C. Exception: Ta, Mo, W ... more thermally stable, but fail due to Cu diffusion through grain boundaries (polycrystalline films)
- Transition metal alloys: e.g., TiW. Can be deposited as amorphous films (stable up to 500° C)
- Transition metal - compounds: Extensively used, e.g., TiN, TaN, WN.
- Amorphous ternary alloys: Very stable due to high crystallization temperatures (i.e., Ta3Si14N50, Ti3Si23N43)
- Currently PVD (sputtering/evaporation is used primarily to deposit the barrier/liner, however, step coverage is not good & ALD is being developed for new application.

Interconnect Fabrication Options

![Fabrication Options Diagram]

- Positive Pattern
- Metal Etch
- Dielectric Deposition
- Dielectric Planarization by CMP
- Subtractive Etch (Conventional Approach)
- Negative Pattern
- Dielectric Etch
- Metal Deposition
- Dielectric Deposition
- Metal CMP
- Etch Stop (Dielectric)
Various deposition methods for Cu metallization have been attempted:

- **Physical vapor deposition (PVD): Evaporation, Sputtering**
  - conventional metal deposition technique: widely used for Al interconnects
  - produce Cu films with strong (111) texture and smooth surface, in general
  - poor step coverage: not tolerable for filling high-aspect ratio features
Various deposition methods for Cu metallization have been attempted:

- **Physical vapor deposition (PVD):** Evaporation, Sputtering
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  - Poor step coverage: not tolerable for filling high-aspect ratio features

- **Chemical vapor deposition (CVD):**
  - Conformal deposition with excellent step coverage in high-aspect ratio holes and vias
  - Costly in processing and maintenance
  - Generally produce Cu films with fine grain size, weak (111) texture and rough surface

- **Electrochemical deposition (EVD):**
  - Good step coverage and filling capability comparable to CVD process (0.25 µm)
  - Compatible with low-K dielectrics
  - Generally produce strong (111) texture of Cu film
  - Produce much larger sized grain structure than any other deposition methods through self-annealing process
Deposition methods: Electroplating

Copper electroplating Chemistry:

- Plating Bath: standard sulfuric acid copper sulfate bath (H₂SO₄, CuSO₄ solution)
- Additives to improve the film quality

Dissociation: CuSO₄ $\rightarrow$ Cu²⁺ + SO₄²⁻ (solution)
Oxidation: Cu $\rightarrow$ Cu²⁺ + 2e⁻ (anode)
Reduction: Cu²⁺ + 2e⁻ $\rightarrow$ Cu (cathode, i.e., wafer)

Trench Filling PVD vs. Electroplating of Cu

PVD

Electroplating
Additives for Copper ECD

**DEFINITION**

- Mixture of organic molecules and chloride ion which are adsorbed at the copper surface during plating to:
  - enhance thickness distribution and feature fill
  - control copper grain structure and thus ductility, hardness, stress, and surface smoothness

**COMPONENTS**

- Most commercial mixtures use 3 or more organic components and chloride ion which adsorb at the cathode during plating.

Brighteners (Accelerators) Levelers Carriers Chloride Suppressors

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**Mechanisms of Superconformal Cu plating**

- Wafers immersed in plating bath. Additives not yet adsorbed on Cu seed.
- Additives adsorbed on Cu seed. No current flow.
- Conformal plating begins. Accelerators accumulate at bottom of via, displacing less strongly absorbed additives.
- Accumulation of accelerator due to reduced surface area in narrow features, causes rapid growth at bottom of via.

Role of Additives

Brighteners (Accelerators)
- Adsorb on copper metal during plating, participates in charge transfer reaction. Determines Cu growth characteristics with major impact on metallurgy.

Levelers
- Reduce growth rate of copper at protrusions and edges to yield a smooth final deposit surface.
- Effectively increases polarization resistance at high growth areas by inhibiting growth to a degree proportional to mass transfer to localized sites.

Carriers
- Carriers adsorbed during copper plating to form a relatively thick monolayer film at the cathode (wafer). Moderately polarizes Cu deposition by forming a barrier to diffusion of Cu^{2+} ions to the surface.

Chloride
- Adsorb at both cathode and anode.
- Accumulates in anode film and increases anode dissolution kinetics.
- Modifies adsorption properties of carrier to influence thickness distribution.

Effect of the seed layer on the properties of the final Cu

- Electroplating needs a seed layer of Cu as it does not occur at a dielectric surface.
- Properties of the final Cu layer critically depend upon the characteristics of the seed layer.
- The deposition of the seed layer can be done by PVD, CVD or ALD.
- Currently PVD is preferred, CVD and ALD being investigated.
Plated Copper Fill Evolution

Ref: Jonathan Reid, ITC, 1999

Trench Filling Capability of Cu Electroplating

Ref: Jonathan Reid, ITC, 1999
Grain Size Distribution

Electroplated Cu gives bigger grain size


Electromigration: CVD vs. Electroplating

Electroplated Cu has higher resistance to electromigration because of its grain structure


Stanford University
EE311/ Saraswat/ Cu Interconnect

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**Film Microstructure vs. EM Time-to-Failure**

- **Empirical relationship (for Al & Al alloys)**

$$MTF \propto \frac{e^{\mu t}}{\sigma^2 \log \left( \frac{I_{(111)}}{I_{(200)}} \right)^3}$$

S. Vaidya et al.,

- **EM dependence on the microstructure of Cu films**

![Graph showing EM dependence on microstructure](image)

Ref: Ryu, Loke, Nogami and Wong,

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**Self-annealing at Room Temperature**

- Grains are initially small in all films but recrystallization increases their size

**Thin Film Cu Resistivity**

- Effect of Electron Scattering
  - Reduced mobility as dimensions decrease
    - Grain boundary scattering
    - Surface scattering
  - Reduced mobility as chip temperature increases
    - Increased phonon scattering

**Cu Resistivity: Effect of Line Width Scaling**

**Surface Scattering**

Fuchs-Sondheimer model

\[ \rho_{\text{surf}} = \rho(w, R, \lambda) \]

- \( h, w \): conductor height and width
- \( p \): specularity parameter
- \( \lambda \): electron mean free path

**Grain Boundary Scattering**

Mayadas-Shatzkes model

\[ \rho_{\text{g.b.}} = \rho(d, \lambda) \]

- \( d \): ave. grain boundary distance
- \( R \): Reflection coefficient at g.b.
- \( \lambda \): electron mean free path

Resistivity increases as grain size decreases due to increase in density of grain boundaries which act as carrier scattering sites.

- Resistivity increases as main conductor size decreases due to increased surface scattering.

\[ \text{Resistivity, } \mu \Omega \text{ cm} \]

\[ \text{Line Width, nm} \]


**Thin Film Cu Resistivity**

- Effect of Cu diffusion Barrier
  - Barriers have higher resistivity
  - Barriers can't be scaled below a minimum thickness
  - Consumes larger area as dimensions decrease
- Resistivity of the composite wire is increased

> Resistivity of metal wires could be much higher than bulk value
**Cu Resistivity: Theoretical Background**

**Barrier Effect**

\[ \frac{\rho_b}{\rho_o} = \frac{1}{1 - \frac{A_b}{AR \cdot w^2}} \]

- Important parameter: \( A_b \) to \( A_{\text{int}} \) ratio
- \( \rho_b \) increase with \( A_b \) to \( A_{\text{int}} \) ratio
- Future: ratio may increase

**Electron Surface Scattering Effect**

\[ \frac{\rho_s}{\rho_o} = \frac{1}{1 - \frac{3(1 - P)\lambda_{\text{in}}}{2d} \left[ \frac{1}{X^3} - \frac{1}{X} \right] e^{-\frac{d}{\lambda_{\text{mfp}}}} \right] } \]

- Reduced electron mobility
- Operational temperature
- Copper/barrier interface quality
- Dimensions decrease in tiers: local, semiglobal, global


**Cu Resistivity: Effect of Barrier**

- Barriers can’t be scaled and have high resistivity
- Surface electron scattering increases resistivity
- Real chips operate at higher temperatures

Kapur and Saraswat, IEEE TED, April 2002
Semi-global & Local Interconnects

- With ALD least resistivity rise
- Al resistivity rises slower than Cu. Cross over with Cu resistivity possible
  - no 4 sided barrier
  - smaller $\lambda_{\text{mfp}}$ ⇒ smaller $k$

Cu Resistivity: Effect of Chip Temperature

- Higher temperature ⇒ lower mobility ⇒ higher resistivity
- Realistic Values at 35 nm node: P=0.5, temp=100 °C
  - local ~ 5 $\mu$Ω-cm
  - semi-global ~ 4.2 $\mu$Ω-cm
  - global ~ 3.2 $\mu$Ω-cm
Summary

• Interconnect scaling issues
• Thermal issues
• Electromigration
• Aluminum technology
• Copper technology