Solution to EE 311 Midterm Exam, Spring 1995

1. A logic circuit containing 100 gates is fabricated in a 1μm CMOS technology. If the interconnections are made of superconductors will it improve the speed of the circuit?

This is a small circuit with relatively short interconnections, and the transistor is not too fast. Hence the transistor delay will be appreciably longer than the interconnect RC delay. Using superconductors will not enhance the performance.

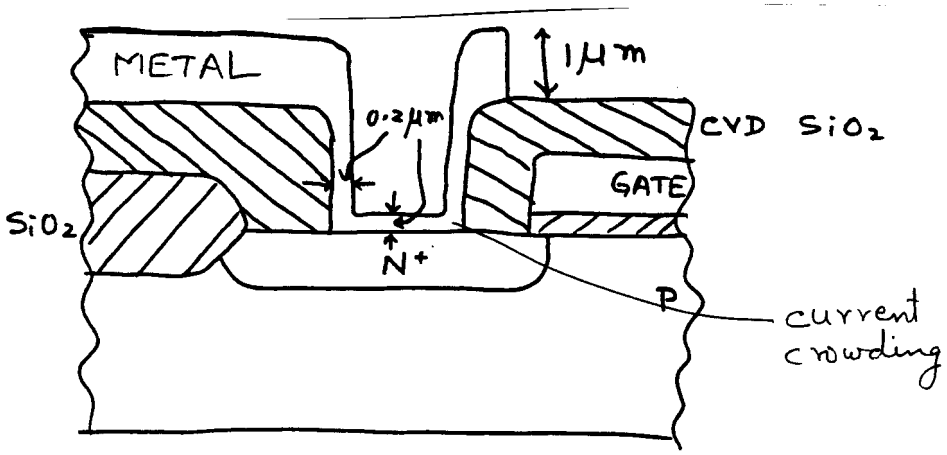
2. As the device dimensions are scaled and chip size increases the time delay due to interconnections influences the circuit speed. The width of an interconnect has to be scaled with the same factor as the device to increase the packing density and decrease interconnect length. Do we have to scale the thickness, knowing that scaling the thickness causes problems for electromigration and line resistance?

The thickness of the interconnects will have to be scaled due to the following reasons:

(a) To reduce the interline capacitance, otherwise the RC delay and crosstalk will cause problems.

(b) If not scaled the gaps with high aspect ratio will cause technological problems, such as, step coverage.

3. In an MOS transistor a new metal is used to make both interconnections and contacts to source-drain junctions with sheet resistance of 500 Ω/sq. and specific contact resistivity of 5×10^{-8} Ωcm^2. As shown in the figure below the thickness of the metal on the top flat surface is 1 μm whereas on the sidewall and bottom of the contact it is only 0.2μm. Where do you expect the electromigration failure to occur? By increasing the metal thickness on the sidewall and bottom to 0.5μm will the electromigration lifetime improve?



Transfer length of the contact $l_t = \sqrt{\frac{\rho_c}{R_s}} = \sqrt{\frac{5\times10^{-8}}{500}}$ cm = 1000 Å

Hence most of the current will be crowed at the right-bottom corner. Electro migration will thus take place at this corner. Since the transfer length is only 1000 Å, increasing the Al thickness won't help. (In real life this will not really happen because real ρ_c values are about a factor of 10 higher and hence l_t is also higher.)

4(a). ϕ_{BN} for Pt Si is about 0.85 eV whereas for Al is 0.65. Why in practice the contact resistance of N^+ Si to Al is higher than to PtSi?

Pt can diffuse through native oxide on Si more effectively than Al, which forms Al_2O_3 by reducing SiO_2. Hence Pt Si has a much cleaner interface giving lower contact resistance.