MOS Gate Dielectrics

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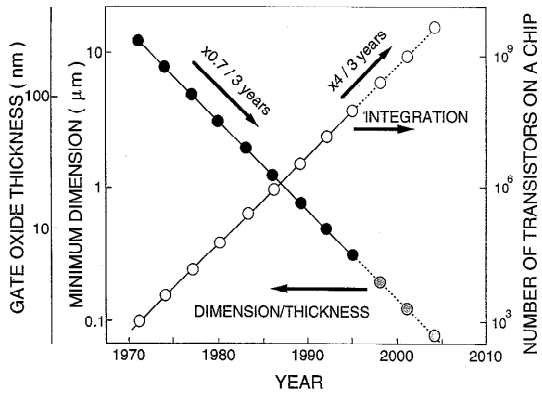
Outline

- Scaling issues
- Technology
- Reliability of SiO_2
- Nitrided SiO_2
- High k dielectrics

Scaling of MOS Gate Dielectric



$I_D \propto$ *Charge x velocity*
$\propto C_{ox}(V_{GS} - V_T)$ *x velocity*
$\propto C_{ox}(V_{GS} - V_T)$ *x velocity*

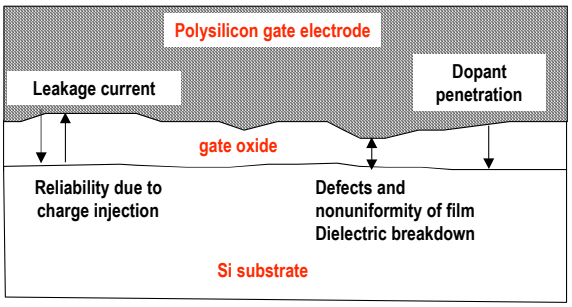
$$C_{ox} \propto \frac{K}{thickness}$$

(Ref: S. Asai, Microelectronics Engg., Sept. 1996)

Gate SiO_2 thickness is approaching < 20 Å to improve device performance

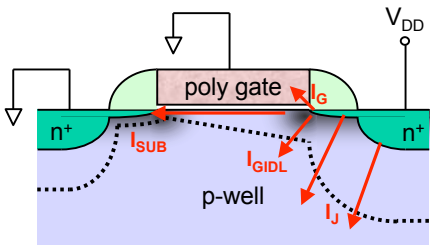
- **How far can we push MOS gate dielectric thickness?**
- **How will we grow such a thin layer uniformly?**
- **How long will such a thin dielectric live under electrical stress?**
- **How can we improve the endurance of the dielectric?**

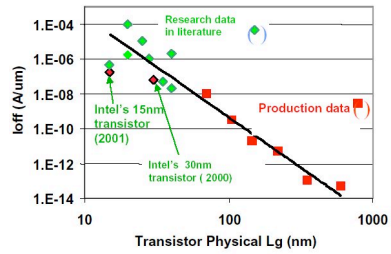
Problems in Scaling of Gate Oxide



- Below 20 Å problems with SiO_2
  - Gate leakage => circuit instability, power dissipation
  - Performance degradation due to t_{ox}(electrical) > t_{ox}(physical)
    - Carrier quantization in the channel and depletion in poly-Si gate
  - Degradation and breakdown
  - Dopant penetration through gate oxide
  - Defects

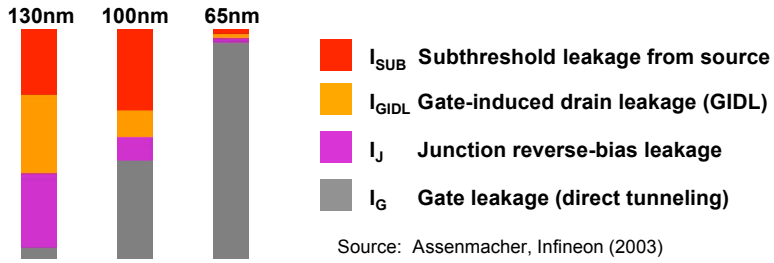
Leakage Current Contributions





Source: Marcyk, Intel

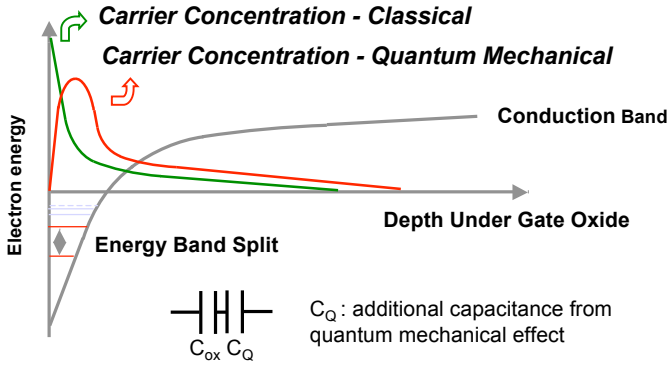
Relative contributions of OFF-state leakage (but magnitude of total leakage getting exponentially worse for deeper submicron nodes)



Source: Assenmacher, Infineon (2003)

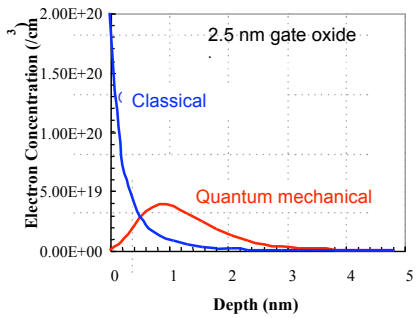
Quantum Mechanical Effect under gate oxide

- Band bending under gate oxide creates a quantum well that splits carrier energy band into subbands
- The spatial distribution of carriers is modified with the maxima in the semiconductor
- This results in additional capacitance

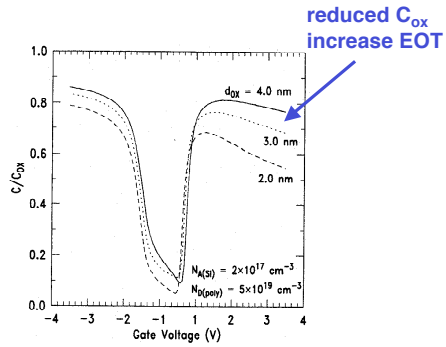


C_Q : additional capacitance from quantum mechanical effect

Performance degradation due to t_{ox}(electrical) > t_{ox}(physical)



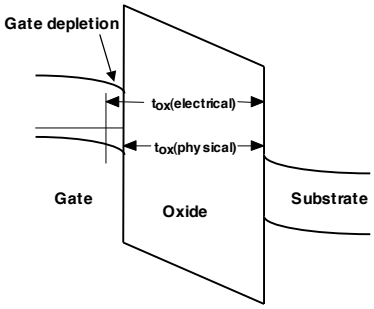
Ref: T.-Y. Oh PhD thsis, Stanford Univ. 2004

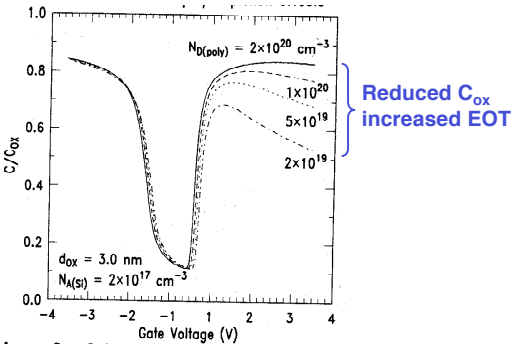


Ref: Buchanan et al., Proc. ECS Vol. PV 96-1, 1996

- The maximum of carrier concentration is located ~ 1nm under the gate oxide
- Corresponds > 20% of physical gate oxide thickness of current technology
- Effect of quantization is to increase effective t_{ox} and thus reduce C_{ox}

Carrier depletion in poly-Si gate.





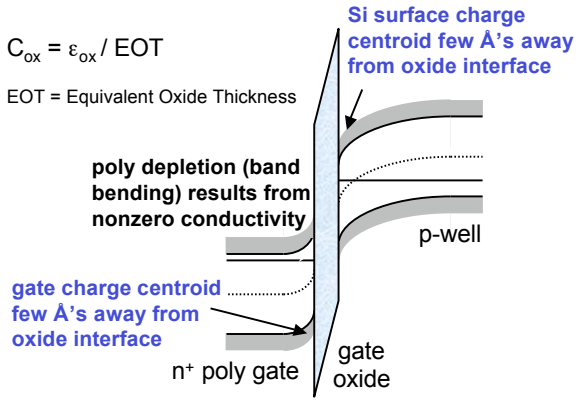
(Buchanan and Lo, Proc. ECS Vol. PV 96-1, 1996)

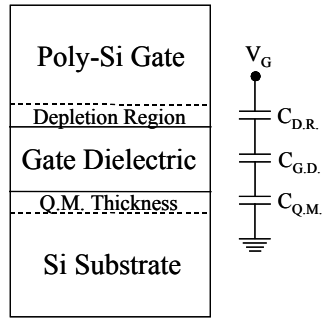
- High E - field due to a combination of higher supply voltage and thinner gate oxide causes band bending even in heavily doped poly-Si gate
- This causes depletion in poly-Si gate, especially for boron doping
- Effect of depletion is to increase effective t_{ox} and thus reduce C_{ox}

Combined Effects of Depletion and Quantization

$C_{ox} = \varepsilon_{ox} / EOT$

EOT = Equivalent Oxide Thickness





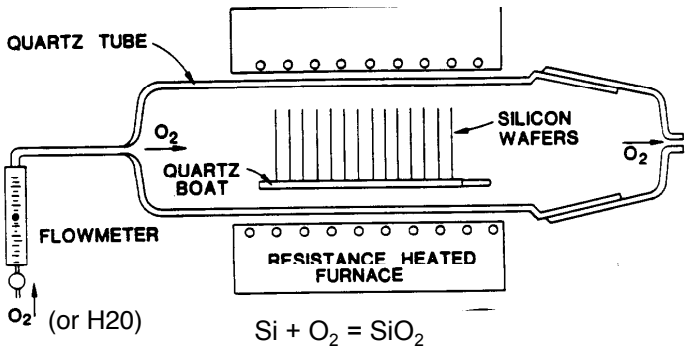
$EOT_{TOT} = EOT_{D.R.} + EOT_{G.D.} + EOT_{Q.M.}$

- Combined effect of depletion and quantization is to increase effective t_{ox} and thus reduce C_{ox}
- A reduced C_{ox} implies reduction in g_m and thus I_D(on)

Outline

- Scaling issues
- Technology
- Reliability of SiO_2
- Nitrided SiO_2
- High k dielectrics

Resistance Heated Furnace

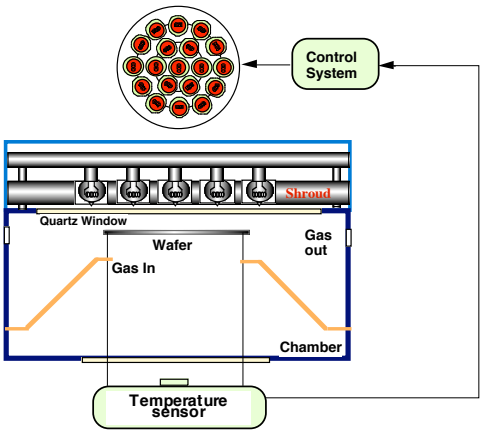


$$Si + O_2 = SiO_2$$

$$Si + 2H_2O = SiO_2 + 2H_2$$

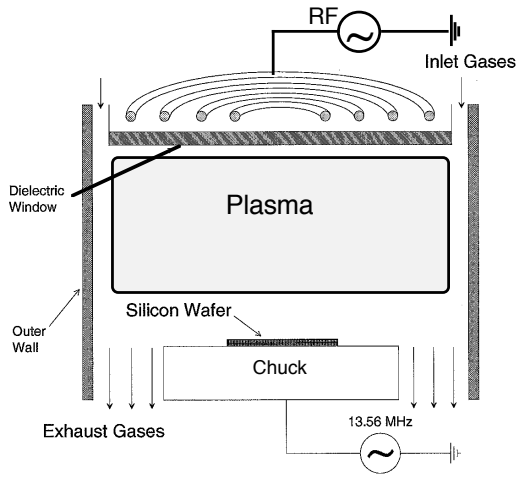
- Batch processing ⇒ low cost
- High thermal mass ⇒ long process times.
- Ideal for growing thick oxides.
- Multiprocessing for nitrided oxides not easy to do.

Lamp Heated Rapid Thermal Oxidation



- Single wafer processing ⇒ real time measurement and control
- Low thermal mass ⇒ short process times.
- Ideal for growing ultrathin gate oxides.
- Multiprocessing ideal for composite dielectrics, e.g., nitrided oxides.
- Rapid thermal CVD of ultrathin Si_3N_4

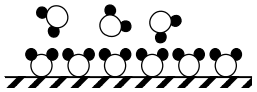
Plasma CVD System



Primarily used in low temperature applications, e.g., TFTs for displays

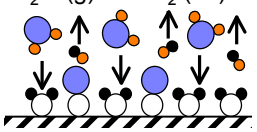
Atomic layer CVD (ALCVD)

1) $ZrCl_4(g)$

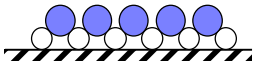


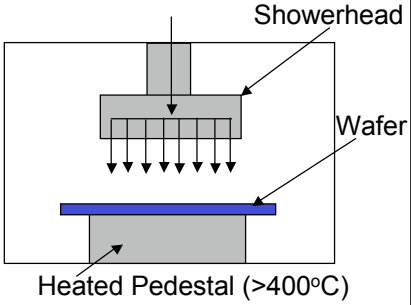
2) $ZrCl_4(ad)$

3) $ZrCl_4(ad) + 2H_2O\ (g) \rightarrow ZrO_2\ (ad) + 4HCl\ (g)$



4) $ZrO_2(ad)$

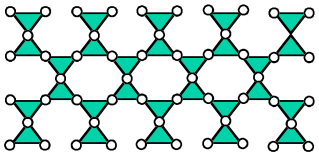




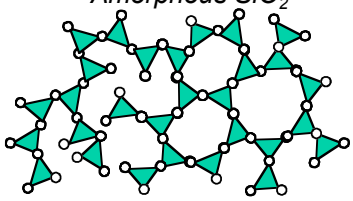
- **Deposition is done one monolayer at a time: excellent control**
- **Being investigated for high-k dielectrics like ZrO_2, HfO_2**

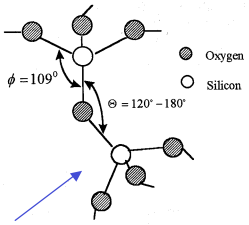
Microstructure of SiO_2

Crystalline quartz



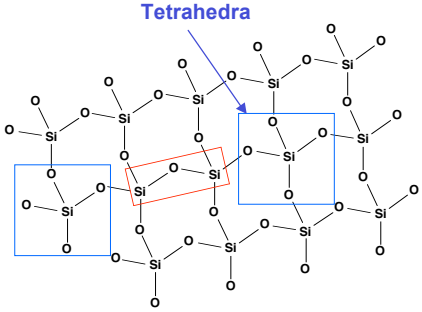
Amorphous SiO_2





Tetrahedra

Crystalline SiO_2 consists of ordered networks of corner-sharing SiO_4 tetrahedra In the amorphous SiO_2, the basic structural unit is the SiO_4 tetrahedron with each Si atom surrounded by four O atoms. The angle of O-Si-O bonds is fixed at 109.5º. However, the Si-O-Si angle is rather flexible. Each O atom bridges two neighboring SiO_4 tetrahedrons. The bond is relatively easy to bend, stretch or rotate. The Si-O-Si bonds are capable of accommodating large lattice distortion



MOS Gate Dielectrics

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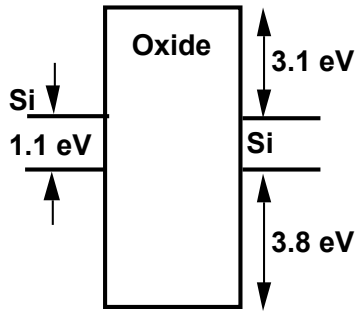
Ideal MOS

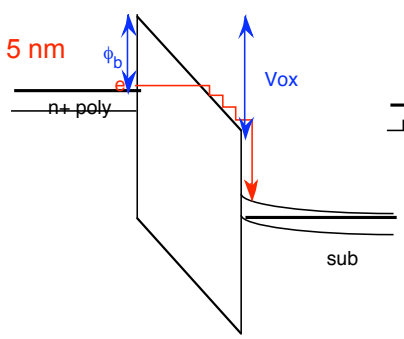


- The microstructure gives rise to a band structure with a large band gap of about 9 eV
- Large barriers between Si and SiO_2

Conduction in Dielectrics: Tunneling

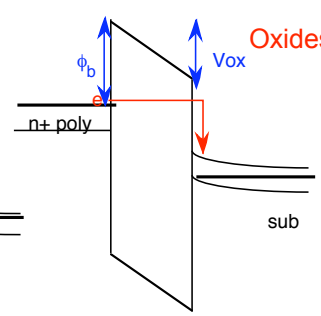
Fowler-Nordheim Tunneling

Oxides > 5 nm



Direct Tunneling

Oxides < 3 nm



$$J = AE_{ox}^2 e^{-\frac{B}{E_{ox}}}$$

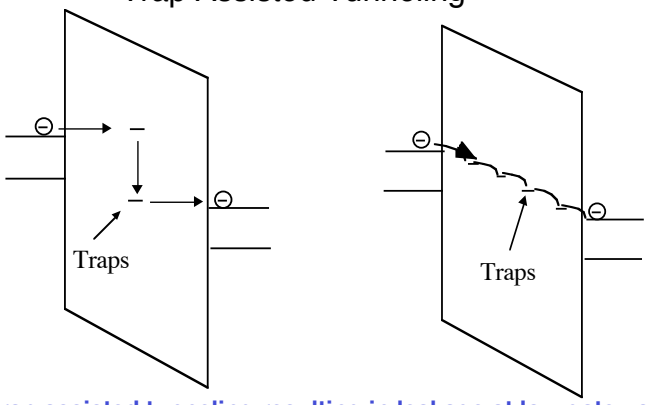
$$J = AE_{ox}^2 \exp \frac{-B\left\{1-(1-\frac{V_{ox}}{\phi_b})^{3/2}\right\}}{E_{ox}}$$

$$A = \frac{q^3 m}{8\pi\hbar m_{ox}\phi_b} \qquad B = \frac{8\pi\sqrt{2m_{ox}}\phi_b^{3/2}}{3hq}$$

m is the mass of electron in vacuum
m_{ox} is the average electron mass in the oxide

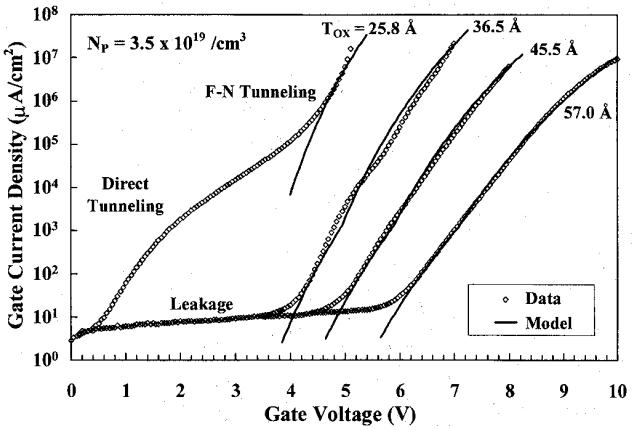
Conduction in Dielectrics: Leakage

Trap Assisted Tunneling



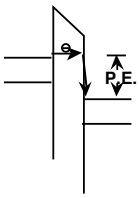
- Trap assisted tunneling resulting in leakage at low gate voltage
- An increase in traps will cause more leakage
- Traps are present in as grown dielectric
- Traps can be generated by electrical stress

Conduction in Thin Oxides

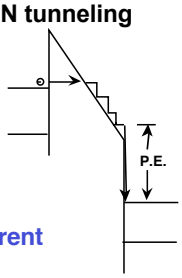


Ref: Gupta, et al., IEEE Electron Dev. Lett. Dec. 1997

THIN OXIDE
Direct tunneling

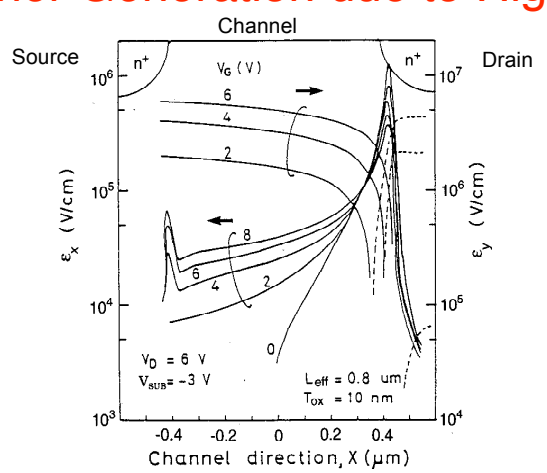


THICK OXIDE
FN tunneling



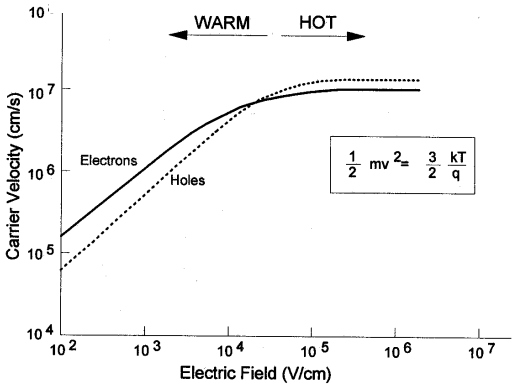
Below ~35 Å direct tunneling causes excessive gate current

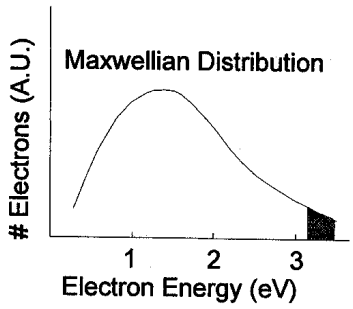
Hot Carrier Generation due to High E-field



- The E-field can be very high in the channel, especially near the drain
- The free carriers passing through the high-field can gain sufficient energy

Hot Electrons and Holes

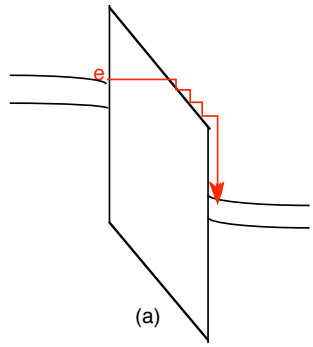




- At high electric fields the carriers are accelerated to high velocities
- These energetic carriers are termed as hot carriers

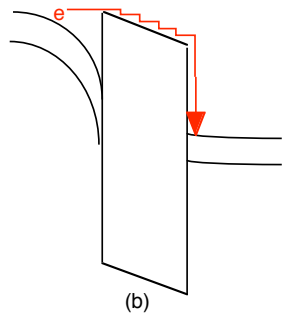
Hot electron injection

Fowler-Nordheim Tunneling



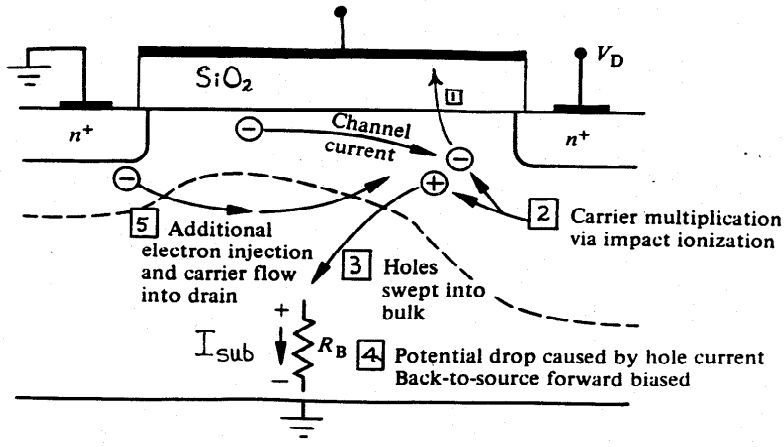
- Requires sufficient band bending for electrons to tunnel into the conduction band of the oxide

Hot electron injection



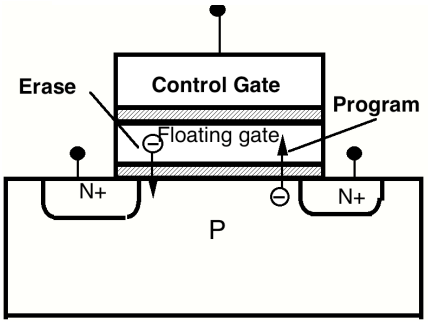
- Electrons being injected have to be highly energetic to overcome the barrier
- Hot electrons can be produced in drain depletion region
- Hot holes behave similarly

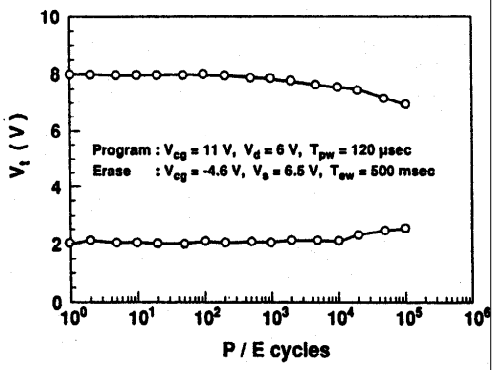
Hot carrier effects in an MOS transistor



- **The free carriers passing through the high-field can gain sufficient energy to cause several *hot-carrier* effects.**
- **This can cause many serious problems for the device operation, e.g. change in V_t, g_m, leakage, junction breakdown**

Non Volatile Memories

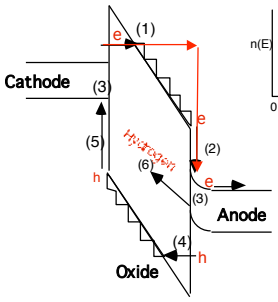


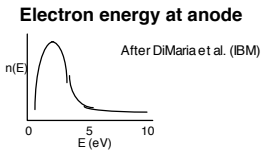


- Carrier injection is also used beneficially for making non volatile memories
- V_t shift due to carrier trapping during program and erase functions

Dielectric Degradation Mechanisms

- Degradation during device operation due to high E field causing current injection
- Degradation during fabrication due to charging in plasma processing

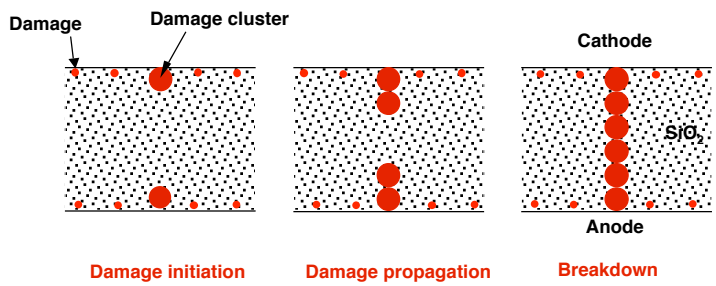




(1) Electron injection
(2) Energy released by hot electron
(3) Bond breaking - trap generation
(4) Hot hole generation
(5) Energy released by hot hole - trap generation
(6) Hydrogen release - trap generation

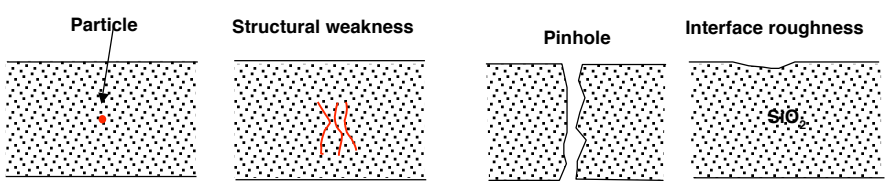
Dielectric damage and breakdown is due to interface trap generation initiated by the energy loss of injected electrons and holes

Intrinsic Dielectric Breakdown



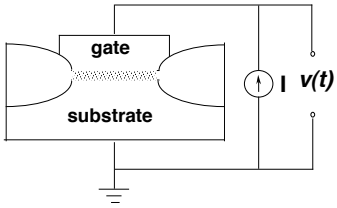
- Damage initiates at anode and cathode interfaces causing degradation.
- Eventually it spreads throughout the body of the dielectric causing breakdown.
- Degradation can be minimized if damage at the interfaces is prevented

Extrinsic Breakdown



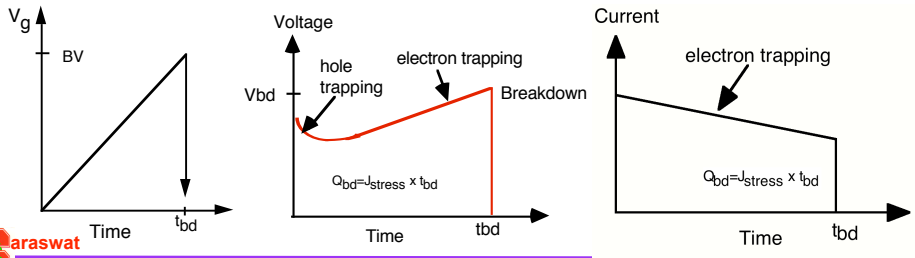
- Damage initiates at an extrinsic defect present in the oxide
- Eventually it spreads throughout the body of the dielectric causing breakdown.
- Degradation is minimized by careful processing to reduce process induced defects

Methods of testing degradation and breakdown in dielectric films

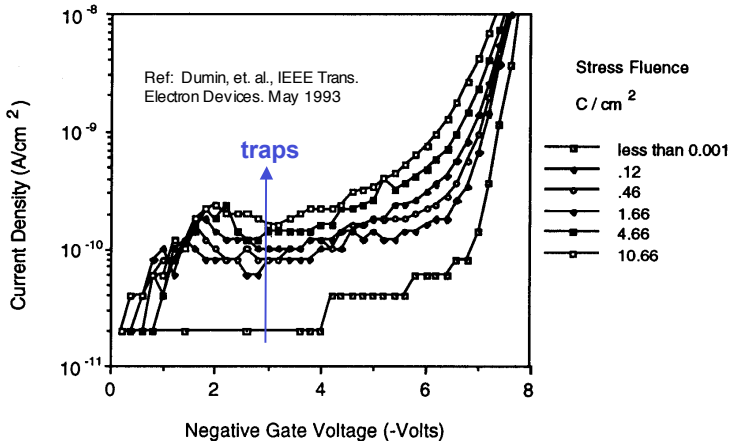


A voltage (or current) stress is applied to a capacitor. The current (or voltage) is monitored till the device breaksdown. Time to breakdown (t_{bd}) and total injected charge to breakdown (Q_{bd}) are then determined

Ramped voltage stress | Constant current stress | Constant voltage stress

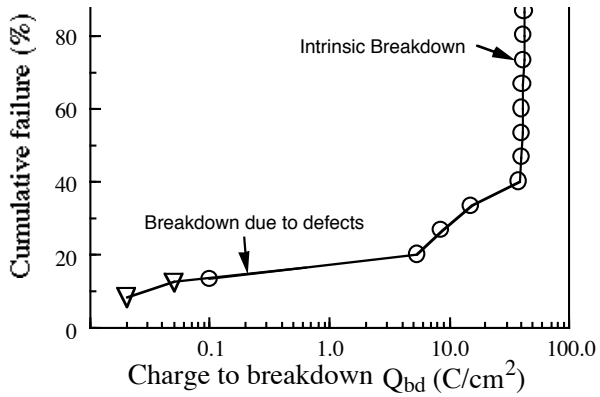


Stress Induced leakage Current



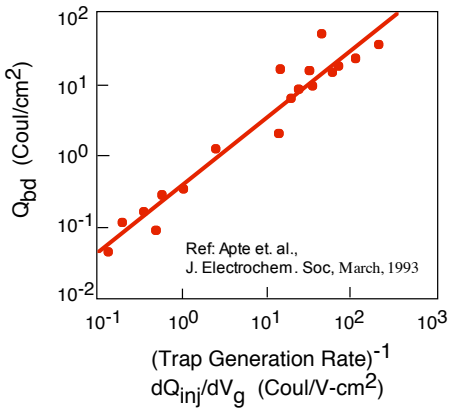
- Electrical stress in SiO_2 causes leakage to increase at low gate voltages
- Electrical stress generates traps
- Leakage is caused by traps assisted tunneling

Breakdown Statistics



- Intrinsic breakdown has higher Q_{bd}
- Extrinsic breakdown results in early breakdown
- A good set of devices should not have early breakdown

Q_{bd} vs. Trap Generation Rate≈



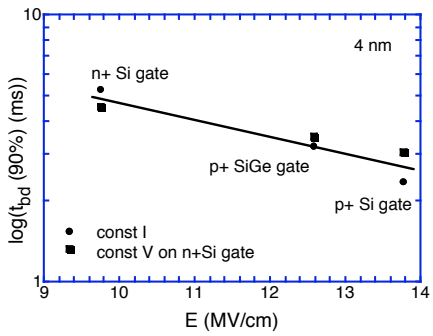
T_{ox} = 30 - 250 Å

T = 20 - 300°C

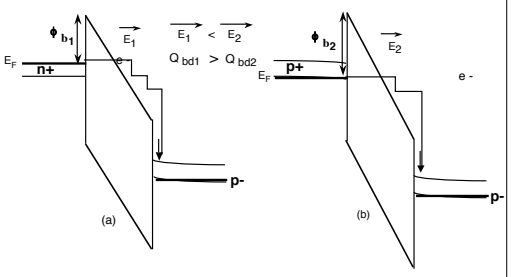
$J_{ox} = 10^{-2}$ - 1 A/cm^2

- Q_{bd} and net trap generation track for different oxide thickness, stress current density and temperature
- Higher trap generation rate causes lower Q_{bd}
- Dielectric damage and breakdown is due to interface trap generation initiated by the energy loss of injected electrons and holes

Dependence of t_{bd} on Electric Field



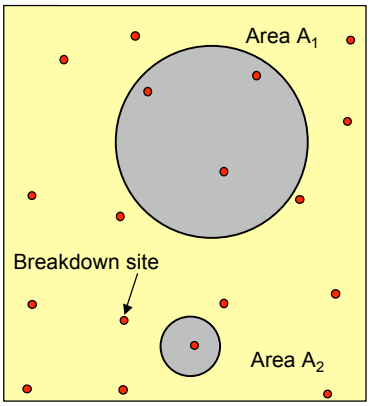
Ref: Yang, et. al., IEEE Trans. Electron Dev., July 1999

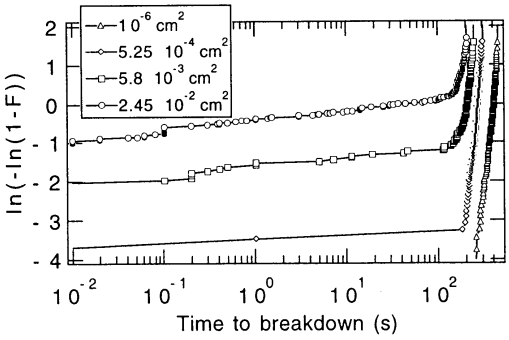


Energy diagrams for (a) n+ poly-Si and (b) p+ poly-Si gate MOS capacitor on p- substrates. Barrier height is 3.1 eV for n+ gate and 4 eV for p+ gate. Higher barrier height gives larger oxide electric field and therefore lower Q_{bd} at a fixed current density.

Higher E field in gate oxide ⇒ higher electron energy at the anode
⇒ lower T_{bd}

Effect of Area on t_{BD}

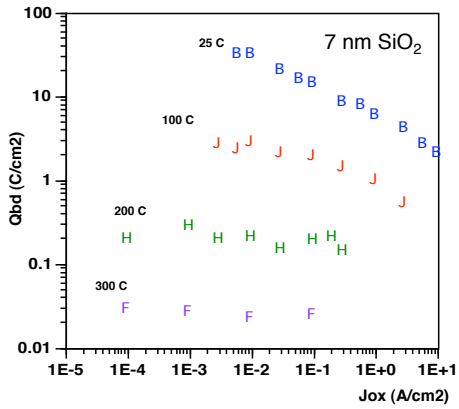




Ref: Degreve, IRPS 1997

- **Device with larger area has higher probability of containing a breakdown site ⇒ Larger area devices have lower t_{BD}**
- **Measurements made on larger area capacitors need to be correlated to smaller area transistors**

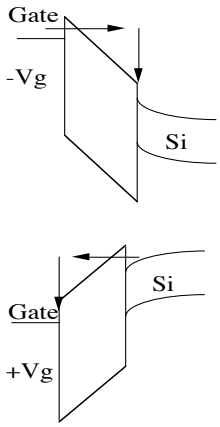
Effect of Electrical Stress Temperature on Q_{bd}

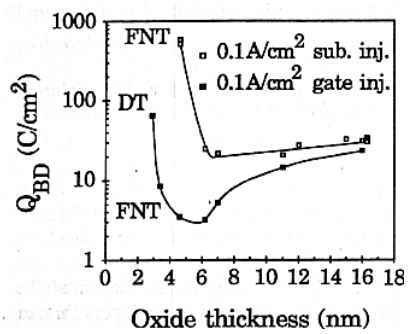


- **Higher stress temperature results in lower Q_{bd}**
- **Important for plasma induced damage**

Ref: Apte et. al., J. Electrochem. Soc, March, 1993

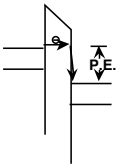
Substrate vs. Gate Injection



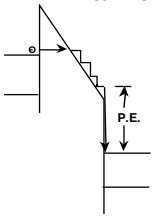


Ref: M. Depas et al., Electrochem Soc., Vol. PV96-1, p. 352, 1996

THIN OXIDE: Direct tunneling

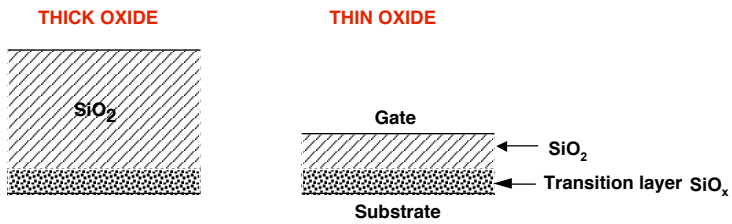


THICK OXIDE: FN tunneling



- Q_{bd} is lower for gate injection of electrons ⇒ Effect of the strained transition layer
- As gate oxide thickness decreases Q_{bd} is not affected much for substrate injection but decreases for gate injection ⇒ Effect of the strained transition layer
- For ultrathin oxide direct tunneling dominates resulting in lower energy electrons in the SiO_2. Thus damage is reduced and Q_{bd} increases.

Transition (Strained) Layer at the Substrate Interface



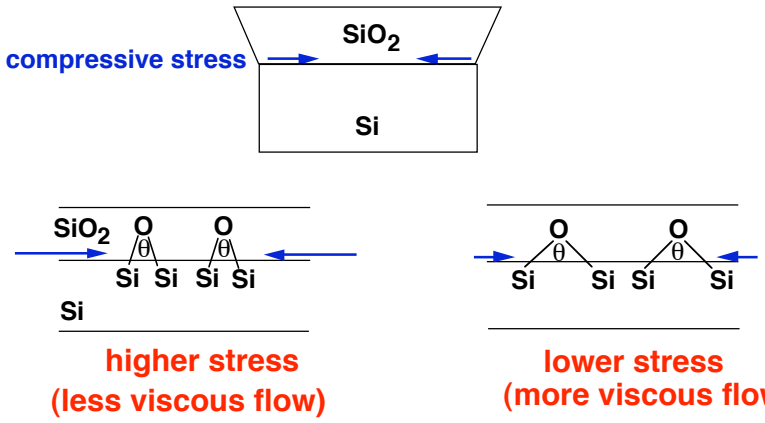
Transition Layer

- Structural inhomogenity (1-2 monolayers) due to transition from Si to SiO_2
- Stress due to volume change during SiO_2 formation.
- Strained bonds are easier to break resulting in lower Q_{bd} for gate injection of electrons.
- For thinner films the transition layer becomes a significant fraction of the total layer.

For increased reliability of deep submicron devices, technology must be developed to reduce the impact of the transition layer

Why is there a stress?

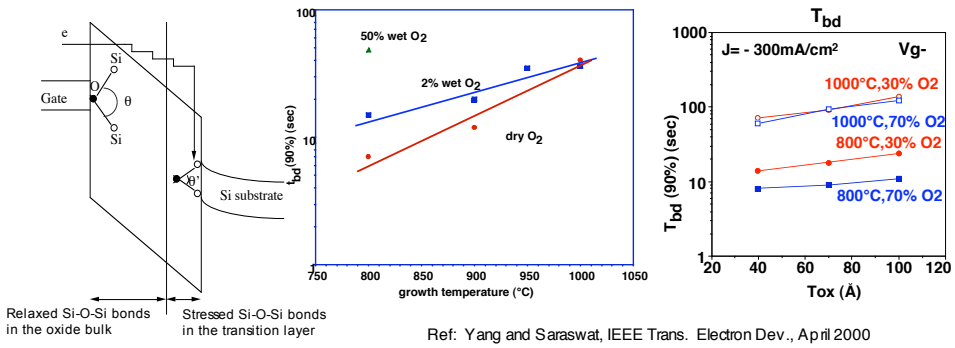
During thermal oxidation,
+126% volume increase from Si --> SiO2



higher stress
(less viscous flow)

lower stress
(more viscous flow)

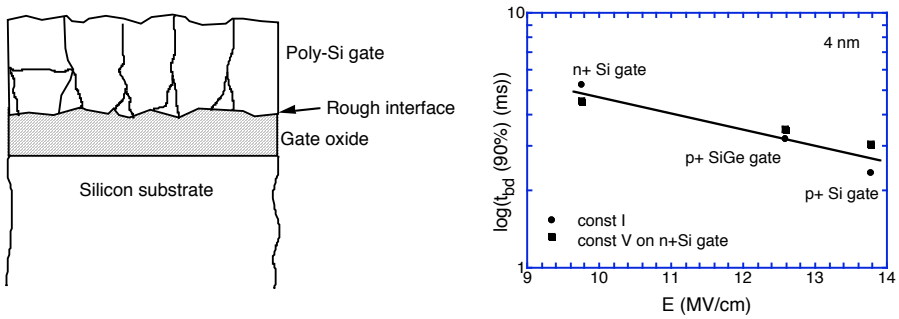
Correlation Between Stress and Q_{bd}



Ref: Yang and Saraswat, IEEE Trans. Electron Dev., April 2000

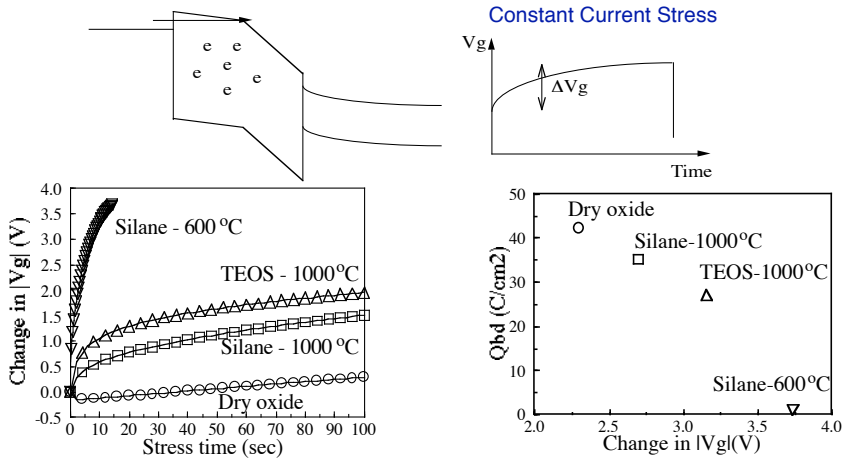
- **Thinner SiO_2 films are more susceptible to degradation (for FN tunneling)**
- **Degradation is always more for conditions resulting in higher physical stress in SiO_2.**
- **Higher temperatures, steam oxidation and longer growth times allow stress relaxation through viscous flow and hence result in SiO_2 of better reliability.**

Effect of Gate Electrode



- Gate electrode roughness at the oxide/gate interface causing enhanced localized electric field intensity.
- Gate electrode workfunction impacts electric field intensity
- Higher electric field intensity results in lower reliability

Effect of Bulk Electron Trapping



Ref: Bhat, et. al., IEEE Trans. Electron Devices., April 1996

- Degradation by bulk electron trap generation is observed in deposited oxides used as gate dielectrics in applications such as non volatile memories and TFTs for flat panel displays
- It can be minimized by a high temperature anneal

MOS Gate Dielectrics

Outline

- **Scaling issues**
- **Technology**
- **Reliability of SiO_2**
- **Nitrided SiO_2**
- **High k dielectrics**