MOS Gate Dielectrics

Outline

• Scaling issues
• Technology
• Reliability of SiO₂
  • Nitrided SiO₂
  • High k dielectrics

Incorporation of N or F at the Si/SiO₂ Interface

Incorporating nitrogen or fluorine instead of hydrogen strengthens the Si/SiO₂ interface and increases the gate dielectric lifetime because Si-F and Si-N bonds are stronger than Si-H bonds.

Nitrooxides
  – Nitridation of SiO₂ by NH₃, N₂O, NO
  – Growth in N₂O
  – Improvement in reliability
  – Barrier to dopant penetration from poly-Si gate
  – Marginal increase in K
  – Used extensively

Fluorination
  – Fluorination of SiO₂ by F ion implantation
  – Improvement in reliability
  – Increases B penetration from P⁺ poly-Si gate
  – Reduces K
  – Not used intentionally
  – Can occur during processing (WF₆, BF₃)
Nitridation of SiO$_2$ in NH$_3$

- Oxidation in O$_2$ to grow SiO$_2$.
- RTP anneal in NH$_3$ maximize N at the interface and minimize bulk incorporation.
- Reoxidation in O$_2$ remove excess nitrogen from the outer surface.
- Anneal in Ar remove excess hydrogen from the bulk.
- Process too complex.

Nitridation in N$_2$O or NO

- The problem of H can be circumvented by replacing NH$_3$ by N$_2$O or NO.

Profile of N in SiO$_2$

Stress-time dependence of $g_{m}$ degradation of a NMOS.
Oxidation of Si in N\textsubscript{2}O

\[
\begin{align*}
N_2O \rightarrow N_2 + O \\
N_2O + O \rightarrow 2NO
\end{align*}
\]

- RTP oxidation shows N accumulation near the Si/SiO\textsubscript{2} interface
- Furnace oxidation shows almost uniform N profile \(\Rightarrow\) lower \(Q_{bd}\)


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Dopant Penetration From Poly-Si Gate

- Incorporation of nitrogen at the interface suppresses dopant diffusion from gate poly-Si into the channel which can cause \(V_T\) shift.
- The problem is more serious for P\textsuperscript{+} poly-Si as boron diffuses more readily in SiO\textsubscript{2}.
- It is desirable to use P\textsuperscript{+} gate for PMOS transistors, for scaled CMOS technology to minimize short channel effects.
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High-k MOS Gate Dielectrics

$I_{\text{channel}} \propto \text{charge} \times \text{source injection velocity} \propto (\text{gate oxide cap} \times \text{gate overdrive}) \times v_{\text{inj}}$

$\propto C_{\text{ox}} (V_{\text{GS}} - V_{\text{T}}) \times E_{\text{source}} \times \mu_{\text{inj}}$

Historically $C_{\text{ox}}$ has been increased by decreasing gate oxide thickness. It can also be increased by using a higher K dielectric

$I_D \propto C_{\text{ox}} \propto \frac{K}{\text{thickness}}$

$20 \text{ Å SiO}_2 \ K \approx 4$
$40 \text{ Å Si}_3\text{N}_4 \ K \approx 8$

Higher thickness $\rightarrow$ reduced gate leakage

$J_{DT} \propto e^{-t_{\text{ox}}}$
Benefits of High-κ Gate Dielectrics

$$C_{ox} = \frac{\kappa \varepsilon_0 A}{t_{ox}} \Rightarrow t_{\text{high-κ}} = \left( \frac{\kappa_{\text{high-κ}}}{\kappa_{\text{SiO}_2}} \right) \cdot t_{\text{SiO}_2}$$

Historically $C_{ox}$ has been increased by decreasing gate oxide thickness. It can also be increased by using a higher K dielectric.

Alternatives to SiO$_2$: Silicon Nitride

- A factor of 2 increase in K
- Reduction in bandgap → increased gate leakage

Nitridation of Silicon

• Si reacts with NH₃ to grow Si₃N₄
  – Excellent gate dielectric properties
  – Reaction needs very high temperatures

• Si reacts with atomic nitrogen
  – Reaction temperature could be reduced using nitrogen plasma
  – More research needed

• Several deposition methods under investigations, e.g., rapid thermal CVD, jet vapor deposition (JVD)


Nitride / Nitrooxide Sandwich Gate MOS

• 1.2 nm EOT (Equivalent oxide thickness) gate dielectric can be formed by
  - thermally growing ultrathin oxinitride
  - CVD of Si₃N₄

• Low gate leakage
• 40 nm channel length CMOS demonstrated

(Ref: M. Bohr, Intel, IEDM 2002.)
Requirements for the MOS gate dielectrics

- High dielectric constant $\Rightarrow$ higher charge induced in the channel
- Wide band gap $\Rightarrow$ higher barriers $\Rightarrow$ lower leakage
- Ability to grow high purity films on Si with a clean interface.
  - High resistivity and breakdown voltage.
  - Low bulk and interfacial trap densities.
- Compatibility with the substrate and top electrode.
  - Minimal interdiffusion and reaction
  - Minimal silicon reoxidation during growth and device processing
    - Even a thin SiO$_2$ layer would deteriorate the $C_{\text{gate}}$ significantly.
- Thermal stresses — most oxides have larger thermal expansion coefficients than Si.
- Good Si fabrication processing compatibility.
  - Stability at higher processing temperatures and environments
  - Ability to be cleaned, etched, etc.

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>Permittivity</th>
<th>Band Gap (eV)</th>
<th>$\Delta E_C$ to Si</th>
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<tr>
<td>SiO$_2$</td>
<td>3.9</td>
<td>9</td>
<td>3.5</td>
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<td>Si$_3$N$_4$</td>
<td>7</td>
<td>5.3</td>
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<td>6</td>
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<tr>
<td>HfSiO$_4$</td>
<td>15</td>
<td>6</td>
<td>-</td>
</tr>
</tbody>
</table>


- Higher K materials have lower bandgap
- There are many performance, reliability and process integration issues yet to be solved
- More research is needed to make these materials manufacturable
Thermodynamic Stability of High-K Dielectric Oxides

- Unstable oxides (e.g. TiO$_2$, Ta$_2$O$_5$, BST)
  - React with Si to form SiO$_2$ and silicides upon thermal annealing
  - Barrier (e.g. Si$_x$N$_y$) is required to prevent such a reaction
    - A monolayer of nitride on both sides of gate dielectric already contributes 5 Å to the physical oxide thickness
- Stable oxides (e.g. HfO$_2$, ZrO$_2$, Al$_2$O$_3$) and their silicates (e.g. ZrSi$_x$O$_y$) and aluminates (e.g. ZrAl$_x$O$_y$)
  - Do not react with Si upon thermal annealing (up to 1000°C)
  - May not require a barrier layer between Si and the metal oxide
- Simple structure: poly-Si/stable oxide/Si substrate

Stability of Metal Oxides with Si

After Beyers, J. Appl. Phys. 56, 157, 1984
And Wang and Meyer J. Appl. Phys. 64, 4711, 1988

- ZrO$_2$/Zr-Si-O stable on Si; Ta and Ti oxide/silicate not stable
- Zr, Hf Silicates: no interfacial layer required
Capacitance and Leakage for High-k Gate Dielectric Films Grown Using ALCVD

Perkins, Saraswat and McIntyre, Stanford Univ. 2002

Chui, Kim, Saraswat and McIntyre, Stanford Univ. 2004

Atomic Layer CVD of Hi-κ Dielectric

McIntyre, Saraswat, Stanford

Perkins, Saraswat and McIntyre, Stanford Univ. 2002

Chui, Kim, Saraswat and McIntyre, Stanford Univ. 2004


**Atomic Layer Deposition**

\[
\text{Zr} - \text{OH}^+ + \text{ZrCl}_4 \rightarrow \text{Zr} - \text{O} - \text{ZrCl}_3 + \text{HCl} \uparrow
\]

Saturated adsorption

Substrate

**1/4 cycle**: Injection of reactant A (ZrCl\(_4\)/HfCl\(_4\))

**2/4 cycle**: Purging (N\(_2\))
Atomic Layer Deposition

Reactant A
(ZrCl$_4$/HfCl$_4$)

Reactant B
(H$_2$O)

1 cycle

3/4 cycle:
Injection of reactant B (H$_2$O)

4/4 cycle:
Purging (N$_2$)

Zr – Cl$^-$ + H$_2$O $\rightarrow$ Zr – OH$^-$ + HCl $\uparrow$

Substrate

ZrO$_2$/HfO$_2$ (s)
Atomic Layer Deposition

- Surface saturation controlled process
- Layer-by-layer deposition process
- Excellent film quality and step coverage

Microstructure of ALD HfO₂ and HfO₂

As-deposited ALD-ZrO₂ is polycrystalline.

As-deposited ALD-HfO₂ is amorphous.

- There is always a thin layer of chemical SiO₂ present at the interface
- There are charges and trap states at various interfaces and grain boundaries
High-k Gate Dielectric Can Also be Applied to Other Semiconductors

- Passivation of Ge with GeO$_x$N$_y$, ZrO$_2$ and HfO$_2$
- 1st demo of Ge MOSFETs with hi-$\kappa$
- $p$-MOSFET with 3x mobility vs. Hi-k Si
- Passivation of many other materials being experimented, e.g., carbon nanotubes, GaAs, etc.

Issues With High k Dielectrics

- How good is the interface with Si? $\Rightarrow$ mobility
- Contamination of Si by metal atoms
- Compatibility with gate electrode $\Rightarrow$ metal gate
- Device reliability and lifetime
- Minimum EOT achievable
- Technology integration

More research is needed to make these materials manufacturable and reliable
Reduced Mobility in High- K Gate Stacks

\[ \frac{1}{\mu_{\text{eff}}} = \frac{1}{\mu_{C}} + \frac{1}{\mu_{\text{ph}}} + \frac{1}{\mu_{sr}} \]

Possible Sources for Reduced Mobility in High- K Gate Stacks

Extensive research is needed to understand these mechanisms and how to minimize their impact on device performance.
Effect of Interface states on CV curves

- Severe distortion, hysteresis, and frequency dependence in C-V can be observed if large number of slow states are present.
- This causes degradation in device properties, such as, $V_t$, mobility, etc.

Effect of Slow $D_{it}$ states on CV Curves

- Measurement is like a regular C-V setup with a DC sweep from $+$ve to $-$ve followed by a DC sweep from $-$ve to $+$ve.
- Hysteresis in C-V is due to the VERY slow states that do not empty out fast enough and cannot even respond to the slow DC sweep.
Effect of Interface States on Mobility in High- K Gate Stacks

Effect of interface traps on mobility. Coulombic scattering reduces the mobility.

Ref: T. P. Ma, IEEE TED, Jan 04

High-K/Poly-Si Gate Transistors

- High-K/poly-Si gate transistors suffer from high $V_T$, degraded channel mobility and poor drive performance.
- Phonon scattering limits channel mobility in high-K/poly-Si gate MOSFETs.

R. Chau, Intel, ICSICT 2004
Metal Gate Screens Surface Phonon Scattering and Improves Mobility in High-K Transistors

R. Chau, Intel, ICSICT 2004

Annealing Crystallization of ALD-HfO₂

In-situ anneal at 520°C using 30Å HfO₂ on 25Å thermal SiO₂.

- Upon annealing the amorphous films crystallize
- Grain boundaries cause statistical variation in the properties
- By adding other elements (e.g. N, Al, Si) to HfO₂ crystallization can be impeded
Crystallization and Phase Separation

- Non-uniformity of k-value leads to mobility degradation
- This can occur in the case of silicates.

B. Foran et al., ALD conference, 2004

Luigi Colombo, et al., (T.I.) IWGI Nov 2003 Tokyo, Japan
Mobility: N Incorporation in HfSiO

Luigi Colombo, et al., (T.I.) IWGI Nov 2003 Tokyo, Japan

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