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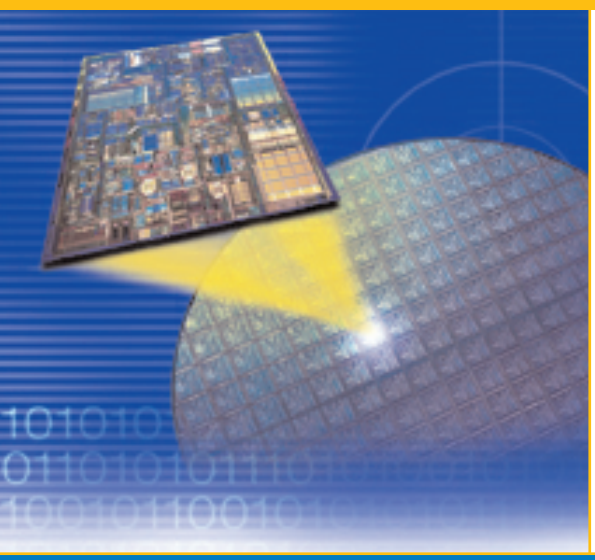

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Transistor Elements for 30nm Physical Gate Length and Beyond

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Transistor Elements for 30nm Physical Gate Lengths and Beyond

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ABSTRACT

We have fabricated conventional planar transistors of various gate lengths down to as small as 10nm polysilicon gate lengths, in order to examine transistor scaling. At 30nm gate lengths, the devices show excellent device characteristics, indicating that this node can be met with conventional transistor design. At lower gate lengths of 20 and 15nm, the devices still maintain excellent device characteristics and follow traditional scaling with respect to gate delay and energy delay, although off-state leakage and gate leakage do increase. At 10nm gate lengths, the transistors continue to function as MOS devices, but they are limited by off-state leakage.

One feasible method of significantly improving off-state leakage is through reducing the sub-threshold gradient. We show that *Depleted Substrate Transistors (DST)*, a broad category of devices that include single- and double-gate transistors, whose active channel region stays fully depleted during operation, can achieve near-ideal sub-threshold gradients and a reduction in off-state leakage of at least two orders of magnitude over bulk transistors. We believe that DST architecture will adequately address transistor scaling needs down to 10nm gate lengths.

In addition to DST device architecture, new electronic materials and modules will be needed to maintain high performance and low-parasitic leakages. As an example, to alleviate increasing gate leakage, changes in the gate stack are necessary. Replacement of SiO_2, the workhorse of the industry for over 30 years, with a high-K dielectric will be required. Other changes will include use of raised source/drain, metal gate electrodes and channel engineering.

INTRODUCTION

Moore's Law, formulated in the 1960s, states that the transistor count on an integrated circuit chip doubles every 18 months and has been the driving force behind the phenomenal growth of the semiconductor industry. This same law, which is the basis for the International Technology Roadmap for Silicon, guides the industry with respect to the features of future generations [1].

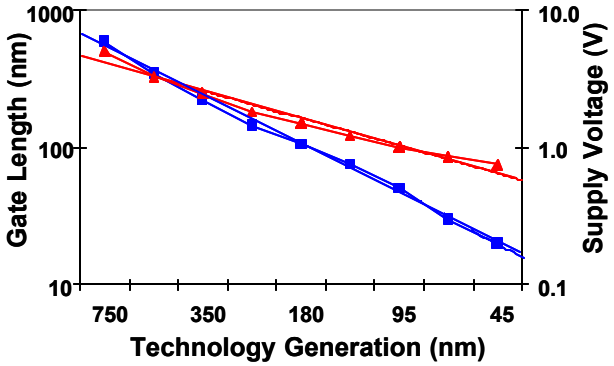

Figure 1: Gate length and power-supply voltage vs technology node

One of the most important consequences of scaling resulting from Moore's law is transistor gate length scaling. Figure 1 shows the gate lengths and power-supply voltages as a function of technology generation. Historically, the power supply scales at 0.85x/generation, while the gate length scales at 0.65x/generation. The gate length has been scaling and is expected to continue to scale at considerably less than half the lithography pitch for future generations. With respect to the power supply,

the voltage is expected to drop below one volt shortly, and continue to decrease. It is thus of considerable interest to study the implications of gate length and power-supply scaling for transistor design and architecture.

In this paper, we examine gate length scaling on bulk MOS devices. Although we concentrate mostly on n-MOS devices, the same results and conclusions are true for p-MOS transistors as well. Using special lithographic techniques, we show that it is possible to shrink gate lengths as small as 10nm and still maintain meaningful transistor functionality. The device characteristics of transistors at these small gate lengths and associated scaling issues are discussed in detail. Possible solutions to enable continued scaling are then proposed.

GATE LENGTH SCALING

Polysilicon Patterning

In order to examine the consequences of gate length scaling down to 10nm, a methodology for patterning polysilicon at these extreme dimensions, called *Spacer Gate* (SG) [2], has been used.

This approach has recently been shown to be capable of generating line widths down to 6.5nm [3]. The SG process steps are outlined in Figure 2.

After poly gate electrode deposition, an oxide layer (100nm) is deposited and patterned so that the edge of the oxide blocks is aligned to the edge of the gates to be patterned. A nitride film is deposited on the wafer, whose thickness determines the dimension of the gate to be printed. The nitride is now RIE-etched, leaving a nitride spacer on the oxide block sidewalls. The oxide block is now removed, and the polysilicon is then etched, leaving polysilicon lines whose dimensions are controlled simply by the thickness of the nitride film deposited.

There are several inherent advantages to the SG approach over conventional lithography:

> The dimensions of the lines being printed depend only on the thickness of the nitride layer deposited.

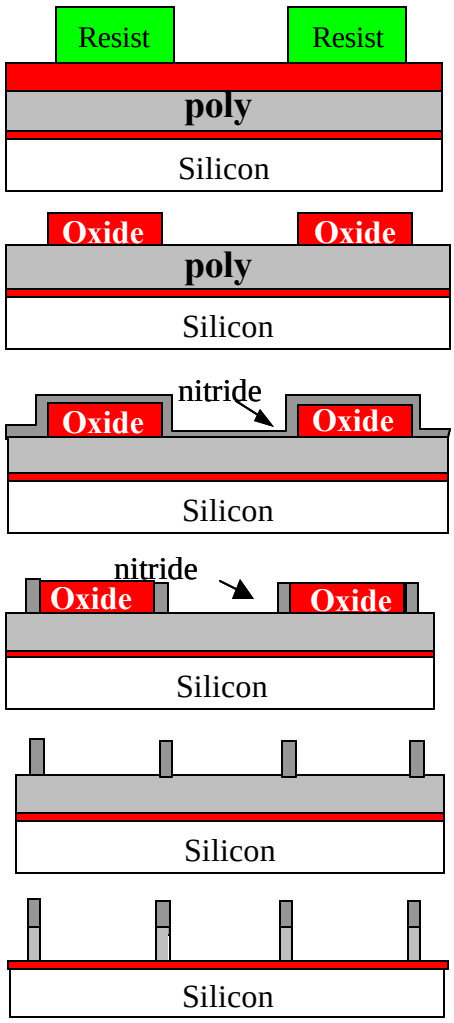

Figure 2: Spacer Gate flow

Since every oxide block produces two poly lines (see Figure 2), the pitch needed for the SG is half that of conventional lithography, and hence an n-2 generation lithography tool can be used to print nth-generation poly lines.

Critical Dimension (CD) control from SG would be expected to be superior to conventional lithography, since it depends simply on the deposition and etch of a thin film in contrast to the many factors that come into play in conventional lithography.

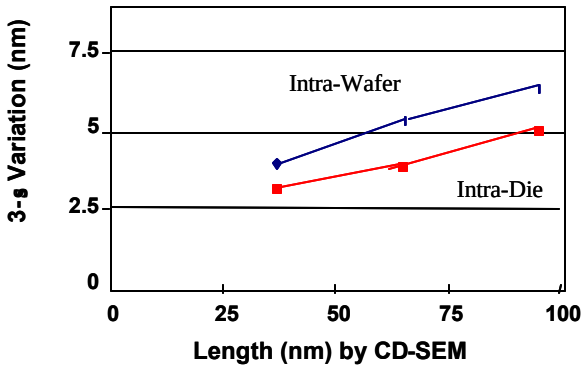

Figure 3: Gate length vs 3-s Electrical CD variation for structures fabricated by Spacer Gate techniques

In order to test for CD control with SG, Electrical CD (ECD) structures were measured (Figure 3). For structures measuring 95nm, 65nm, and 38nm, the intra-wafer 3- CD control measured 6.3, 5.3, and 3.9nm respectively. The intra-die values were even tighter, at 4.9, 3.8, and 3.1nm respectively, meeting the 10% 3- CD variation targets of the silicon technology roadmap [1].This SG approach enables the fabrication of polysilicon lines down to 10nm using 248nm lithography. Figure 4 shows an example of the methodology. The top-down Scanning Electron Microscope (SEM) micrograph of a polysilicon line, fabricated using a nitride film whose thickness was 30nm, resulted in poly lines with a width of 30nm. It can also be seen that the lines are extremely straight, showing very little line-edge roughness.

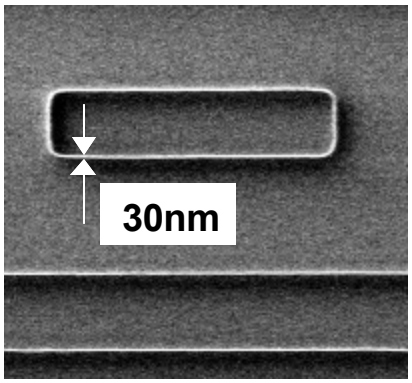

Figure 4: Top-down SEM of poly lines printed using the Spacer Gate technique

This technique was used for the fabrication of n-MOS transistors to explore transistor scaling. An example of a 15nm device fabricated using this technique is shown in Figure 5 .

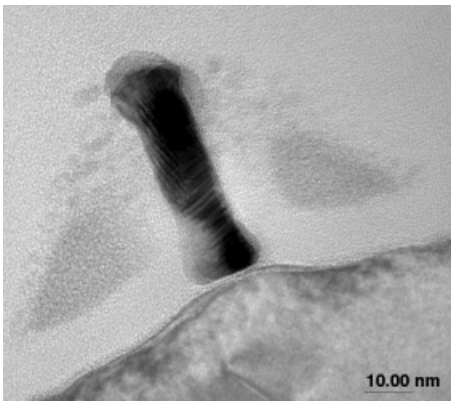

Figure 5: TEM cross-section of a 15nm transistor

For the devices discussed in this paper, the physical gate oxide was aggressively scaled to sub-1.0nm in order to achieve high drive currents and controllable short channel effects. Figure 6 (insert) shows a TEM cross-section of the sub-1.0nm gate oxide. Because of difficulties in measuring GV in the presence of high gate leakage, a transmission line model was used [4]. Figure 6 also shows the inversion GV characteristics of the resulting gate stack. An inversion capacitance exceeding 1.9 F/cm^2 was achieved for both p- and n-MOS.

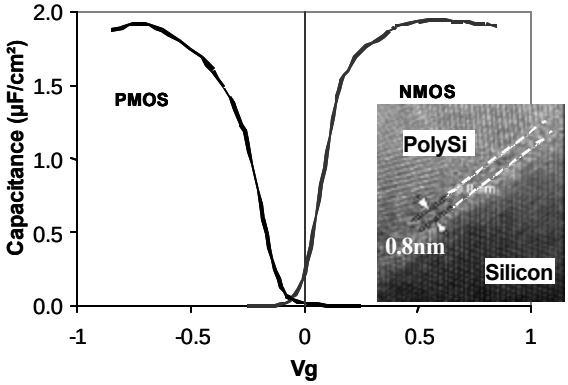

Figure 6: Inversion C-V capacitance

In order to control short channel effects and achieve sufficiently low external resistance and overlap capacitance, retrograded wells, aggressively scaled S/D and S/D extensions, and thermal anneal temperatures below 1000°C were used. To minimize the poly depletion effect with scaled junctions, the polysilicon gate thickness was scaled to below 100nm. The silicide was also scaled with junction scaling.

Figures 7 and 8 show the I-V characteristics of a 30nm device [5]. It can be seen that this transistor shows excellent I_{on}-I_{off} performance with I_{on}=570 A/ m for n-MOS and 285 A/ m for p-MOS with I_{off} at or below 100nA/ m at a scaled-down voltage of Vcc=0.85V.

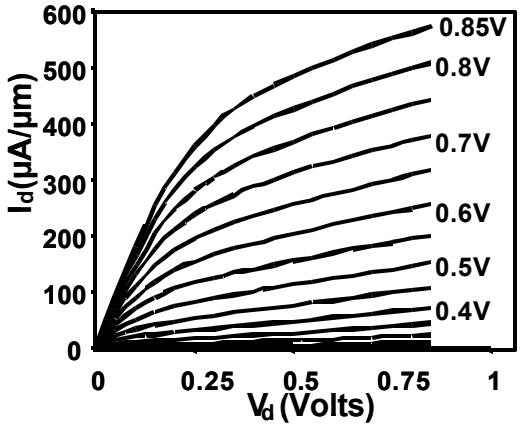

Figure 7: MOSFET I_d-V_d curves for the 30nm n-MOS

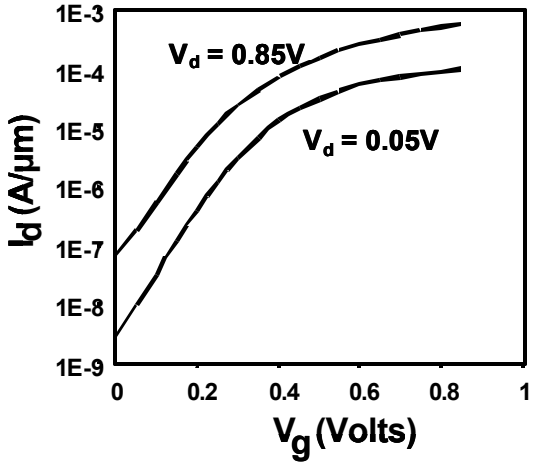

Figure 8: MOSFET sub-threshold I_d-V_g curves for the 30nm n-MOS device

Going to even shorter channel lengths, Figures 9 and 10 show the I-V characteristics of an n-MOS device with a 15nm physical gate length.

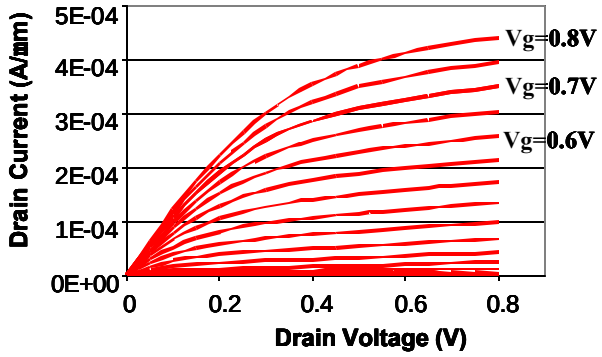

Figure 9: I_d-V_d characteristics for a n-MOS transistor with a physical gate length of 15nm

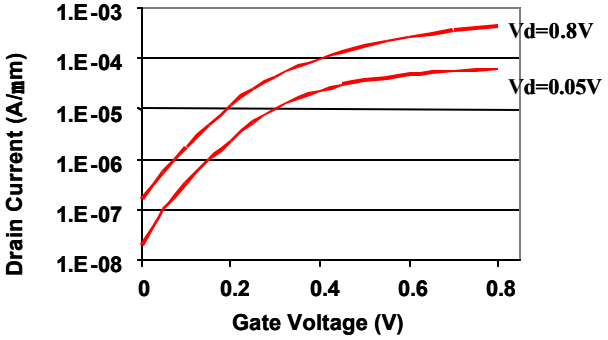

Figure 10: Id-V_g characteristics for the same 15 nm gate length device as in Figure 9

Figure 9 shows the I_d-V_d characteristics for different applied gate voltages, while Figure 10 shows the I_d-V_g at V_d=0.05V and V_d=0.8V. It can be seen that the device has I_{off} of 180nA/ m at V_{cc}=0.8V, a sub-threshold gradient of 95mV/decade at V_{cc}=0.85V, and a Drain Induced Barrier Lowering (DIBL – the gate voltage difference for Id=1E-6 A/ìm between Vd=0.05V and Vd=0.8V) effect of about 90mV/V. These results suggest that the device has a controllable short channel effect. The drive current for this device is 443 A/ m at V_{cc}=0.8V, as can be seen from the Id-Vd characteristics of Figure 9.

Moving to smaller dimensions, Figure 11 shows a cross-sectional TEM of a transistor with poly gate length measuring only 10nm. At these dimensions, even the slight recessing of the source-drain region becomes greatly magnified and tends to thicken up the gate oxide. Another aspect of the device is that the height to width of the transistor is approximately scaled, the height being approximately 50nm for this 10nm L_g transistor.

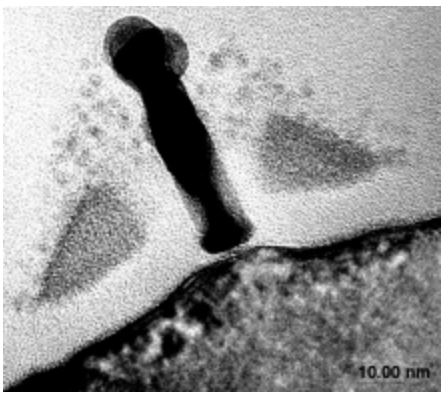

Figure 11: TEM cross-section of a 10nm transistor

To get a perspective of the magnitude of the scaling to get to 10nm, Figure 12 compares TEM's from the 0.18 micron technology node with the 10nm transistor (circled in this figure) on the same scale. It can be seen that the transistor is barely visible at this magnification, and that to

get these dimensions, not only the width, but the height is also scaled.

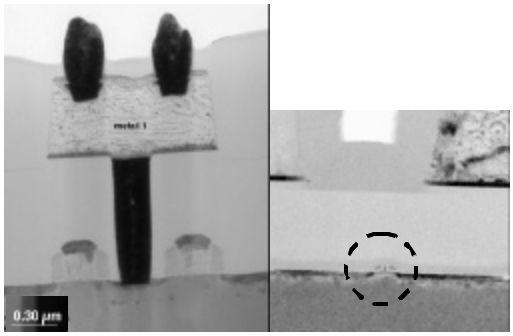

Figure 12: 0.18um technology node transistors (left), with 10nm transistor (circled on right) on the same scale

The transistor characteristics of a 10nm L_g device are shown in Figure 13. It can be seen that at this gate length, the transistor still behaves as a MOS device, although there is now increased conductance in the saturation region, and the leakage current (at V_g=0V) continues to increase. This is in part due to a relatively thicker gate oxide used in the present study than required at this technology node. A thinner Tox would give much better Short Channel Effects (SCE) control.

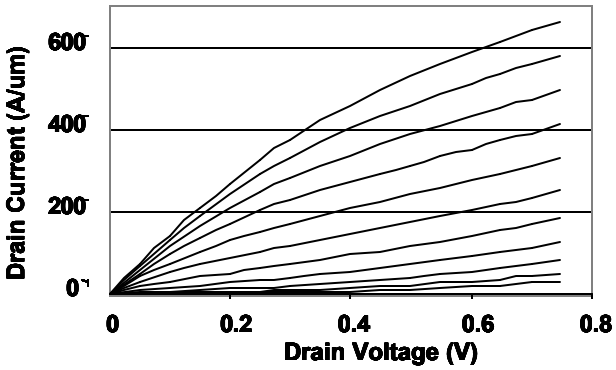

Figure 13: Id-Vd curves of 10nm transistor. V_g to 0.75V, steps of 0.1V

It should be noted that the supply voltage has been scaled in going from 30nm to 10nm poly lengths. Nevertheless, the leakage for the smallest gate length transistors is an issue of some importance. This is discussed later.

Taking the drive current values for the gate delay and energy delay, and plotting these against published data for longer gate lengths (Figures 14 and 15), it can be seen that the devices continue to scale on the same historical rate, even down to the lowest gate lengths. At 15nm, the gate delay is 0.39psec, and for 10nm gate length, the gate delay has dropped to 0.11psec (Figure 14). Similarly, the energy-delay product also drops exponentially, as can be seen in Figure 15, decreasing almost two orders of magnitude between the 30nm transistor and the 10nm transistor. Thus, even though the drive currents on these research transistors are not high (due to voltage scaling), they maintain the historic trend in gate delay and energy-delay.

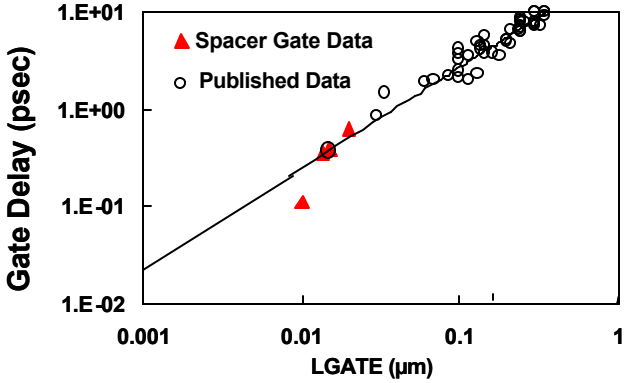

Figure 14: Gate delay for published & Intel Spacer Gate transistors

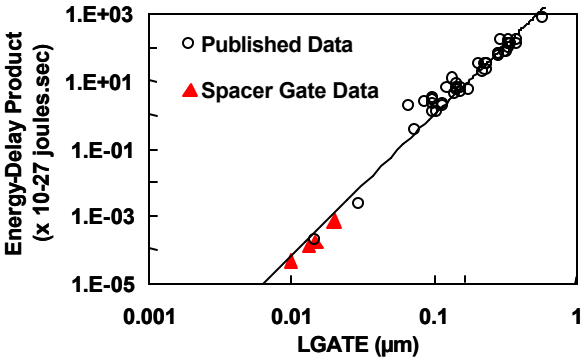

Figure 15: Energy delay for published & Intel Spacer Gate transistors

TRANSISTOR LEAKAGES

Junction Leakage

Returning to the issue of leakage current, there are three dominant sources of leakage: junction leakage, gate leakage, and off-state leakage. These three sources of leakage increase as transistors are scaled down towards 10nm.

Commencing with junction leakage, it has been suggested that this source of leakage alone will limit scaling [6]. This leakage arises from the high doping concentration in the channel region required to attain threshold voltages, and to limit short channel effects in aggressively scaled devices. The proximity of the valence and conduction bands in the depletion region of the junctions causes a parasitic tunneling current. Figure 16 shows the junction

edge leakage (I_{JE}) as a function of substrate doping at 25°C and 1V reverse bias. Although the leakages are high (above 1nA/ m at L_g=30nm), they are still a lot less than the other sources of leakage at 30nm, with less than 1.0nA/um for both n-MOS and p-MOS, a small percent of the transistor I_{off}.

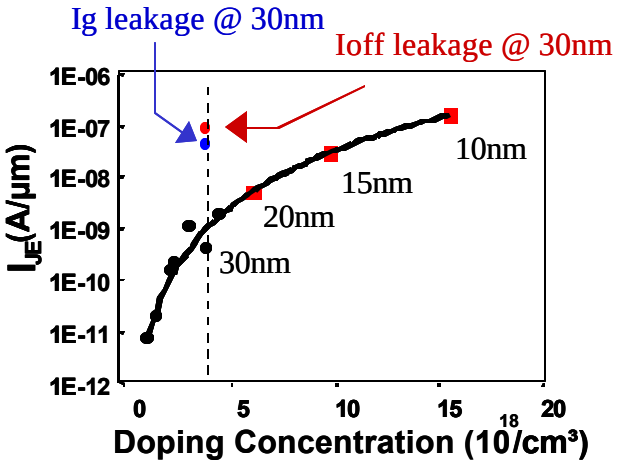

Figure 16: Junction leakage vs doping concentration. Circles - data, squares - extrapolated points. Other sources of leakage at L_g=30nm have been added to the graph

The arrows in Figure 16 indicate gate leakage and off-state leakage for L_g=30nm, both of which are more than an order of magnitude greater than the junction leakage. For the shorter channel devices, extrapolating to the 10nm gate lengths, and assuming a 1.6x doping concentration increase per technology generation, the junction leakage is still far below a value of 1 A/ m, the upper leakage limit.

Gate-Oxide Leakage

With respect to other sources of leakage, gate-oxide scaling has long been considered an eventual limiter for gate oxides below ~2nm gate dielectric thickness [7]. It was felt that with oxides reaching the thickness of several atoms, gate leakage would rival and would surpass the transistor off-current leakage. However, the examination of gate oxides down to 0.8nm [5] has not shown this to be the case in the present study. Figure 17 shows the gate current versus gate bias for the 0.8nm oxides [5]. The measurement results show that at 0.85V and 100°C, the gate leakage value is in the mid-10^{-8}A/ m^2, approaching the off-state leakage level of the 30nm L_g transistor (see Figure 16).

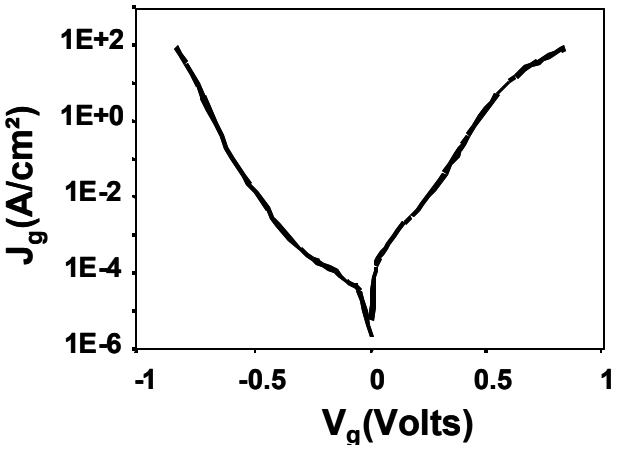

Figure 17: Gate current leakage for a 0.8nm oxide for the 30nm transistor [5]

Extrapolating further, below 0.8nm of gate-oxide thickness, leakage will become a limiter. With this in mind, research on high-K dielectrics for MOS transistor applications has become an area of active research. The reason for this is shown in Figure 18. It can be seen here that for the same equivalent oxide thickness (the thickness that SiO_2 would have for a given capacitance value), the high-k dielectric has more than four orders of magnitude less gate leakage than SiO_2.

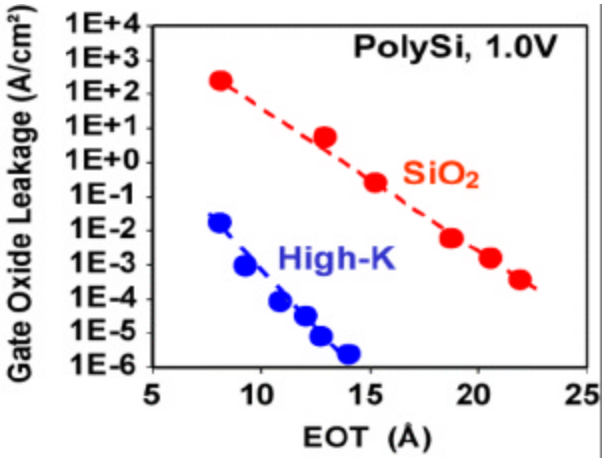

Figure 18: Comparison of gate leakage between SiO_2 and high-K dielectrics

Thus, for future scaling, a change in the transistor architecture to include high-K dielectrics will be necessary if gate capacitance scaling is to continue down to 10nm gate lengths.

Off-Current Leakage

Transistor leakage is perhaps the greatest problem facing continued scaling. As the transistor scales, the internal fields become greater, which necessitates scaling of the power supply voltage. This is also driven by the need to

decrease the power (P) generated by the chip, which is governed by the equation

$$P=C.V^2.f + I_{off}.V \qquad (1)$$

where f is the chip frequency, C is the gate-oxide capacitance, and I_{off} is the total transistor leakage current for the chip. The first part of Equation 1 refers to the active power, and the second refers to the off-state power. From this equation, it can be seen that reducing V has a significant effect on power. Scaling the power supply also necessitates the scaling of V_t, if Idsat is to be maintained. However, decreasing V_t results in increasing I_{off}, which in turn increases the off-state power.

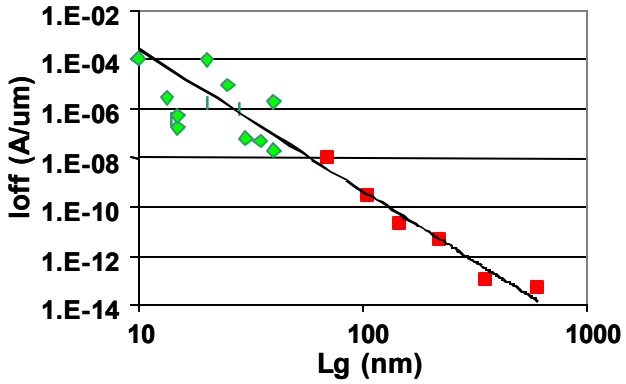

Figure 19: Transistor off-state leakage vs gate length
Red squares indicate pre-production transistors
Green diamonds indicate research devices

Figure 19 shows transistor off-state (source-drain) leakage versus transistor gate length. The red symbols are taken from the literature for transistors near production at the time of publication, while the green symbols are for 'research' devices (devices several generations from production at the time of their publication). Drawing a trend line through the data shows that the research transistors fall roughly on the same trend line that the advanced production devices fall on, irrespective of the gate length, obeying the power law relationship:

$$I_{off}=A.L_g^{-5.6} \qquad (2)$$

The fact that the research devices below 50nm follow the same relationship established for *pre-production* transistors at longer gate lengths suggests that this relationship is intrinsic to the scaling of bulk transistors using current methodologies (meaning the scaling of gate length, drive current, and voltage at the same time). Historically, it is the leakage current that has been relaxed to enable us to achieve the drive current scaling. If this same scaling methodology continues, controlling off-currents while at the same time maintaining aggressive drive currents will be difficult in bulk CMOS.

The effect of increasing I_{off} on total power [8] is illustrated in Fig. 20. In this figure, the off-state and active power components to the total leakage are plotted by taking 30 meters of transistor width for each technology generation (note that the chip leakage per generation increases since the total transistor width per generation also increases).

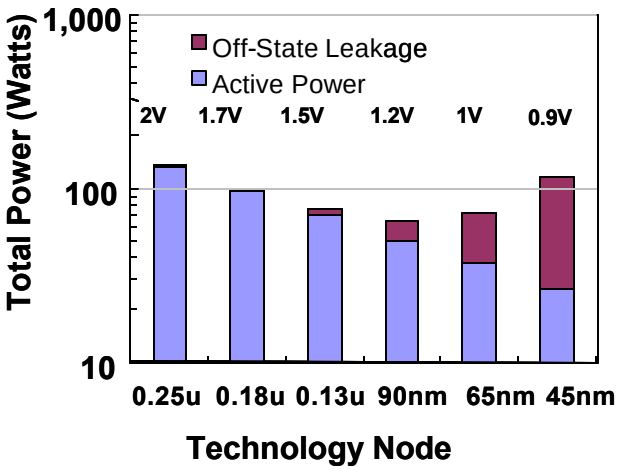

Figure 20: Total power as a function of technology node, for a fixed (30m) total transistor width, showing the increasing importance of off-state current as technology scales

It can be seen that the off-state leakage component to total power exceeds active power as the technology decreases beyond the 65nm node. Thus, finding a solution to the off-current issue is one of the most important challenges facing transistor design.

TRANSISTOR ARCHITECTURE FOR LEAKAGE

Depleted Substrate Transistor–Single Gate

One of the ways to overcome the issue of static power is to increase the threshold voltage. However, increasing the threshold voltage while scaling the power-supply voltage decreases the drive current of the device. A feasible way of addressing the power issue is to improve the sub-threshold gradient of the transistor. As the transistor scales, and the channel doping increases to support the thinner oxide, the sub-threshold gradient degrades. The sub-threshold gradient is linked to the depletion capacitance by the equation

$$S=(kT/q).\ln 10.(1+C_D/C_{ox}) \qquad [4]$$

where T is the temperature, q is the electronic charge, S is the sub-threshold gradient, CD is the capacitance of the depletion region, and C_{ox} is the gate-oxide capacitance [9]. From equation 4, it can be seen that decreasing the depletion capacitance C_d will improve the sub-threshold

gradient towards the minimum theoretical value of 60mV/decade. Decreasing C_D can be achieved by the use of Silicon-On-Insulator with a fully depleted substrate, since the depletion layer now extends through the buried oxide into the substrate. The value of C_D then becomes negligible compared to C_{ox} in Equation 4. We call this broad category of devices, which include several elements necessary for future scaling, a Depleted Substrate Transistor (DST), and this can be seen in Figure 21 [10].

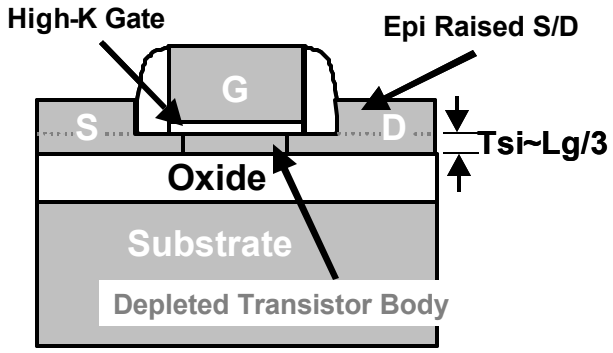

Figure 21: Illustration of Depleted Substrate Transistor (DST)

We define the DST as consisting of three elements:

The body of the device is fully depleted, be this double-gate (DG) [9] transistors, gate-all-around transistors (GAA) [11], or even transistors whose bodies are no longer silicon (III-V's etc.).

The gate dielectric is a high-k material mentioned previously.

The junctions are raised epitaxial source/drain.

Figure 22 shows a TEM cross section of such a device. The epitaxial raised source/drain are necessary to decrease the series resistance of the transistor, due to the thin silicon body.

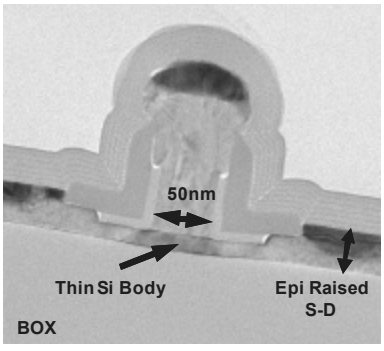

Figure 22: TEM of the Depleted Substrate Transistor (DST)

Depleted Substrate CMOS transistors were fabricated on a thin silicon body with a thickness of <25nm on top of a ~200nm buried oxide. The physical gate-oxide thickness was equal to 1.5nm, the same as the bulk devices. Figure 23 shows the I_d-V_g characteristics of two 60nm L_g n-MOS transistors, a bulk transistor and a DST.

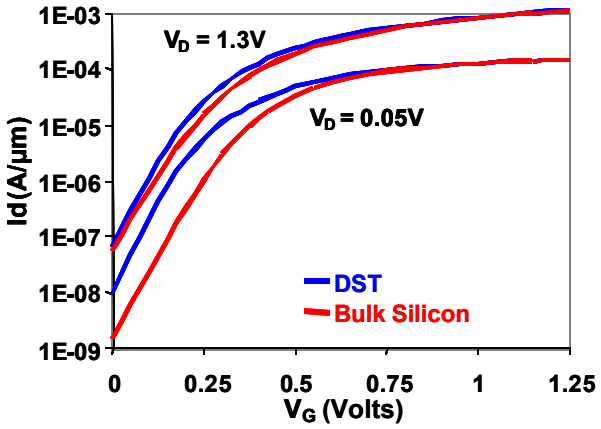

Figure 23: Log Id-V_g characteristics of a bulk and DST transistor

Two features can be seen from this figure: the sub-threshold gradient, which has improved from 95 mV/decade to 75mV/decade, and the DIBL, which has decreased from 100mV/V to 45 mV/V. The improved sub-threshold gradient thus allows the DST to decrease threshold voltage by 40-50mV, while the improvement in DIBL allows a further 50mV decrease in V_t. As power supply voltages decrease below 1V, the DST devices will allow substantial gains in gate overdrive (V_g-V_t), as well a reduction in off-state power by 2 orders of magnitude.

Depleted Substrate Transistor–Double Gate

As transistors continue to scale, control of short channel effects become more and more important. It will be increasingly difficult to control the electrostatic communication between source and drain that results in transistor leakage by using bulk or even single-gate DSTs. Solutions are being researched that enclose the channel area by the gate stack. The most common form of this transistor architecture is called the *Double-Gate* transistor.

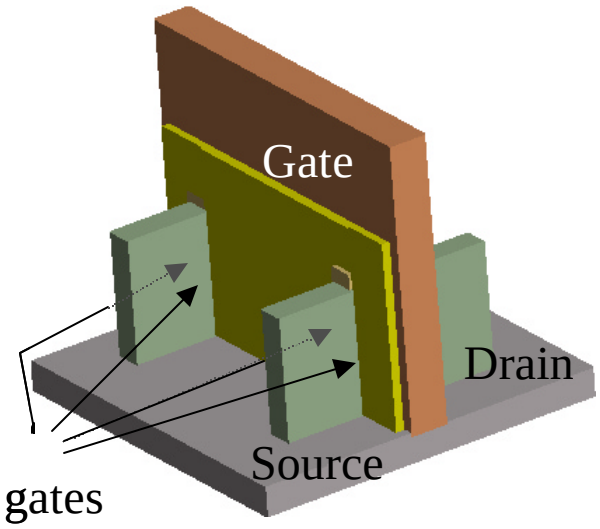

Figure 24: Illustration of a two-FinFET Double-Gate transistor. The current flows along each sidewall of the fins

Figure 24 shows an illustration of a two-fin transistor, one form of double-gate device. In this case, the current runs along both sidewalls of the fins.

The gate controls the front and back of such a double-gate transistor, thus offering better short channel control than a single gate. However, double-gate devices are much more difficult to fabricate due to their three-dimensional nature. Figure 25 shows a double-gate FinFET device in the direction of current flow and Figure 26 shows the transistor perpendicular to current flow.

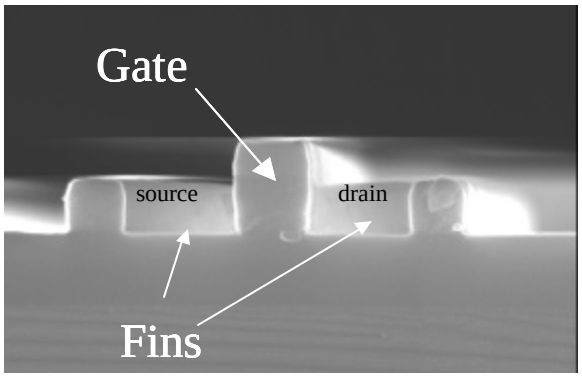

Figure 25: SEM of Double-Gate Multi-Fin Structure

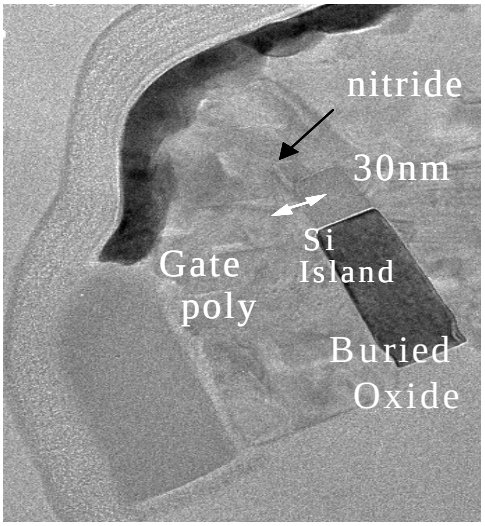

Figure 26: TEM cross-section of a 30nm double-gate device

In terms of short channel control, simulations have shown that double-gate devices can buy up to a two-generational gain in DIBL over single-gate DSTs [12]. However, it should be noted that one of the issues concerning both types of device is the thickness of the silicon that forms the channel region. In the case of single-gate DSTs, the thickness of the silicon channel body has been found to be approx $L_g/3$. In the case of double-gate DSTs, the thickness of the Fin is twice the body thickness ($2L_g/3$), as each gate controls a thickness of $L_g/3$.

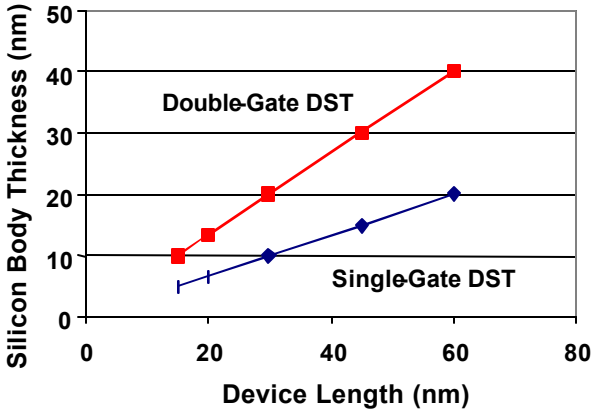

Figure 27: Silicon body thickness required for full depletion of a single-gate DST and a double-gate DST

As the gate length scales, the thickness of the silicon body (Tsi) also scales. Figure 27 shows the thicknesses needed to provide full depletion for both single- and double-gate DSTs. It can be seen that for single gates, the thickness quickly approaches to less than 10nm. This constraint of requiring Tsi < 10nm is relaxed in FinFETs,

since the Tsi is perpendicular to the wafer plane (Figure 24), and the thickness values are twice that of single-gate DSTs (Tsi is the fin width in the case of double-gates). However, this dimension is achieved using lithography, and this means that the most critical lithography step is no longer polysilicon patterning, but Fin patterning. In other words, for FinFET devices, the fin width needs to be smaller than the gate length. For example, for 20nm L_gs, the Fin patterning will require lithography that can reproducibly print 13nm Fin widths.

Drive Current

One of the most serious issues with gate length scaling is our ability to maintain high drain current as the power-supply voltage scales without being able to fully scale V_t, which remains high to control transistor leakage currents. The power-supply scaling shown in Figure 1 suggests that keeping Idsat constant will be a significant challenge. In order to illustrate this point, Figure 28 shows the data from a 20nm gate length device at Vdd=0.85V and Vdd=0.7V. It can be seen that a power- supply voltage drop of 0.15V results in a drop of 30% in the drive current capabilities of the transistor, from 533 A/ m to 375 A/ m. Some of the issues facing drive current scaling are discussed below.

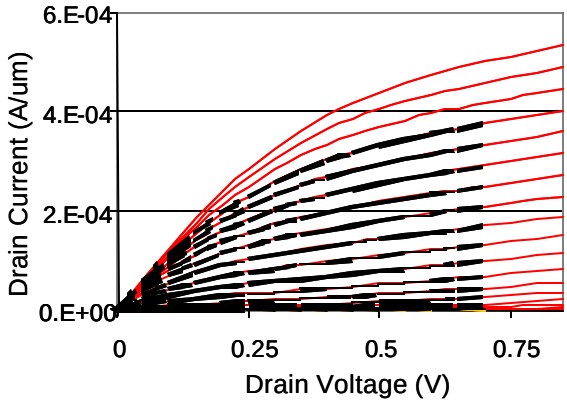

Figure 28: Id-Vd characteristics for the 20nm transistor at two different supply voltages, 0.85V and 0.7V

Series Resistance

With DST-like devices comes the need to keep the body thickness in the range that allows for complete depletion. In the representation of the DST transistor in Figure 21, the thickness of the silicon body (T_{Si}) needs to be kept to around $L_g/3$ to maintain complete depletion (see also Figure 27). As the transistors scale to L_g=20nm, the body thickness will need to be of the order of 6-7nm. Apart from the fabrication issues for such thin bodies discussed above, the increase in series resistance arising from ultra-thin junctions will limit transistor drive currents [13].

The solution to the drive current issue (from external parasitic resistance) is to use raised source/drain, which increases the effective thickness of the junctions and hence the junction conductance [14]. Figure 29 shows the advantage of raised source/drains over conventional junctions on DST transistors. The transistors with and without raised source/drain were fabricated with a gate length of 60nm. At matched I_{off} of 60nA/ m, DST devices with raised source/drain (blue lines) exhibit superior drive currents, up to 50% more than the non-raised source/drain DST structures (red lines).

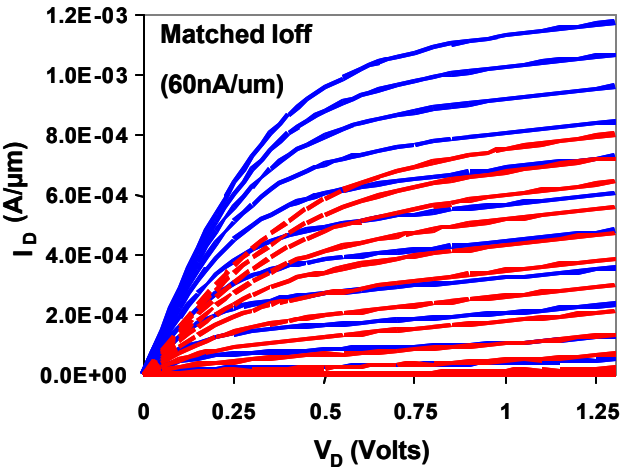

Figure 29: I_D-V_D characteristics for 60nm DST transistors, with no raised S/D (red lines), and with raised S/D (blue lines)

Figure 30 further illustrates the performance gains that can be obtained in combining DST with raised source/drains. Figure 30 shows the PMOS I_{on}-I_{off} comparison of the depleted-substrate transistor with and without raised source/drain, and the standard 0.13um-generation bulk Si transistors at V_d = 1.3V. For a given I_{off} (e.g., 1.0 nA/um), the depleted-substrate transistor with raised source/drain shows the highest I_{on} value, about 30% higher than the standard bulk Si transistor. Conversely, at a fixed drive current (e.g., at 0.6mA/ m), the off-current is decreased by about two orders of magnitude for DST.

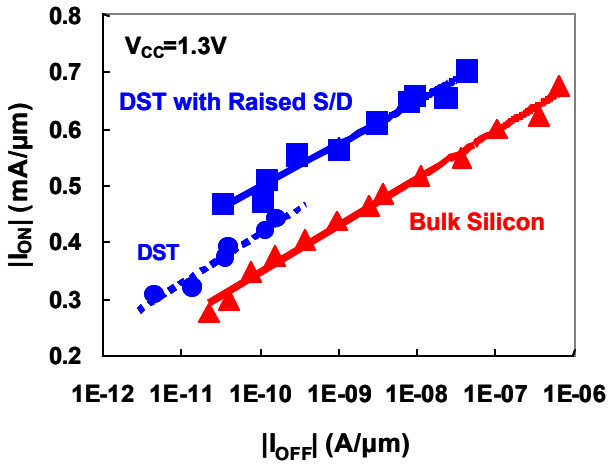

Figure 30: Comparson of p-MOS bulk silicon (triangles), DST (circles) and DST with raised source/drains (squares)

Another way of looking at the data is from a power-supply perspective. DST pMOS with raised source/drain achieves the same I_{on}-I_{off} performance at 1.1V as the bulk-device at 1.3V, thus enabling a reduction in power by 30% (power voltage^2).

GATE STACK

As discussed in a previous section, future transistor design will need to incorporate high-K dielectrics for continued transistor scaling. One of the considerations with high-k dielectrics is the dielectric integrity at high frequencies. With clock speeds already in the gigaherz, the gate material must maintain its dielectric integrity to frequencies well above this. If the responding material cannot follow the switching at high frequencies, the high dielectric constant measured normally at low frequencies will not be obtained, and therefore the gate capacitance and subsequent drive current will be reduced. Figure 31 shows measurements of dielectric constant as a function of frequency for three different materials, SiO_2, HfO_2, and ZrO_2, up to 20GHz. It can be seen that HfO_2 and ZrO_2 show the same invariance to frequency that the SiO2 dielectric shows.

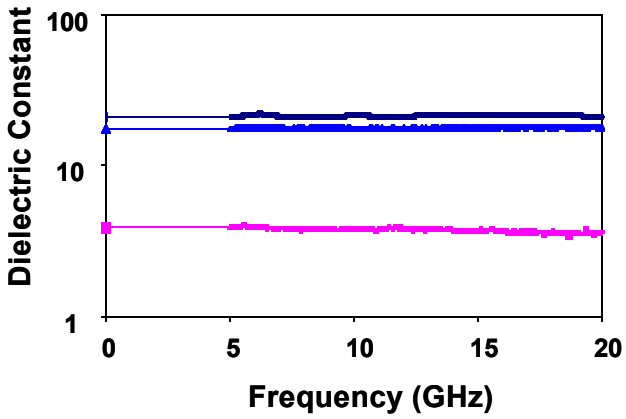

Figure 31: Dielectric constant versus frequency for SiO_2 (bottom) and the High-Ks, ZrO_2 and HfO_2 (bottom)

The dielectric itself is not, however, the only issue in maintaining high gate capacitance. There are other capacitance elements that tend to reduce the net gate capacitance. The gate stack enters into the transistor saturation current equation through the term C_{oxe}:

$$Id = .C_{oxe}.(Z/L).(V_g-V_t)^2 \qquad [3]$$

Where C_{oxe} is the equivalent capacitance of the gate stack (C_{oxe}= $_{SiO2}/T_{oxe}$), and is made up of

$$T_{oxe}=T_{oxp} + T_{qm} + T_{pd} \qquad [4]$$

where T_{oxp} is the equivalent thickness of the dielectric itself, if it were SiO2; T_{qm} is the quantum mechanical term coming from quantization of the inversion layer, which tends to cause the electrons to reside in the silicon a short distance away from the Si/SiO_2 interface; and T_{pd} is the depletion region in the poly electrode resulting form incomplete degeneration of the gate electrode. The values typically taken for these are 0.5nm for poly depletion and 0.5nm for quantum mechanical effects [15].

The quantum mechanical contribution always persists, and even if dielectric thickness is reduced to zero, the electrical T_{ox} (inversion) would approach 1nm. A further increase in capacitance can be achieved by eliminating the poly depletion portion with use of a conductive metal gate electrode. This would reduce the equivalent oxide thickness by 0.5nm. This approach is being actively researched (e.g., [16]).

CONCLUSIONS

Transistor scaling issues have been examined to determine the implications on device performance. We have fabricated planar Si transistors down to 10nm physical gate length using a special spacer gate technique. Transistors at these aggressively scaled dimensions down

to 15nm are shown to exhibit good device characteristics. Although transistors with 10nm physical gate length show normal switching characteristics, they exhibit very high off-state leakage. To alleviate the high parasitic leakage problem, we have demonstrated a transistor structure with a fully depleted substrate (DST) providing near-ideal sub-threshold gradient and highly reduced DIBL. In addition to DST device architecture, new electronic materials and modules will be needed in the future to maintain high performance and low parasitic leakages.

REFERENCES

[1] ITRS Roadmap, "Process Integration, Devices and Structures and Emerging Research Devices section, 2001 Edition.

[2] H. Liu et al., "A Patterning Process with sub-10nm 3-CD Control for 0.1 m CMOS Technologies" *SPIE* vol. 3331, pp. 375-381, 1997.

[3] Y-K Choi et. al., "A Spacer Patterning Technology for Nanoscale CMOS," *IEEE Trans. Electron Device Letters*, vol. 49, pp. 436-441, 2002.

[4] D. W. Barlage et. al., "Inversion MOS capacitance extraction for high-leakage dielectrics using a transmission line equivalent circuit," *IEEE Electron Device Letters*, vol. 21, pp. 454-456, 2000.

[5] R. Chau et. al., "30 nm physical gate length CMOS transistors with 1.0 ps n-MOS and 1.7 ps p-MOS gate delays" *IEDM* , 2000, pp. 45-48.

[6] T. Ghani et. al., "Scaling challenges and device design requirements for high-performance sub-50 nm gate length planar CMOS transistors," *VLSI*, 2000, pp. 174-175.

[7] J.H. Stathis et. al., "Reliability projection for ultra-thin oxides at low voltage," *IEDM* 1998, pp. 167-170.

[8] V. De and S. Borkar, "Technology and Design Challenges for Low Power and High Performance," *1999 ISLPED*, pp. 163-168, August 1999.

[9] J-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, Kluwer Academic Publishers, 1991.

[10] R. Chau et. al., "A 50nm depleted-substrate CMOS transistor (DST)," *IEDM* 2001, pp. 621-624.

[11] J-P. Colinge et. al., "Silicon-On-Insulator Gate-All-Around Device," *IEDM*, 1990, pp. 595-599.

[12] H.-S.P. Wong, "Device design considerations for double-gate, ground-plane, and single-gated ultra-thin SOI MOSFET's at the 25 nm channel length generation," *IEDM* 1998, pp. 407-410.

[13]Kim, S.D., et. al., "Advanced model and analysis of series resistance for CMOS scaling into nanometer regime," *IEEE Trans. Electron Devices*, Vol. 49, pp. 457-472, 2000.

[14] S. Yamakawa et. al., "Drivability improvement on deep-submicron MOSFETs by elevation of source/drain regions," *IEEE Electron Device Letters*, Vol. 20., pp. 366-368, 1999.

[15] S.V. Walstra et. al., "Thin oxide thickness extrapolation from capacitance-voltage measurements," *IEEE Transactions on Electron Devices*, Vol. 44., pp. 1136-1142, 1997.

[16] I. Polishchuk et. al., "Dual work function metal gate CMOS transistors by Ni-Ti interdiffusion," *IEEE Electron Device Letters*, Vol. 23, pp. 200-212, 2002.

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