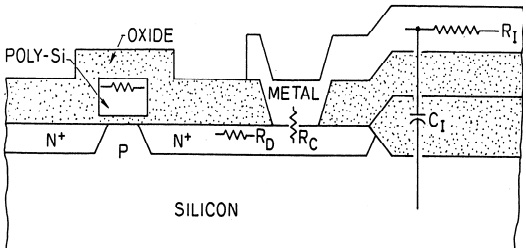
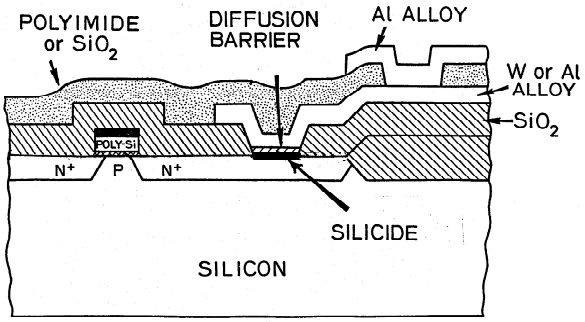
# Interconnections: Aluminum Metallization

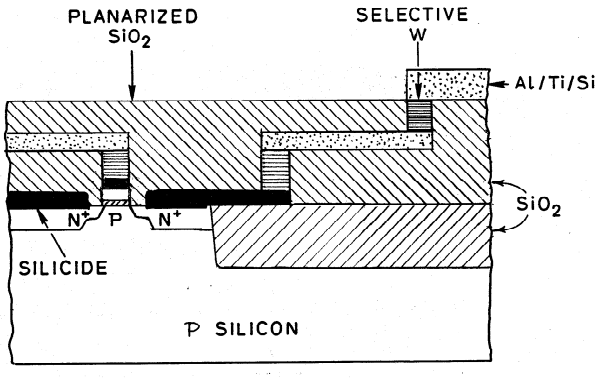
## Advances in the multilevel interconnect technology




**70's** Poly-Si
Aluminum




**80's** Local planarization
Aluminum alloys
Silicide contacts
Polycide gates




**90's** Global planarization
Salicides
CVD tungsten plugs
Low K dielectrics

**last and present decades:**
Copper
Low k dielectrics

## Conductors for Multilayer Interconnections:

Table 1 Properties of interconnect materials.

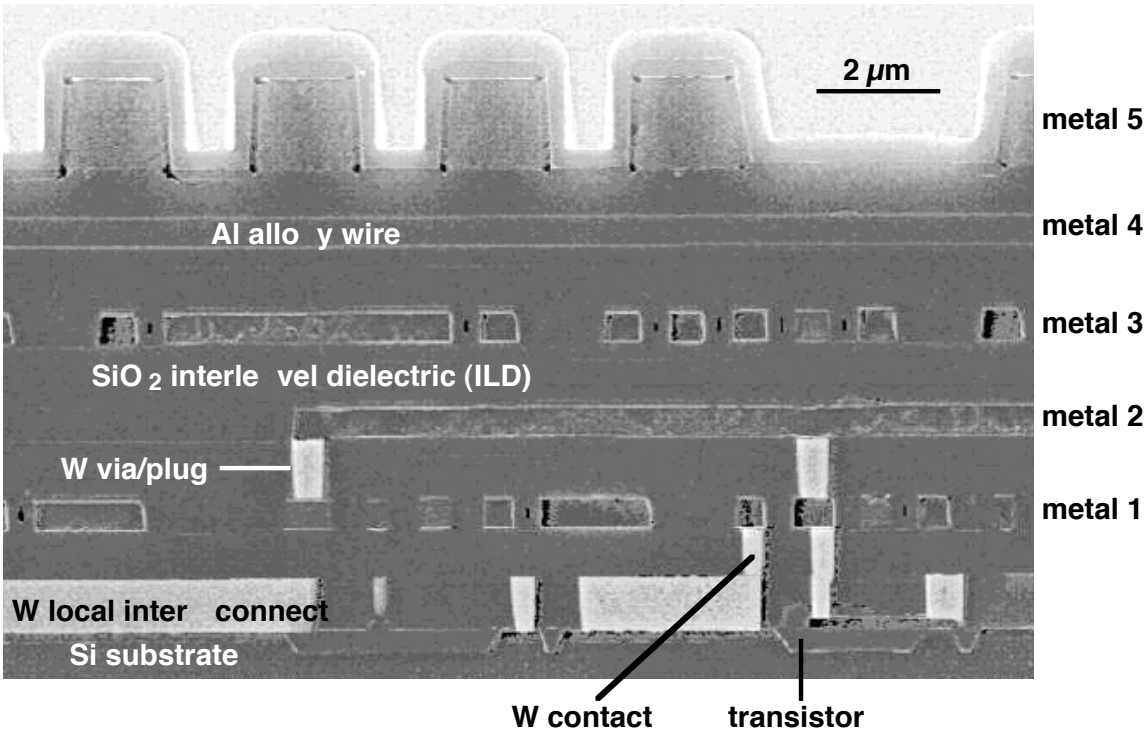
| Material | Thin film resistivity ($\mu\Omega - cm$) | Melting point (˚C) |
|---|---|---|
| Cu | 1.7-2.0 | 1084 |
| Al | 2.7-3.0 | 660 |
| W | 8-15 | 3410 |
| PtSi | 28-35 | 1229 |
| $TiSi_2$ | 13-16 | 1540 |
| $WSi_2$ | 30-70 | 2165 |
| $CoSi_2$ | 15-20 | 1326 |
| NiSi | 14-20 | 992 |
| TiN | 50-150 | ~2950 |
| $Ti_{30}W_{70}$ | 75-200 | ~2200 |
| polysilicon (heavily doped) | 500-1000 | 1410 |

- POLY-SI - For Gate electrodes and very short local interconnections where cleanliness and process compatibility are required. To reduce resistance a sandwich of poly Si and a silicide can be used (polycide).
- SILICIDES - For short local interconnections which have to be exposed to high temperatures and oxidizing ambients, e.g., polycide and salicide structures.
- REFRACTORY METALS – Via plugs, future gate electrodes, local interconnections which need very high electromigration resistance.
- TiN, TiW – Barriers, glue layers, anti reflection coatings and short local interconnections.

ALUMINUM and COPPER - For those layers where low resistivity is required, i.e., global and semi global interconnections.

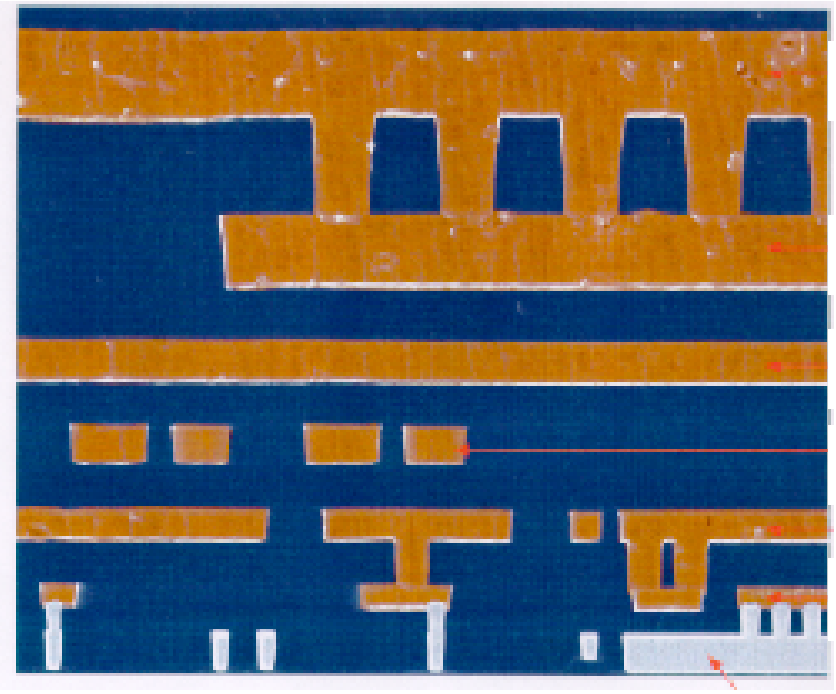
- Al has been used widely in the past and is still used
  - Low resistivity
  - Ease of deposition,
  - Dry etching
  - Does not contaminate Si
  - Ohmic contacts to Si but problem with shallow junctions
  - Excellent adhesion to dielectrics
  - Problems with Al
    - Electromigration=> lower life time
    - Hillocks=> shorts between levels

**A Motorola *µ*processor with 5 Al layers**



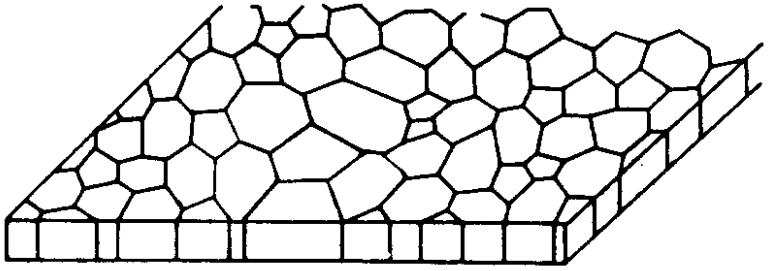
- Cu is slowly replacing Al because
  - Cu has lower resistivity => lower RC delay
  - Cu has lower electromigration => higher life time
  - Cu has fewer hillocks => less shorts between levels
  - Cu can't be dry etched => CMP
  - Cu contaminates Si => needs barriers

**IBMs 7 layer Copper Metallization Technology (1998)**

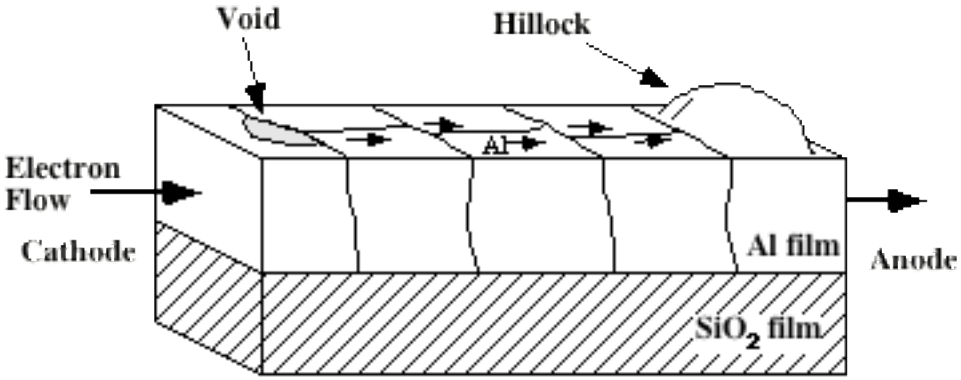



**In this chapter we will focus primarily on aluminum**

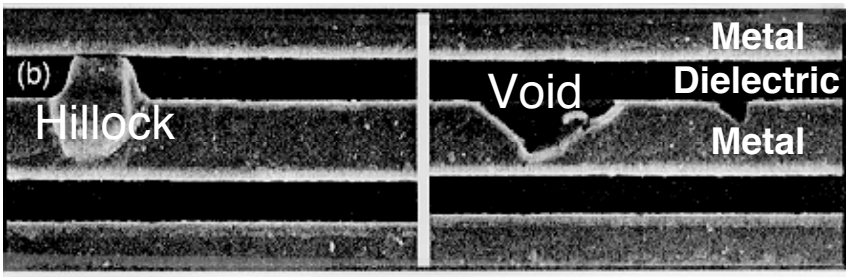
## ELECTROMIGRATION



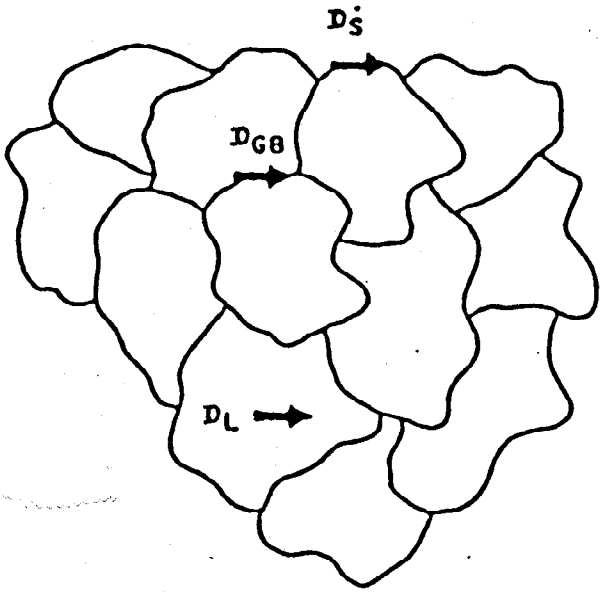
Schematic of a polycrystalline film of a metal layer used for interconnections



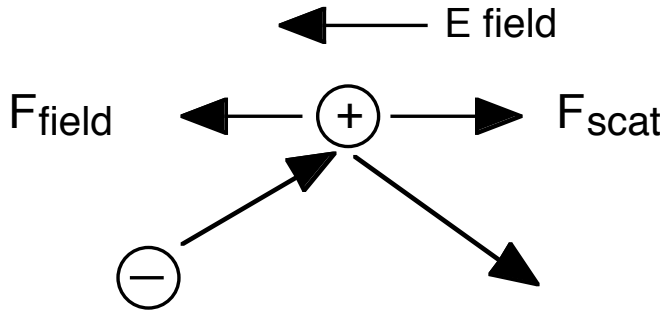

Schematic illustration of electromigration with resultant hillock and void formation. Diffusion of Al through grain boundaries is indicated.




SEM of hillock and voids that have formed due to electromigration in an Al(Cu,Si) line




$D_S$ surface diffusion
$D_{GB}$ grain boundary diffusion
$D_L$ lattice diffusion
For Al $D_{GB} >> D_s$ or $D_L$




**Total force on an atom in a metal film is**

$F_{TOTAL}$ = Scattering force + E-field force

$$= F_{SCAT} + F_{FIELD} \cong qz^* \vec{E}$$

where qz* is effective ion charge and is often negative due to the dominance of $F_{SCAT}$. The drift velocity of the atom is

$$\upsilon_D = \mu \vec{\mathrm{E}}$$

$$= \frac{qZ^*}{kT} \cdot D \cdot \vec{E} \qquad \text{using Einstein's relation}$$

Since current density is related to $\vec{E}$ by

$$J = \sigma \vec{E} = \frac{\vec{E}}{\rho}$$

And diffusivity is in general given by

$$D = D_O \, e^{-\frac{Ea}{kT}}$$

$$\upsilon_D = J \rho \frac{qZ^*}{kT} D_0 \, e^{-\frac{E_a}{kT}}$$

Meantime to failure (MTF) is thus

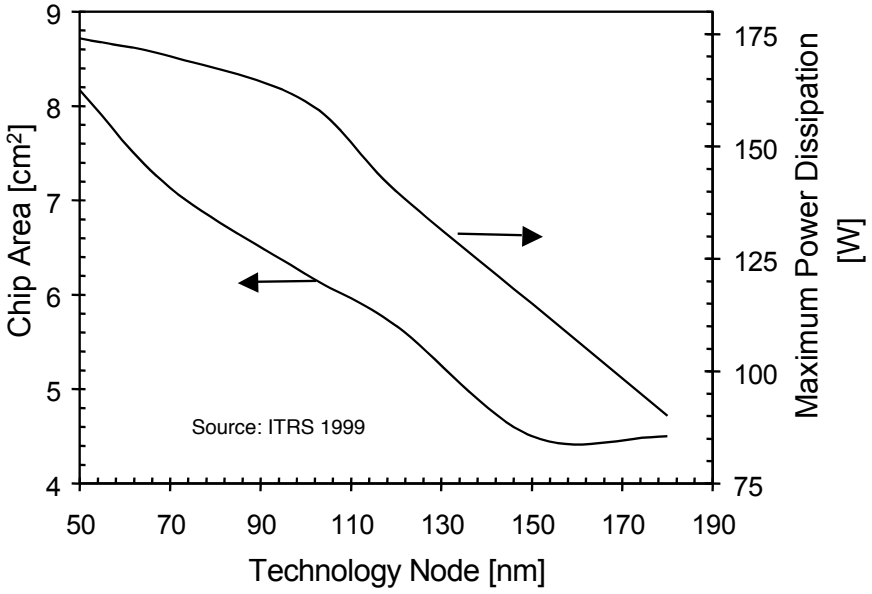
$$MTF \propto e^{Ea/kT}$$

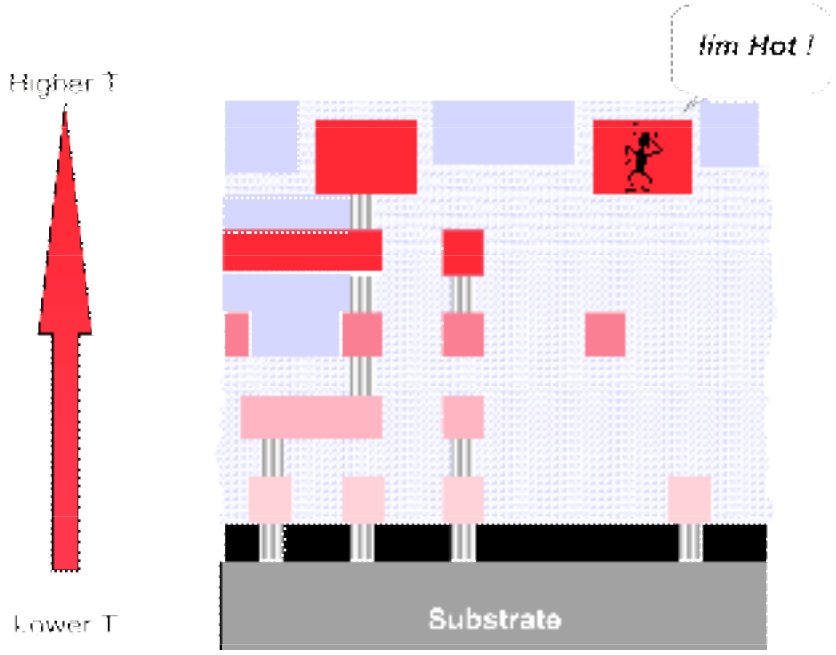
A phenomenological model for MTF is

$$MTF = \frac{A}{\gamma^m J^n} e^{Ea/kT}$$

Where A is a materials related factor, $\gamma$ is the duty factor, m and n are constants and T is the operation temperature. Constant n is generally between 1 and 3

## Thermal Behavior in ICs





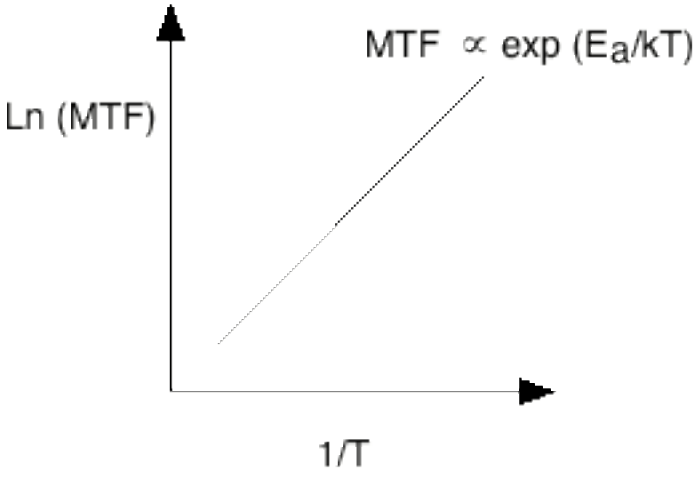

- In addition to the power dissipated by devices there is power dissipation due to interconnects:
  - Joule heating due to $I^2R$ loss
  - Energy dissipated ($CV^2f$) is increasing as performance improves

**Average chip and interconnect temperature is rising**

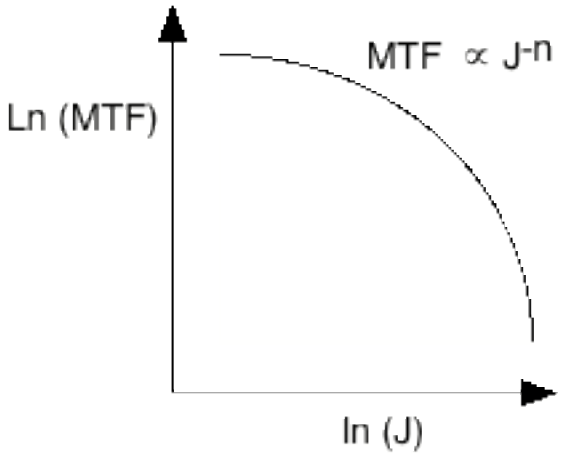
## Parametric Dependencies of Electromigration

$$MTF = \frac{A}{\gamma^m J^n} e^{Ea/kT}$$

Temperature



Current Density




For aluminum n ~ 2 ± 0.5,

The MTBF decreases drastically as temperature and current density is increased. This behavior is used to do accelerated testing. Typically measurements are done at 175-250°C and at a current density around $10^6$ A/cm$^2$

**Materials**

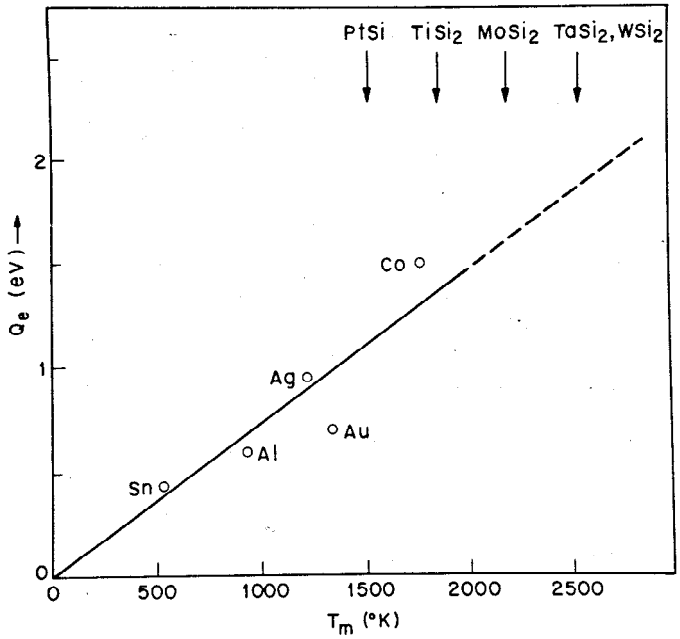



*Figure: Activation energy $Q_e$ of the electromigration in various metals as a function of the melting point of the metals. The straight line has been extrapolated to higher temperatures. Possible electromigration activation energies for silicides are pointed out [original curve from Magro-Campero]*

## Composition

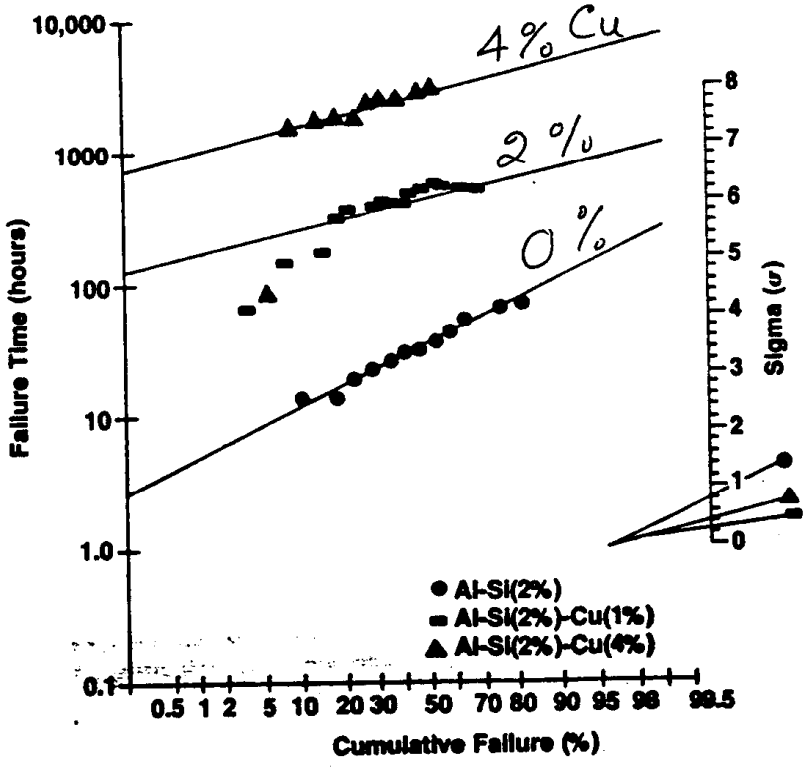



*Figure: Accelerated electromigration life-test plots (log-normal paper) of Al-Si(2%) alloys for different copper concentrations; 0%, 1%, and 4% Cu. Test done at 220°C and a current density of $10^6$ A/cm$^2$. $t_{50}$ is found from the intersection of the 50% cumulative failure line and the straight-line of the data points. (Ref: P. Merchant HP Journal August 1982)*

## Structure

Layered structure: Ti reacts with Al to form $TiAl_3$ which is a very hard material and less prone to electromigration.

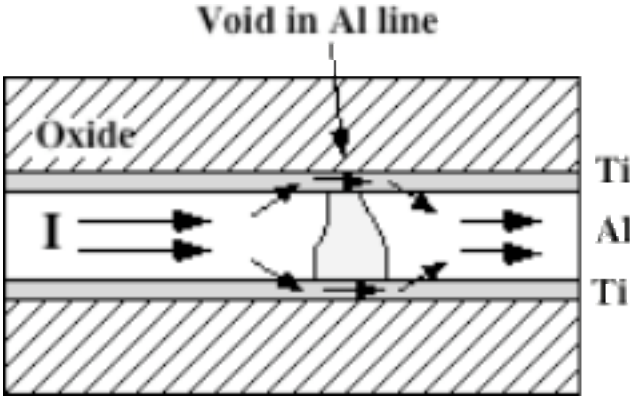



*Figure: Illustration of shunt layers to minimize electromigration problems. Thin layers of metals, such as Ti, are used above and below the Al interconnect line. If a void should form, the current can be shunted around it and through the shunt*

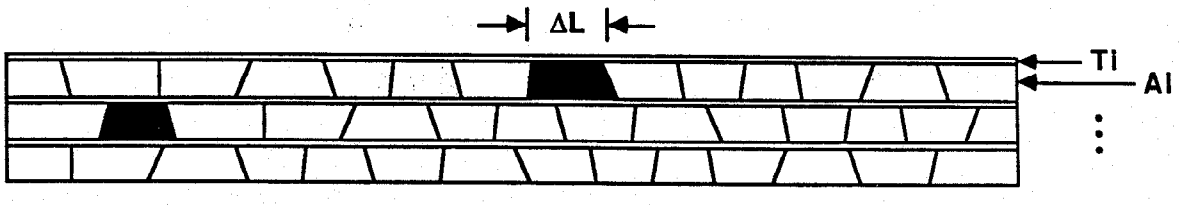



*Fig.: Improvements in layered films as a result of the redundancy. For an open circuit or high-resistance condition to occur, more than one void must coincide.*

Grain Size/Structure:

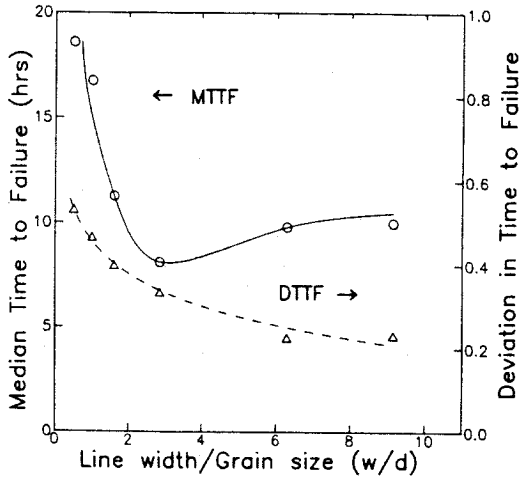
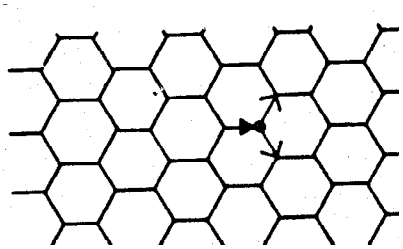



*Figure: The median times to failure (MTTFs) and lognormal standard deviations in the time to failure (DTTFs) for populations of lines with different line width to grain size ratios. (Ref: Cho and Thompson, Appl. Phys. Lett. Vol. 54, 1989, p. 2117)*

Since electromigration occurs via diffusion along grain boundaries, one might expect that as 1/d decreases (i.e. the grain size increases), the metal diffusion would decrease since there are less fast diffusion paths available. This would result in a higher MTTF as 1/d decreases. And as the line width, w, decreases, one might expect that there is more chance for a void to span across the whole line resulting in an open circuit. This results in a lower MTTF as the w decreases. These two trends would both be fairly linear relationships, yet in opposite directions.

## Microstructural Inhomogeneities in the Films and Stress Induced Electromigration

As atoms move in one direction, vacancies move in the opposite direction. The atomic flux and the vacancy flux can converge at certain places in the films giving rise to hillocks and voids respectively. This could happen due to structural inhomogeneties, for example. Eventually this leads to failure through open circuit (void) or short circuit (hillock).



Flux divergence at a triple point in a uniform grain size textured film. On an average the flux should be uniform throughout the film. If the grain size is non uniform the flux will vary accordingly.

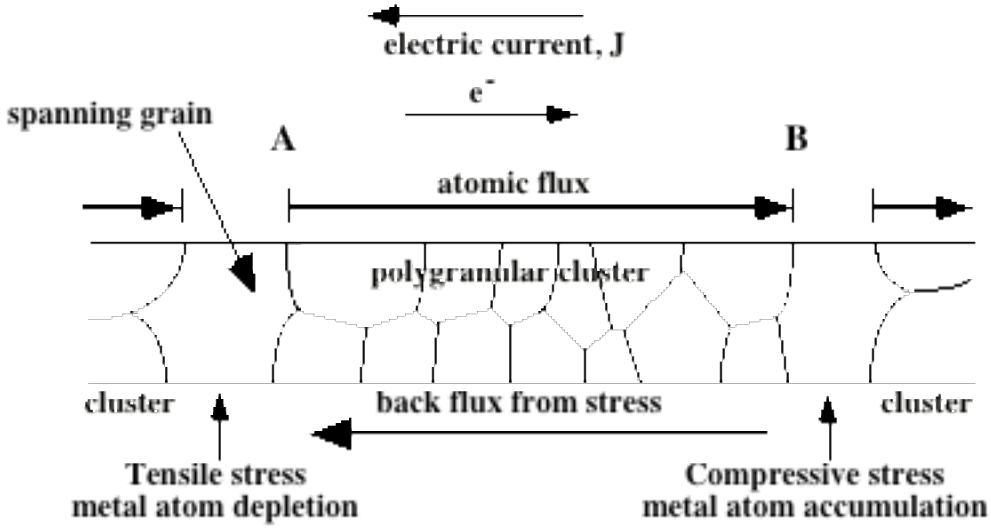
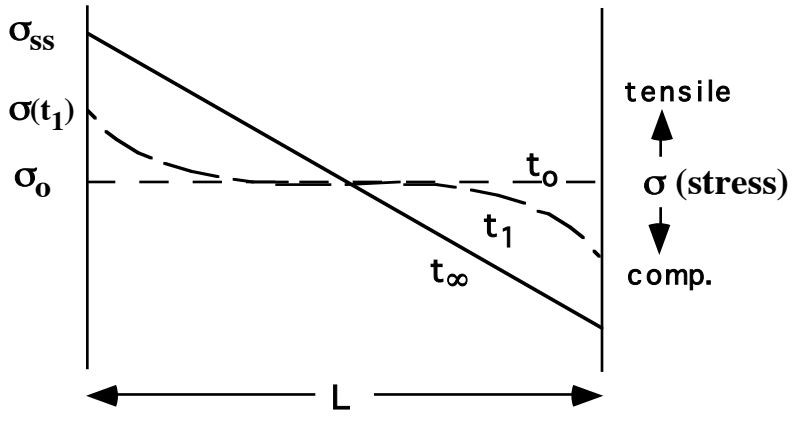
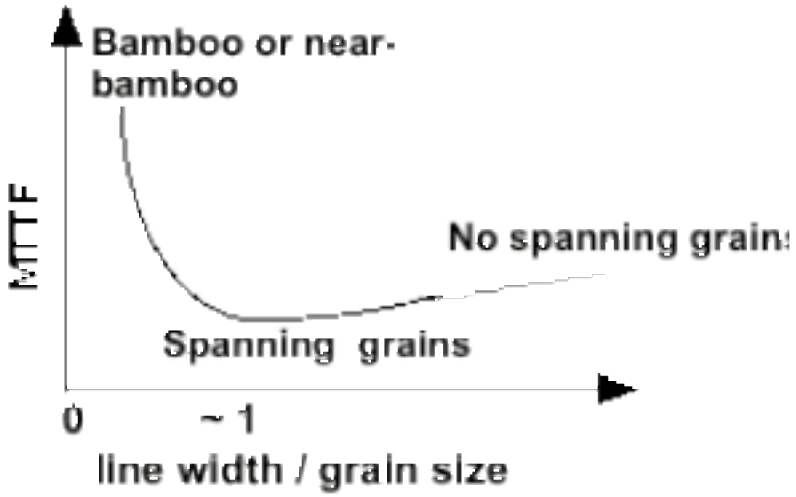



Illustration of polygranular cluster, the region between spanning grains. It is in these regions that the Al diffusion is high due to the high diffusivity paths along the grain boundaries. A divergence of atomic flux will occur at the ends of polygranular clusters, causing metal atom depletion at point A and metal atom build-up at point b. There is stress build-up due to depletion and accumulation of the metal atoms at the ends of the region. This stress causes a back flux of the metal atoms which opposes the flux due to electromigration. [Source; Carl Thompson, MIT]



Schematic illustration of build up of stress within polygranular cluster with time due to electromigration. In the graph, stress ($\sigma$) is plotted versus distance along the cluster of length L for various times. Positive stress is tensile stress, and negative stress is compressive stress. Eventually (as $t \rightarrow t_\infty$), a steady-state is approached where the forward flux is equal to the backward flux due to stress. [Source; Carl Thompson, MIT]
A criterion for failure of an interconnect under electromigration conditions could be if the steady-state stress is equal to or greater than some critical stress for plastic deformation, encapsulent rupture, large void formation, etc. The maximum steady state stress would occur at x=0 or x=L




For very large line width/grain size (w/d) values, no spanning grains are present. No points of flux divergence are present and the time to failure is relatively high. But as w/d decreases, some spanning grains occur. This results in divergences in the flux, causing stress to develop that can be greater than the critical stress for failure (with $L > L_{crit}$ for most or all of the polygranular clusters). The lines would fail and the median time to failure would decrease. Now as w/d decreases more, more spanning grains are present, but the lengths of the polygranular cluster regions between them are shorter, many of them shorter than $L_{crit}$. The stresses that develop, which create the back fluxes and which in turn eventually stop the electromigration flux, are in many cases smaller than the critical stress. For small enough values of w/d bamboo or near-bamboo structures are present. The polygranular clusters are few, and for some lines, all the clusters are shorter than $L_{crit}$ and the lines will not fail by this mechanism. The MTTF thus increases dramatically.

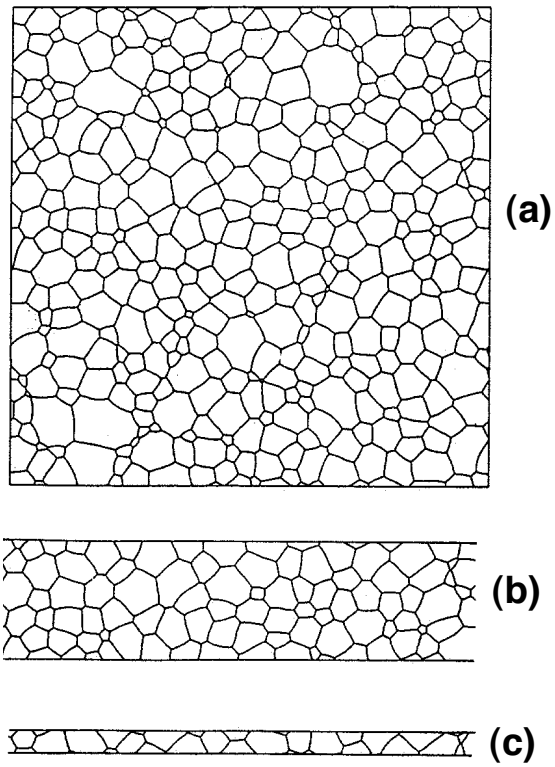



*Figure (a) Top view of a thin-film grain structure. (b) A wide line with width w greater than the line average grain diameter, d, has continuous grain boundary paths along the line for diffusion. (c) When w is less than or about equal to d, the grain-boundary circuit is interrupted.*

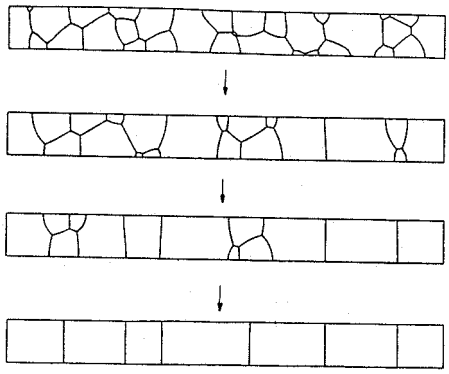



*Figure Effect of post patterning annealing on the grain structure of the film. With sufficient grain boundary migration a "bamboo structure" may develop.*

Texture: The texture of the polycrystalline film also impacts electromigration, e.g., <111> orientation in Al as well as Cu shows higher MTBF.

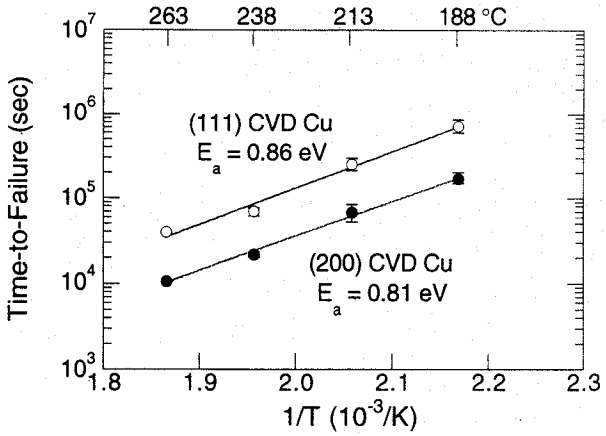



*Fig: Arrhenius plot of time-to-failure of Cu thin films (J = 8 mA/cm$^2$). (Ref: Ryu, Loke, Nogami and Wong, IEEE IRPS 1997.)*

There are several other factors, such as, topology, passivation layers above and below, stress current (AC vs. DC), etc. which also affect electromigration.

## Hillocks:

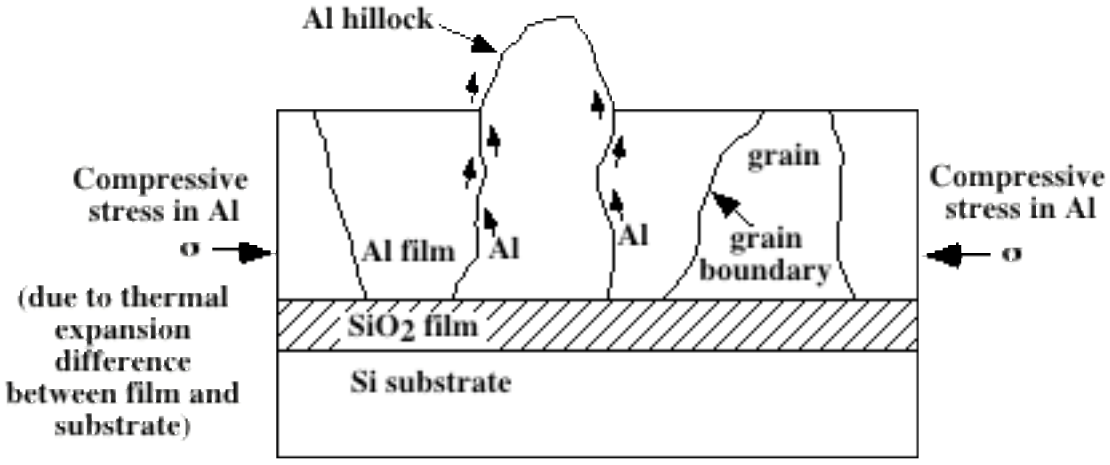



*Fig. Schematic illustration of hillock formation due to compressive stress in an Al film. Al diffusion along grain boundaries is indicated.*

In a multilevel interconnection scheme the hillocks can cause shorts between the layers of metal. Since Al is a low temperature metal in comparison with Cu, W, etc., it suffers with this problem much more.

Hillocks are formed during the heating and cooling cycles generally encountered during the deposition of interlayer dielectric films. They are attributed to:

- Stress
- Plastic deformation
- Enhanced grain boundary diffusion

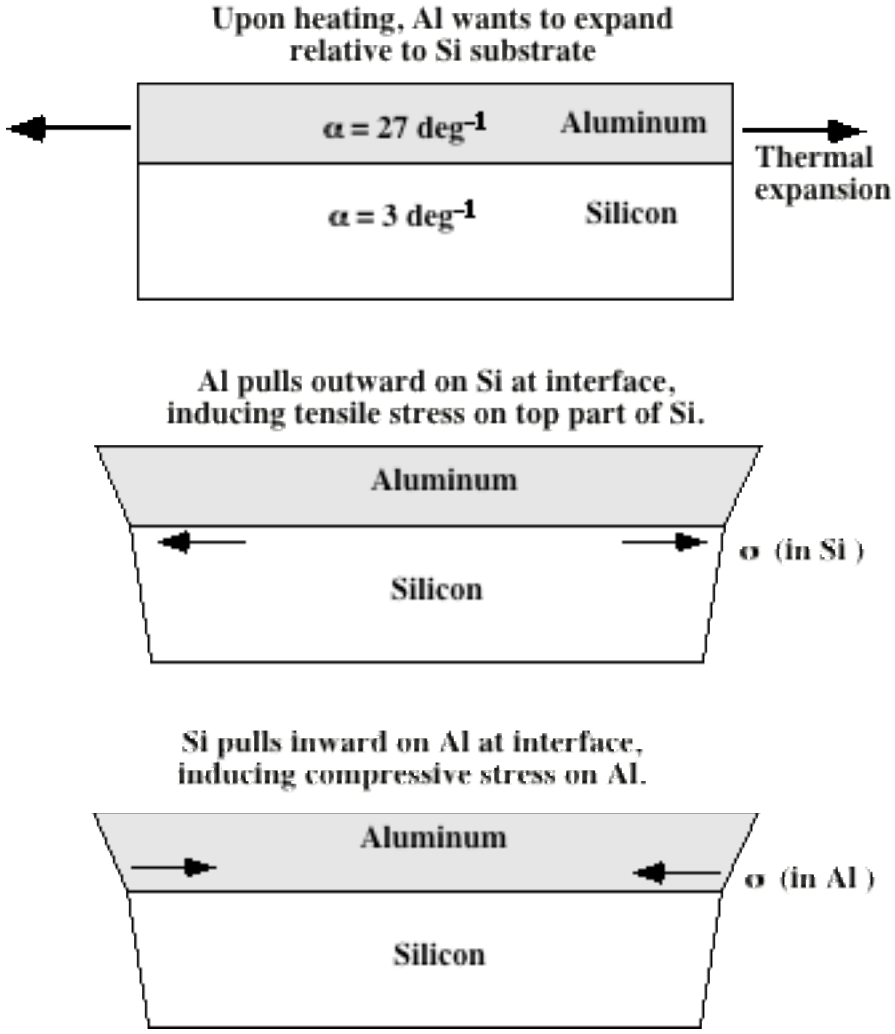



*Fig.: Difference in the linear expansion coefficients of the film and substrate causing stress in the thin film. (a) Film as-deposited (stress free). (b) Expansion of the film and substrate with increasing temperature. (c) Biaxial forces F compress the film to the substrate dimension.*

## Thermal Cycling Induced Stress

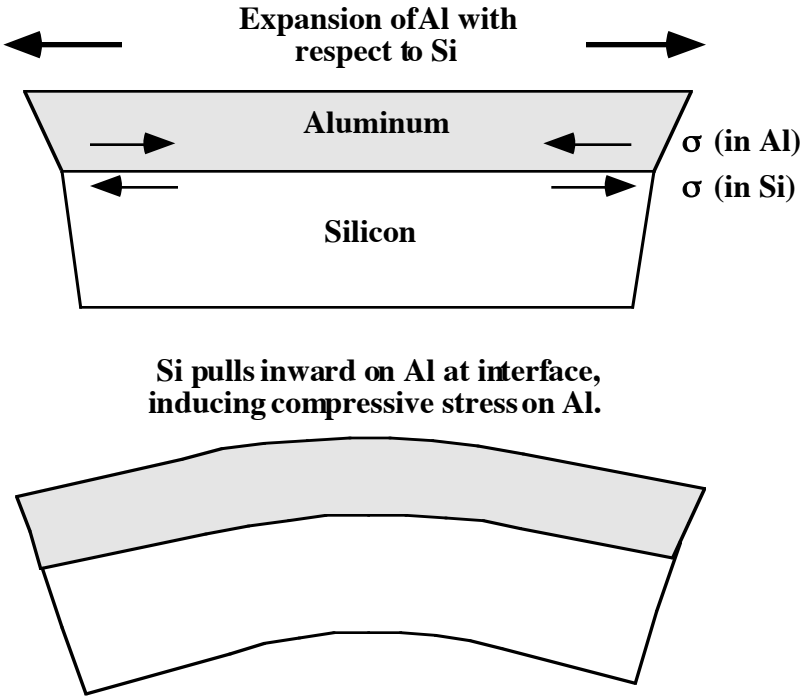



*Fig.: The stresses that develop due to thermal expansion differences, leading to bending of the entire structure. The amount of bending, measured by the radius of curvature, can be used to determine the stresses present in the thin film.*

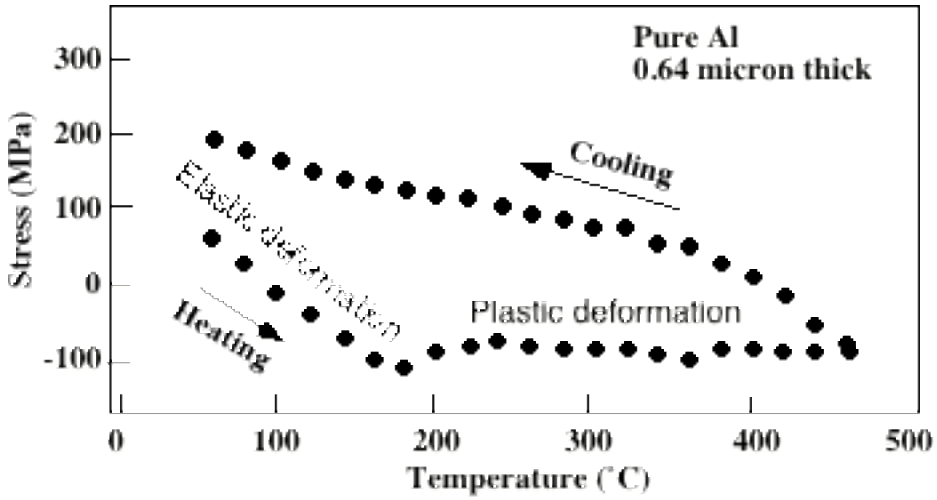
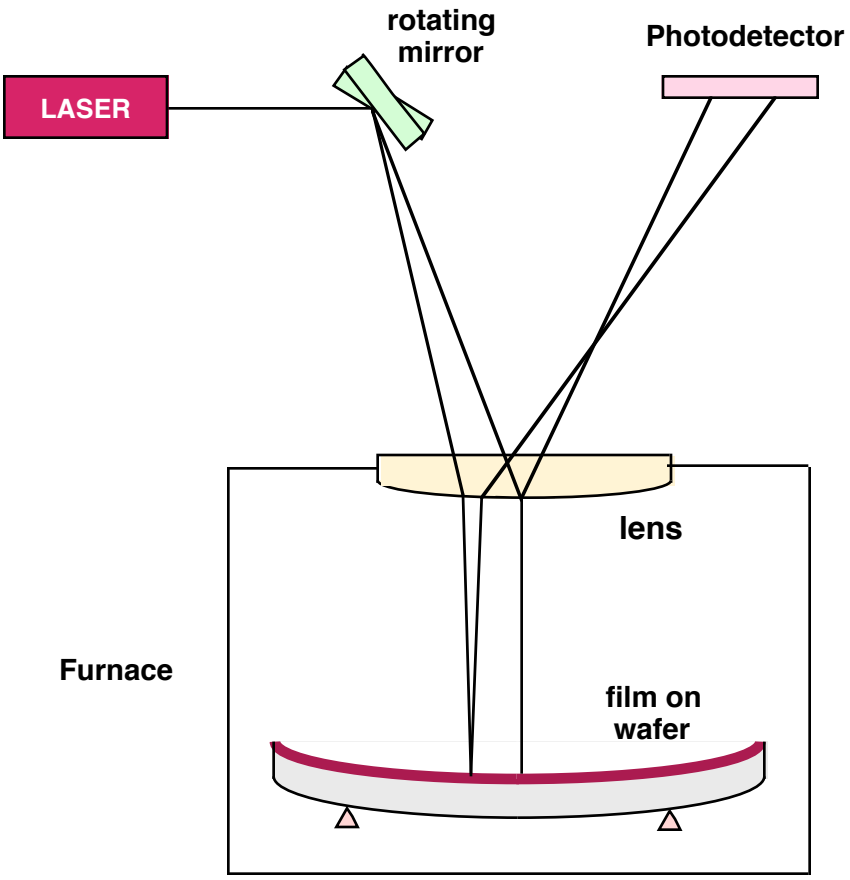



*Figure: Stress-temperature curve of 0.64 μm thick Al film on $SiO_2$..*




Schematic diagram of wafer curvature measuring apparatus.

$$\sigma = \left(\frac{E_s}{1-\nu_s}\right)\left(\frac{t_s^2}{6 t_f R_f}\right)$$

where $(E_s/1-v_s)$ is the biaxial modulus of the substrate, $t_s$ is the substrate thickness, $t_f$ is the film thickness, and $R_f$ is the radius of curvature induced by the film.

Since melting point of Al is low (660°C) plastic deformation takes place at fairly low temperatures relieving the stress.

Table. Mechanical properties of interconnect materials.

| Material | Thermal expansion coefficient (1/˚C) | Elastic modulus, Y/(1-ν) (MPa) | Hardness (kg/mm2) | Melting point (˚C) |
|---|---|---|---|---|
| Al (111) | $23.1 \times 10^{-6}$ | $1.143 \times 10^{5}$ | 19-22 | 660 |
| Ti | $8.41 \times 10^{-6}$ | $1.699 \times 10^{5}$ | 81-143 | 1660 |
| $TiAl_3$ | $12.3 \times 10^{-6}$ | - | 660-750 | 1340 |
| Si (100) | $2.6 \times 10^{-6}$ | $1.805 \times 10^{5}$ | - | 1412 |
| Si (111) | $2.6 \times 10^{-6}$ | $2.290 \times 10^{5}$ | - | 1412 |
| $SiO_2$ | $0.55 \times 10^{-6}$ | $0.83 \times 10^{5}$ | - | ~1700 |

Refractory metals like Ti, W, V form compounds with Al which are very hard and melt at much higher temperatures than Al. As a result hillock growth is minimized. At the same time electromigration is also reduced.

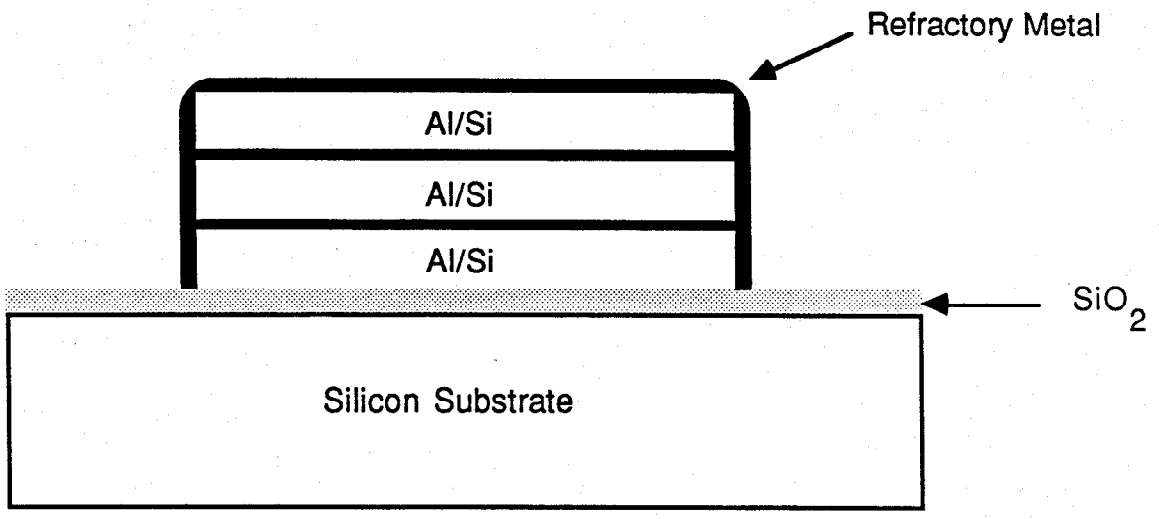
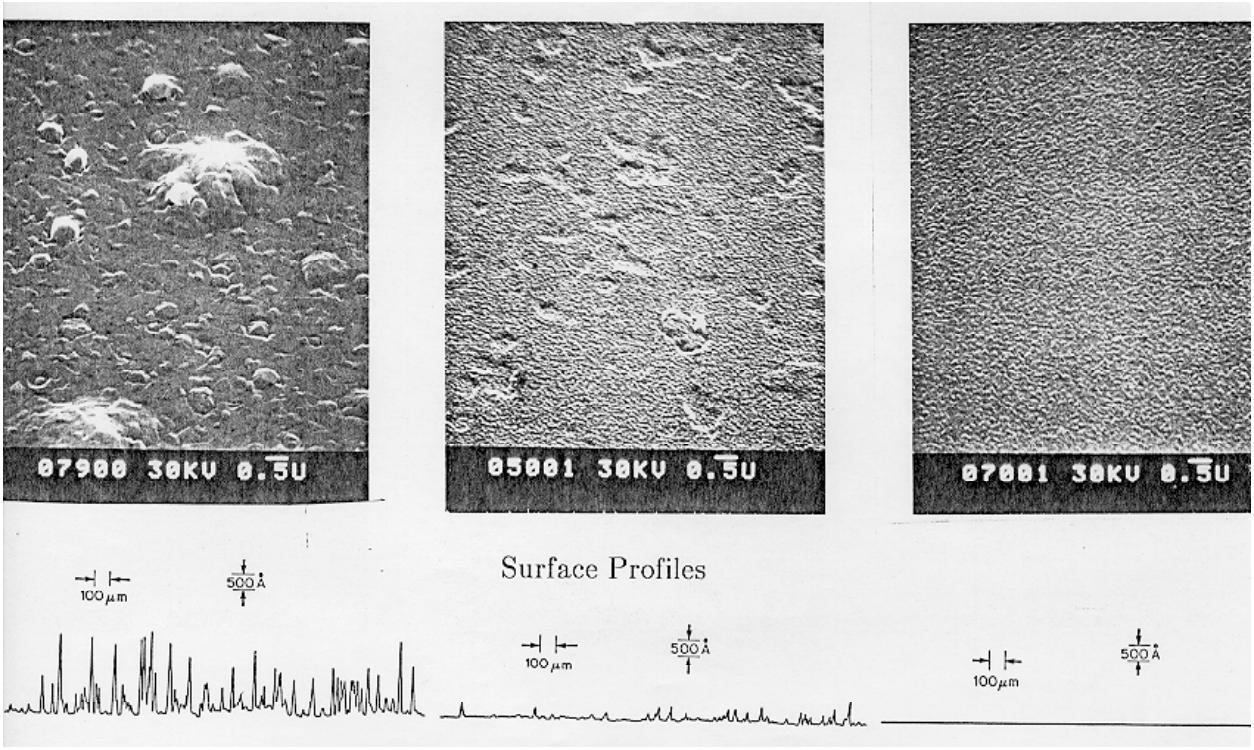
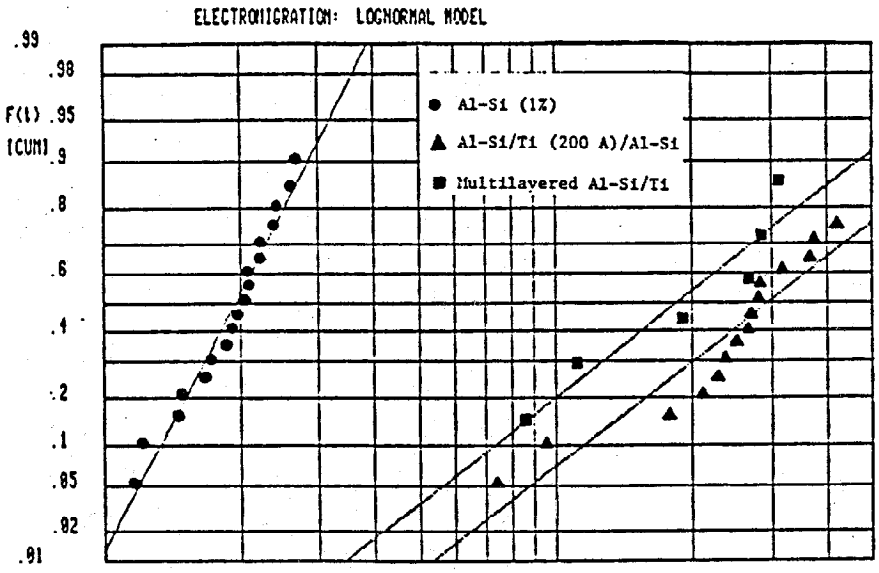


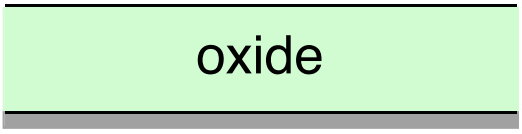

*Figure: Encapsulated multilayer interconnection. The encapsulation, formed by first depositing and then anisotropically etching the material, prevents potential lateral hillocks from forming. Such hillocks have been observed in single layer structures during the later part of the life of the interconnection. The multilayers provide the redundancy leading to greater reliability; fewer layers can be used if the deposition equipment is inadequate. A reduction in hillocks and improved MTF would still result. (Gardner, Ph.D. Thesis, Stanford University, 1987)*
*layers.*


07900 30KV 0.5U
05001 30KV 0.5U
07001 30KV 0.5U
Surface Profiles
100 μm
500 Å
100 μm
500 Å
100 μm
500 Å

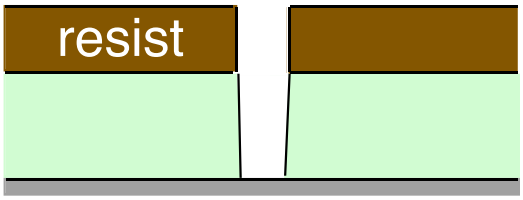

ELECTROMIGRATION: LOGNORMAL MODEL
.99
.98
F(t) .95
(CUM) .9
.8
.6
.4
.2
.1
.05
.02
.01
Al-Si (1%)
Al-Si/Ti (200 A)/Al-Si
Multilayered Al-Si/Ti
Time (arbitrary units)

# Current Aluminum Interconnect Technology

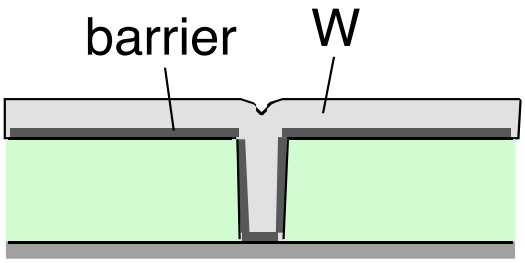
## Fabrication of Vias



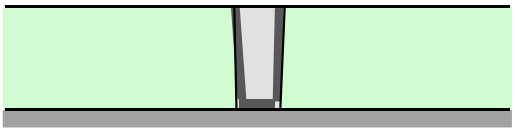

1. oxide deposition




2. via etch

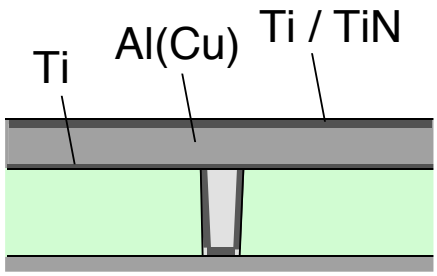



3. barrier & W fill

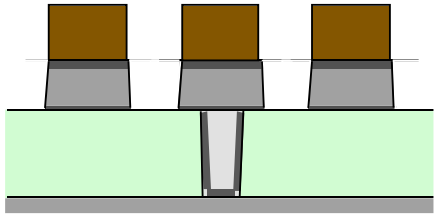


4. W & barrier polish

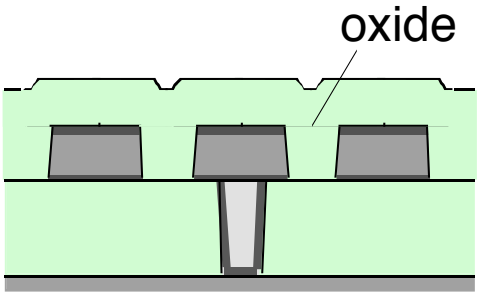
# Fabrication of Lines



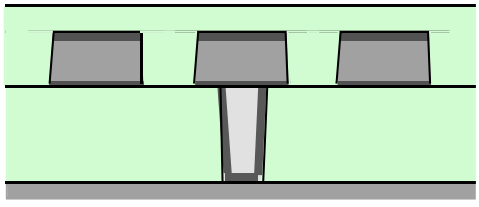

5. metal stack deposition



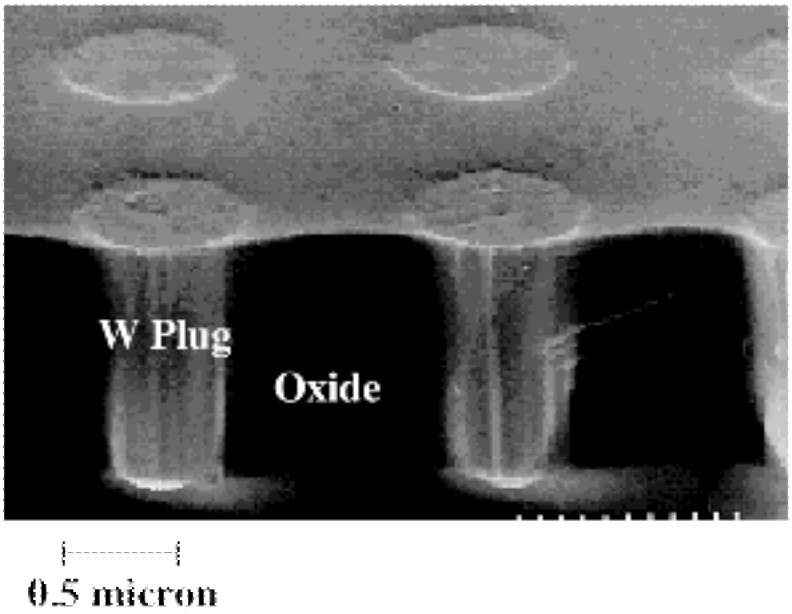
6. metal stack etch




7. oxide gapfill



8. oxide polish




*SEM image of W plugs after blanket CVD deposition and CMP. Photo courtesy of VLSI Technology, Inc.*

## Currently used Al technology

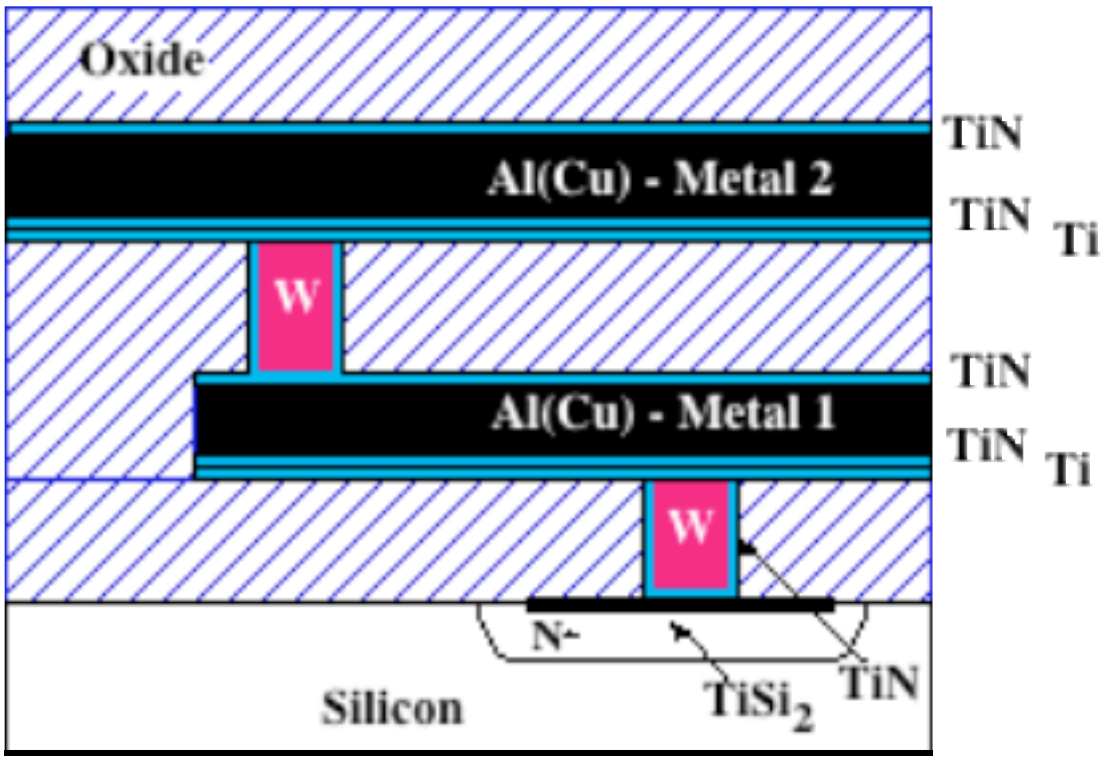
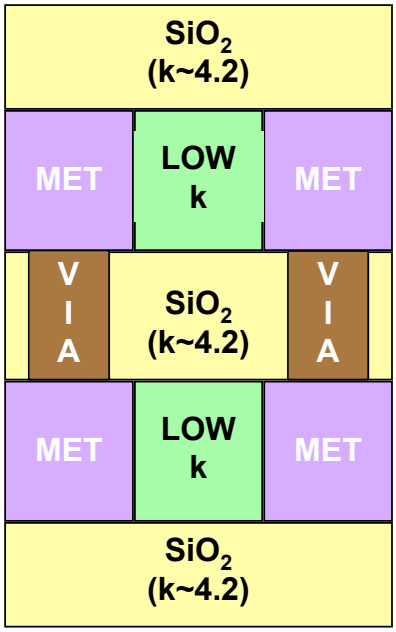



*Fig.: A typical metalization scheme used in current I.C. technology, showing the multi-layer structures that have evolved.*

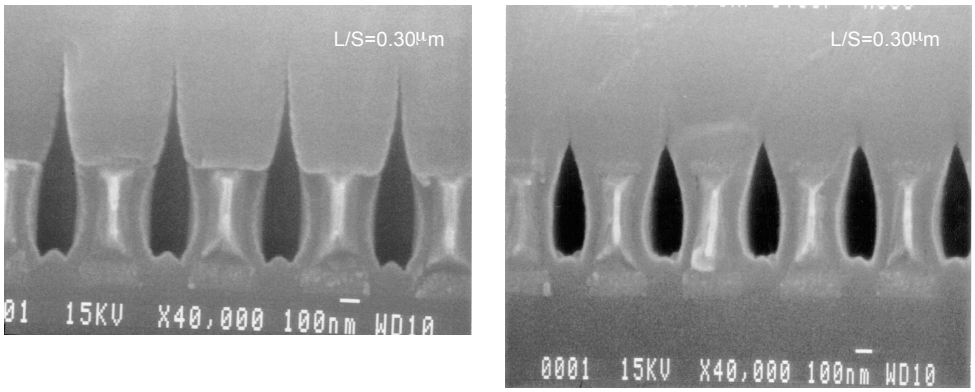
## Embedded Low-k Dielectric Approach




### Why embed Low-k dielectric only between metal lines?

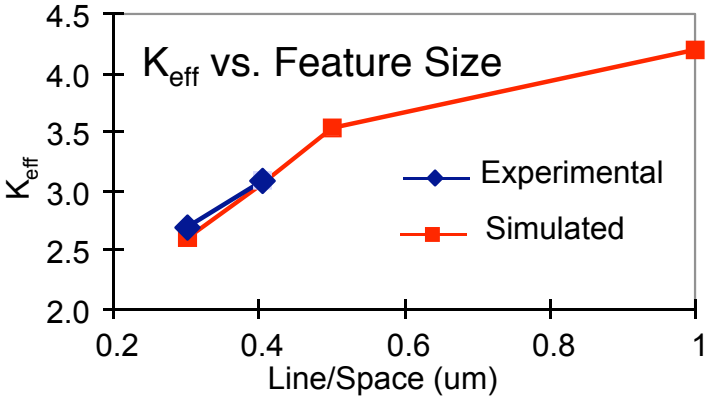
- Mechanical strength
- Moisture absorption in low-k
- Via poisoning/compatibility with conventional dry etch and clean-up processes
- CMP compatibility
- Ease of integration and cost
- Thermal conductivity

## Air-Gap Embedded Low-k Dielectric

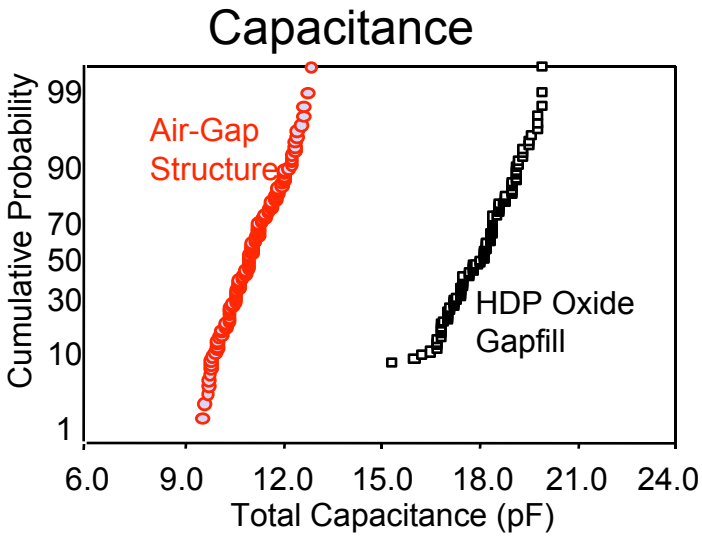



Air-gap size and extension above metal lines can be controlled by varying $SiO_2$ deposition conditions. Both samples were subjected to CMP. (Ref: B. Shieh, L. C. Bassman, D.-K. Kim, K. C. Saraswat, M. Deal, J.P. McVittie, R. S. List, S. Nag, and L. Ting, " Air-Gap Formation During ILD Deposition to Lower Interconnect Capacitance," Proc. IEEE Int. Interconnect Tech. Conf., June 1998, San Francisco, pp. 16-18.)

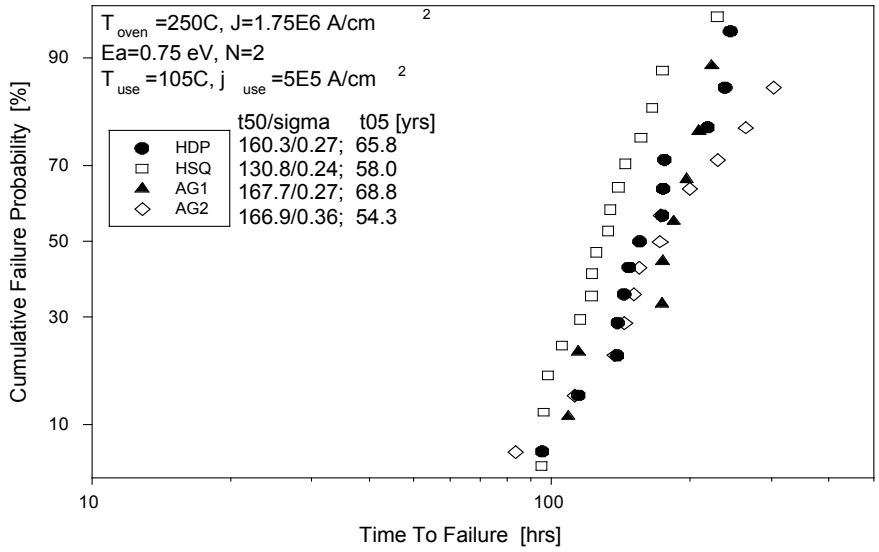
- Reduced capacitance between wires
- Heat carried mostly by the vias
- Electromogration reliability is better because of stress relaxation allowed by free space




$K_{eff}$ vs. feature size using air-gaps between metal lines 0.65$\mu$m tall. For small pitches, $K_{eff}$ drops almost linearly.




Electrical data for air-gaps shows a 40% reduction in capacitance.




Experimental electromigration data showing no significant difference between air-gap samples and HDP oxide gapfill samples.