Ultra Thin (<3 nm) High Quality Nitride/Oxide Stack Gate Dielectrics Fabricated by In-Situ Rapid Thermal Processing

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Abstract

In this paper, ultra thin (< 3 nm) Si_3N_4/SiO_2 stack layer with significant lower leakage current, superior boron diffusion barrier properties, and reliability compared with SiO_2 of identical thickness have been fabricated by in-situ RTP processing. These results demonstrate for the first time that ultra thin LPCVD Si_3N_4 can be used as gate dielectrics, contrary to those conclusions made previously on thicker LPCVD Si_3N_4.

Introduction

The stacked dielectrics of Si_3N_4/SiO_2 (N/O), widely used for DRAMs [1-3], have been suggested as promising gate dielectrics due to its thinner equivalent oxide thickness and more effective suppression of boron penetration in p^+-poly PMOSFETs compared to thermally grown oxide or oxynitrides of identical thickness [4,5]. However, thick LPCVD Si_3N_4 films are known to have higher leakage current, poor masking properties during reoxidation, and inferior hot-carrier reliability [4]. This is largely caused by poor nitride film quality and associated significant charge trapping and larger interface state density. However, LPCVD Si_3N_4 has not been investigated in ultra thin thickness region (direct tunneling) where the ultra thin Si_3N_4 films show much reduced number of traps and enhanced detrapping of trapped charges due to tunneling, both of which contribute to reduced leakage current and improved hot-carrier reliability.

In this paper, ultra thin (< 3 nm) Si_3N_4/SiO_2 stack layer with significant lower leakage current, comparable to JVD nitride [6], and superior boron diffusion barrier properties and reliability compared with SiO_2 of identical thickness have been fabricated by in-situ RTP processing.

Experiment

Both n^+-poly NMOS and p^+-poly PMOS capacitors were fabricated. The entire N/O stack films were formed by RTP. The bottom oxide (6 - 7 Å) is grown in NO at 800 °C for 20 sec. Si_3N_4 films (1.5 - 2 nm) were deposited using SiH_4 and NH_3 at the ratio of SiH_4/NH_3 = 1/40 at 800 °C, 1 Torr. RTP NH_3 anneal (950 °C - 1000 °C, 30 sec. in pure NH_3) is performed on some samples after nitride deposition. All samples received a RTP N_2O post-deposition anneal (850 °C, - 900 °C, 30 sec.). $POCl_3$ doping is used for n^+-poly gate NMOS and BF_2-implanted poly (50 keV, $5x10^{15}$ dose) is used for p^+-poly PMOS. The amount of boron penetration is varied by changing the RTA drive-in conditions for p^+-poly PMOS capacitors. For comparison, identical thickness of SiO_2 and oxynitrides (N_2O, NO) grown by RTP are prepared. Oxide equivalent thickness (T_{eq}) is extracted from high frequency C-V curve in strong accumulation region (-2.5 V for NMOS, +2.5 V for PMOS). Quantum mechanical effects are not taken into account in oxide thickness determination.

Interface Property and Hysteresis

A high quality bottom oxide is necessary for N/O stack layer to have good interface property. However, for ultra thin N/O stack layer, the bottom oxide must be very thin. As shown in Fig. 1, the quasi C-V curve of Si_3N_4 device without the interfacial oxide is distorted severely due to large amount of interface state densities. An ultra thin oxynitride passivation layer (~6 -7 Å) grown by RTP in NO at 800 °C, 20 sec provides excellent interface property for N/O stack layer, which is as good as that of thermal oxide of identical thickness, t_{eq} ~5 nm. It is worth noting that NH_3 post-nitride deposition anneal does not degrade interface property of the N/O stack layer. Hysteresis of the C-V characteristics of the N/O stack film is evaluated with the amount of flatband voltage shift between two different sweep directions in high frequency C-V curve. As the film thickness is reduced to ~2.5 nm, the amount of hysteresis is decreased to few mV range, as shown in Figs. 2, 3. Although NH_3 post anneal induces more hysteresis in thicker film as shown in Fig. 3, however, as the film thickness is reduced, the effect of NH_3 post anneal on the hysteresis becomes much less. It is worth noting that the hysteresis of C-V characteristics is very small (few mV) for ultra thin N/O stack layers (Fig. 2).

Leakage Current and Reliability

For thick N/O stack layers (5 nm), the leakage current is higher than thermal oxide, and NH3 post-deposition anneal has little effect in reducing it, as shown in Fig. 4. As the Si_3N_4 film thickness is reduced to the region where direct tunneling dominates (2.4 nm), the N/O stack films show lower leakage current than thermal oxide by several orders of magnitude, as shown in Fig. 5, particularly in NH_3-annealed Si_3N_4. The use of NH_3 post-deposition anneal reduces the leakage current significantly in ultra thin nitride films. The as-deposited nitride film tends to be Si-rich (as shown by XPS results in Fig. 6), contains lots of traps, and can be oxidized easily during reoxidation (Fig. 6). The NH_3 anneal can convert the as-deposited Si-rich nitride film to be more stoichiometric (XPS results in Fig. 7) and increase its oxidation resistance significantly by incorporating more N into the films (Fig. 8). It also reduces the trap-assisted tunneling current considerably (Fig. 5). As shown in Fig. 9, the NH_3 annealed N/O stack film has much lower leakage current than thermal oxide and oxynitride films grown in NO or N_2O ambient in the direct tunneling region. The NH_3 anneal also increases TDDB lifetime and reduces charge trapping significantly under constant voltage stress due to reduced trap densities and lower leakage current, as shown in Figs. 10, 11. The t_{BD} of the N/O stack film with NH_3 post anneal is similar to that of control oxide of identical thickness (2.5 nm).

Boron Penetration

The N/O stack film without NH_3 anneal shows slightly more boron penetration than oxynitride film grown in nitric oxide ambient (1050 °C, 100 sec.), as shown in Fig. 12 due to its Si-rich film characteristics. However, the NH_3 annealed N/O stack sample shows almost no boron penetration (Fig. 12). This is due to the formation of more denser films associated with stoichiometric Si_3N_4 (Figs. 7, 8), which reduces boron diffusion effectively. Boron penetration-induced low field leakage current is also suppressed considerably by NH_3 anneal, as shown in Fig. 13.

Conclusion

The N/O stack film is compared with other films in direct tunneling region. NH_3 annealed N/O stack film shows several orders of magnitude lower leakage current than SiO_2, improved device lifetime, and complete suppression of boron penetration. These results demonstrate for the first time that ultra thin CVD Si_3N_4 can be used as gate dielectrics, contrary to those conclusions made previously on thicker CVD Si_3N_4. The N/O stack film can be used as a gate dielectric for next generation dual gate CMOSFETs.

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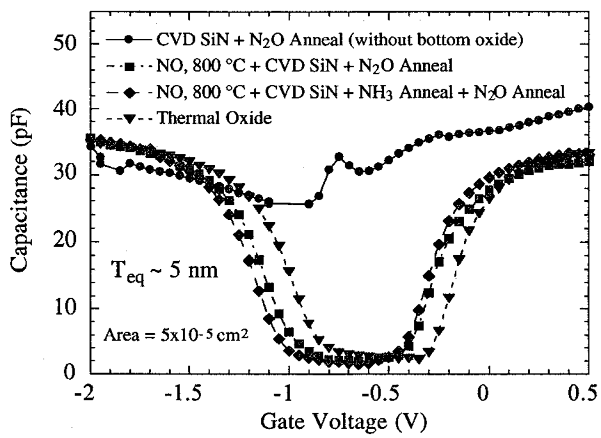

Fig. 1 The interface property of the N/O stack film with different bottom oxide and post anneal conditions.

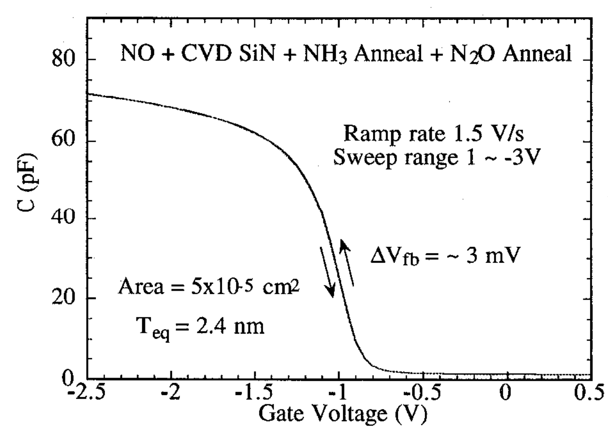

Fig. 2 The hysteresis of the C-V characteristics of the N/O stacked film with NH_3 post anneal.

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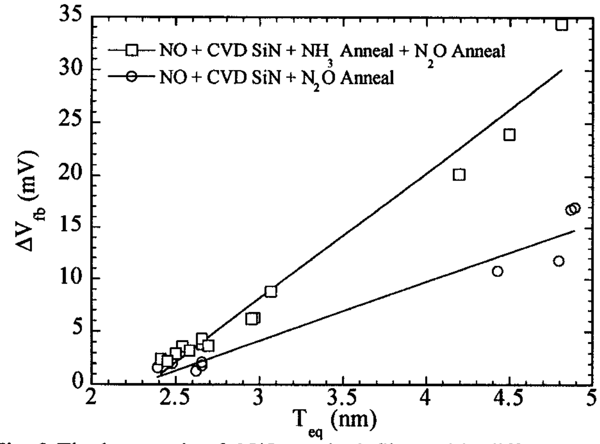

Fig. 3 The hysteresis of N/O stacked films with different post anneal conditions. Sweep rate: 1.5 V/s, Sweep range: 1 ~ -3 V.

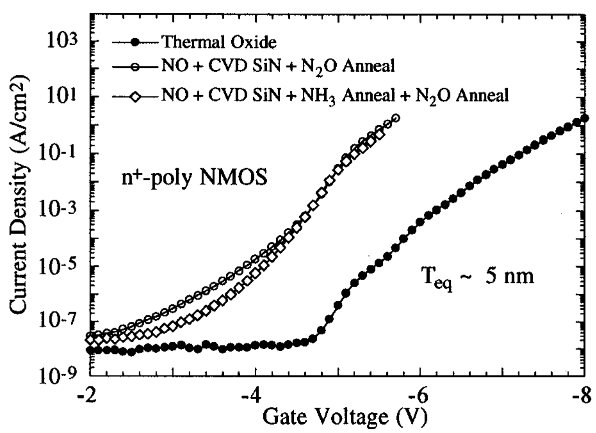

Fig. 4 J-V characteristics of different dielectric films (t_{eq} = 5 nm).

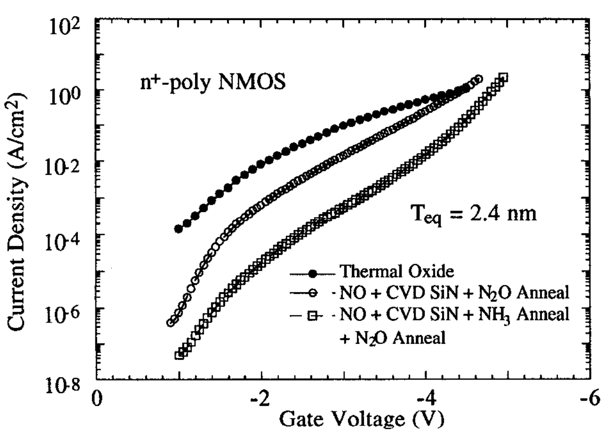

Fig. 5 J-V characteristics of different dielectric films (t_{eq} = 2.4 nm).

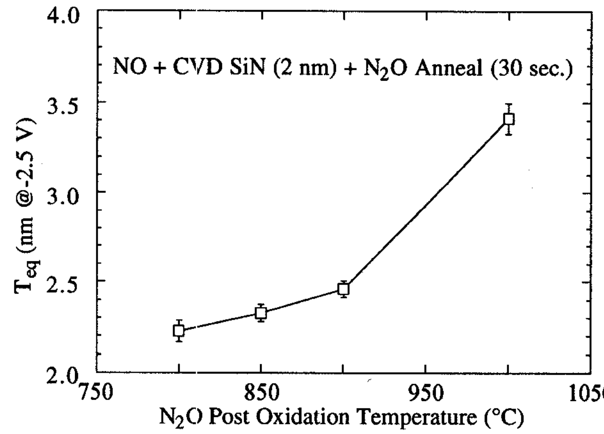

Fig. 6 Equivalent oxide thickness of the N/O stack film for different N_2O post oxidation temperature.

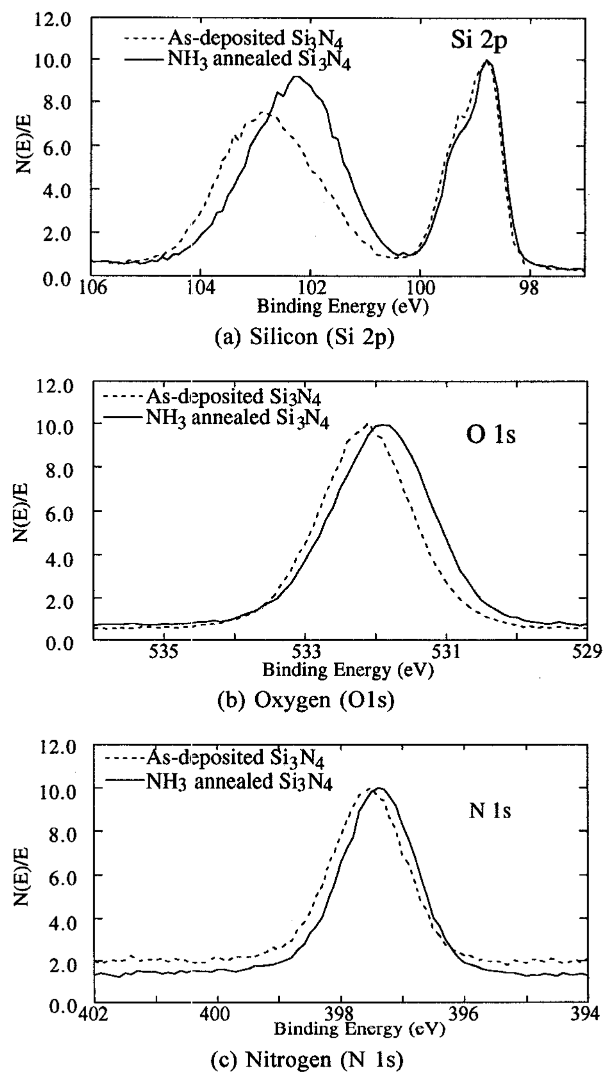

Fig. 7 XPS spectrum of nitride films before and after RTP NH_3 anneal (950 °C, 30 sec.).

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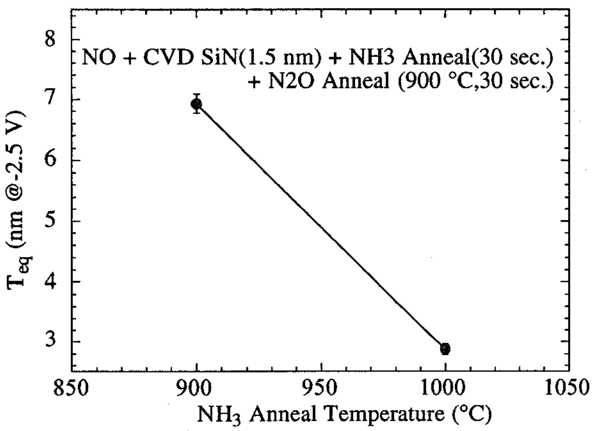

Fig. 8 Effects of RTP NH_3 anneal on oxidation resistance ability of CVD nitride.

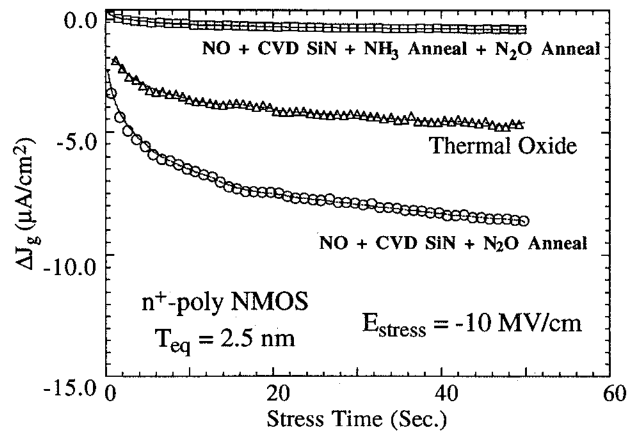

Fig. 11 Charge trapping properties of the N/O stack films under constant field stress.

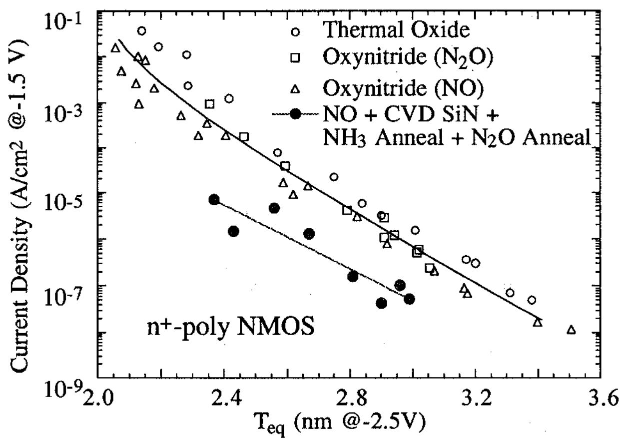

Fig. 9 Leakage current density comparison of dielectric films.

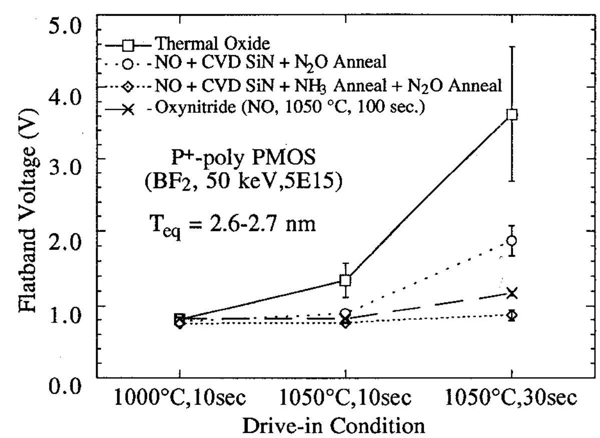

Fig. 12 Comparison of boron diffusion barrier properties.

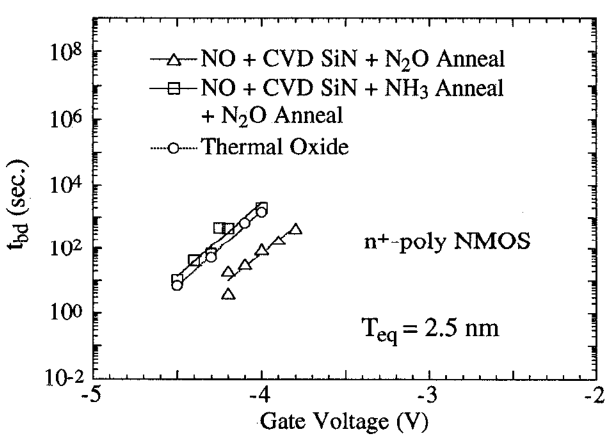

Fig. 10 Effects of NH_3 anneal on the reliability of the N/O stack film.

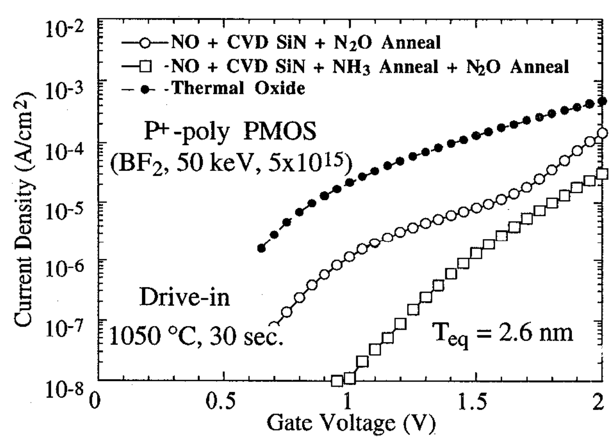

Fig. 13 Boron penetration induced low field leakage current.

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