Local Oxidation Of Siliconfor Isolation

Peter Smeys, Chapter 2, PhD Thesis, Stanford University, 1996

The need for a reduction of the spacing between devices in integrated circuits has led to the development of several device isolation process schemes. In this chapter, we give an overview of the most important trends in isolation technologies, starting with the conventional LOCOS structure. A novel isolation structure that combines several of the features used in advanced isolation structures is demonstrated and is used to investigate the trade-offs between the process steps that lead to a reduction in active area loss and the electrical performance of the isolation structure in terms of junction leakage.

2.1 Introduction

Before the invention of the planar technology [2.1], transistors and diodes were usually fabricated as mesa structures. Surface leakage currents were a big problem in these devices however. The discovery by Atalla et al. [2.2] that a thermally grown oxide on silicon could dramatically reduce the leakage current by passivating the surface, led directly to the development of the first fundamental oxide isolation structure for integrated circuits, the planox process [2.3]. A breakthrough in the field of isolation technology came in 1970 when Appels et al. [2.4] realized that Si$_3$N$_4$ was resistant to oxidation. They applied this concept to selectively oxidize silicon and develop the ‘Local Oxidation of Silicon’, or LOCOS, process to electrically isolate devices.

The concept of the conventional LOCOS isolation structure is illustrated in figure 2.1. After growing a thin oxide (10-20 nm), a layer of LPCVD Si$_3$N$_4$ (100-200 nm) is deposited. The nitride is then patterned to form the active device regions. Because the Si$_3$N$_4$ is resistant to oxidation, oxide will only grow in those regions that have no nitride present. Before growing the field oxide, boron is implanted (1×10$^{13}$ - 4×10$^{13}$ cm$^{-2}$) into the p-well field regions in order to assure an acceptable field threshold. The field implantation can generally be omitted in advanced CMOS processes where either a retrograde p-well is used or the p-well is formed after field oxidation (see 2.2.1.1). Subsequently the field oxide is grown, usually in a steam ambient at temperatures above 950 °C to allow stress-relief by viscous flow of the oxide. The isolation structure is completed by stripping the Si$_3$N$_4$ film in hot (150 - 175 °C) H$_3$PO$_4$ and the pad oxide in a buffered HF solution. Because the final field oxide protrudes significantly above the silicon substrate, this process is often referred to as the semi-recessed LOCOS. When a shallow trench is etched in the silicon before the field oxidation, a fully-recessed LOCOS results. The difference between these structures is illustrated in figure
2.1 Introduction

2.2. In the fully-recessed structure, most of the field oxide is completely below the original silicon surface, hence the name. This class of isolation structures will be discussed in more detail in section 2.2.2.

The ability to locally oxidize silicon is the essential part of any isolation structure. Over the years several alternatives to the conventional LOCOS technology have been proposed in the literature. Most of them however have been rejected over time, and only a limited num-

FIGURE 2.1: Local oxidation of silicon (LOCOS) process sequence.

FIGURE 2.2: Illustration of the difference in shape and topography in a semi-recessed and fully-recessed locos structure.
ber are in use at present. Through innovative modifications to the basic oxidation masking stack, the applicability of LOCOS and some of its derived schemes has been successfully extended to sub 0.5 \( \mu \)m technologies and it is still being considered for 256 Mbit dynamic memory processes and beyond (active area pitch of 0.6 \( \mu \)m) [2.5]. The general trend in isolation structure design has been to make modifications to the composition of the active area masking stack, either by changing the properties of the mask layers or by using sidewall spacers and other fancy schemes. Modifying the properties of the growing field oxide in order to influence the characteristics of the isolation structure is a very attractive way to reduce the encroachment but to date, the only way this has been done is by increasing the oxidation temperature. It should be pointed out that even though LOCOS may still be a viable technology for certain applications there is a clear trend to switch to more advanced isolation processes such as shallow trench isolation, especially in high density digital applications.

Device isolation is one of the process modules that severely limits the packing density in ULSI processes. Hence a fundamental understanding of the parameters that influence the LOCOS shape and its interaction with device structures is essential in order to be able to predict the scalability limits of this technology. In the following paragraphs an overview of the evolution of the integrated circuit isolation process is discussed and results of an experimental and theoretical investigation of the scalability limits of LOCOS are presented.

2.2 Isolation structures

2.2.1 Conventional Semi-Recessed LOCOS

The processing steps needed to fabricate a LOCOS isolation structure have been described in the previous section. In this section, we will discuss processing and device issues associated with fabricating LOCOS isolation structures.

2.2.1.1 Electrical isolation issues

The primary purpose of any isolation structure is to electrically isolate devices from one another. As illustrated in figure 2.3, three leakage paths need to be considered: leakage between two neighboring devices in the same well (path 1), junction to well leakage (path 2) and latch-up triggering (path 3). The requirements for leakage currents are translated into design rules for intrawell active area spacing (\( AA_1 \)) and \( N^+ - P^+ \) active area spacing (\( AA_2 \)). In addition to the leakage current requirements, capacitance considerations play an important role as well. Thicker field oxides are desired to reduce the interconnect to substrate capacitance. This requires longer oxidations, leading to more lateral encroachment of the field
oxide, larger substrate stress generation (see 2.2) and more oxidation enhanced diffusion and dopant segregation into the oxide. To combat the problem of reduced dopant concentration under the field oxide, a p-type field implant is generally required to provide sufficient isolation performance between neighboring NMOS devices. The classical field implant approach to increase the doping under the field oxide region has many drawbacks. The lateral encroachment of the boron into the active region can result in enhanced narrow-width effects as well as degraded n\textsuperscript{+} junction breakdown and capacitance. It requires an additional photolithography step to mask the n-well during the implant or if an unmasked implant is done, it must be compensated by an n-type dopant in the n-well field region to maintain acceptable PMOS electrical isolation. Many techniques have been proposed to reduce the boron segregation [2.6-2.8]. One particularly interesting method is the split-well drive-in [2.9], which achieves acceptable isolation performance without the use of a field implantation. In this technique, a high energy p-well implantation (to form a retrograde profile) is done before the field oxidation and a high temperature drive-in is performed after the field oxide formation. The key point of this approach is the redistribution of the total drive-in time in favor of a larger thermal budget after the field oxidation. The drive-in step after the field oxidation leads to a back-diffusion of boron to the field oxide/silicon interface, compensating the segregation effects. Compared to the classical field implant process, an increase of surface concentration under the field oxide of a factor of 2-3 is obtained in this way. The isolation performance of the n-well is not affected by the increased thermal budget due to the second high temperature diffusion step, mainly because segregation effects play only a minor role in the phosphorous doped n-well.

It is well known that ion implantation introduces significant lattice damage that can lead to extended defect formation during subsequent thermal processing. Defect generation in the silicon substrate due to p-well and field isolation formation is an important parameter in determining junction leakage currents. The stacking fault density in a highly doped p-well is very sensitive to the p-well and field implant dose and p-well formation scheme [2.10]. For doses ranging from $5 \times 10^{13}$ cm\textsuperscript{-2} to a few $5 \times 10^{14}$ cm\textsuperscript{-2} a high defect density, which is gener-
ally annealed out with great difficulty for long drive-in times, especially in an oxygen containing ambient, is often observed. To reduce the defect formation, it is necessary to develop new field isolation process modules that limit the boron segregation so that lower doses can be used. The retrograde p-well and split well drive-in have already been mentioned. Two other alternatives are the field-retro (implant through field oxide) and the polysilicon-retro (implant through the gate polysilicon) field isolation scenarios [2.10]. In both schemes, the stacking fault growth is suppressed and comparable or better electrical performance than with the classical field implant technique is obtained.

Latchup is a serious reliability concern in CMOS technology, especially for small device dimensions. As shown earlier, it is the fundamental limitation to reducing the AA design rule. The latchup immunity can be improved significantly by using retrograde wells and deep trenches. The deep trench approach allows an excellent scalability of the AA design rule and has been used extensively in deep submicron processes [2.11]. Other techniques include the use of a lightly doped epi layer on a highly doped substrate and the introduction of a buried layer with extended defects or oxygen precipitates to reduce the bulk minority carrier lifetime [2.12].

### 2.2.1.2 Isolation structure material issues

All LOCOS and modified LOCOS isolation structures use Si$_3$N$_4$ as a masking layer against oxidation. While Si$_3$N$_4$ is the material of choice, unfortunately there are a lot of problems associated with it. The as-deposited Si$_3$N$_4$ films are typically in a state of high tensile stress (of the order of 1 GPa) and when patterned, can induce large edge forces on the substrate. Unlike what is often believed, this high film stress is not caused by thermal mismatch but develops during the deposition process itself. A simple calculation indeed shows that the difference in thermal expansion coefficients between silicon and Si$_3$N$_4$ is too small to induce a film stress of 1 GPa.

The effect of intrinsic film stress on bird’s beak and defect formation has been investigated by Hui et al. [2.13]. They found that LOCOS structures with Ar implanted Si$_3$N$_4$ showed a lower defect density than non-implanted structures. Implanting Si$_3$N$_4$ with argon, is known to significantly reduce the film stress [2.14] and hence a lower edge force is induced when the nitride is patterned. The effect on the bird’s beak was found to be minimal however. This was later confirmed by Griffin et al. [2.15] who reported that LPCVD low stress nitrides, obtained by changing the flow rate of SiH$_2$Cl$_2$ and NH$_3$ yield only a slight reduction in bird’s beak, caused by an increase of nitride viscosity.

When the nitride film is patterned, large substrate stresses are induced at the film edges, which can lead to dislocation formation during subsequent high temperature thermal processes. This was recognized in the very beginning of the LOCOS technology development.
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To circumvent this problem and obtain defect free LOCOS structures, a thin thermal oxide (the pad oxide, see 2.2.1) had to be grown before depositing the Si$_3$N$_4$. The buffer oxide actually serves two purposes. First, it acts as a stress-relief layer: thermally grown SiO$_2$ is under compressive stress and as a result reduces the substrate forces exerted by the patterned Si$_3$N$_4$ film. In addition, significant stress relaxation occurs in the LOCOS structure due to the viscoelastic properties of the oxide. Secondly, the oxide can be used as an etch-stop during reactive ion etching of the Si$_3$N$_4$. While this buffer layer reduces the propensity to form defects, it also limits the scalability of the LOCOS process. Indeed, the pad oxide creates a path for oxidant diffusion under the mask edge. This results in significant lateral oxidation, thereby reducing the effective active device area.

It should be noted that a reduction in intrinsic film stress, by using PECVD nitride for instance, does not automatically permit a reduction in pad oxide. It is true that for lower intrinsic stresses, a thinner pad oxide can be used in order to still not generate defects when e.g. annealing the patterned films at higher temperature. A thinner pad oxide however also implies that a more abrupt bird’s beak will form during the oxidation, leading to much larger stresses. In addition, low stress Si$_3$N$_4$ deposited by LPCVD has been shown to be somewhat stiffer than stoichiometric LPCVD Si$_3$N$_4$. This will increase the oxidation-induced stress even more. It is clear that without proper optimization of the properties and layer thicknesses, isolation structures will result that may be prone to defect generation.

Techniques that rely on the material properties of the mask layers to reduce the bird’s beak have been reported by several authors. For example, replacing the pad oxide with an oxynitride has been shown to reduce the lateral oxidation significantly while keeping the dislocation density minimal [2.16]. Polysilicon is used in combination with Si$_3$N$_4$ in the isolation structure called Poly-Buffered LOCOS (PBL). In this structure, a polysilicon layer is inserted between the pad oxide and the Si$_3$N$_4$ layer. A detailed process description follows in section 2.2.3.2. Nevertheless, to put the importance of the masking stack material properties in perspective some comments are warranted here. The purpose of the polysilicon is to provide relief of the stress that builds up during the oxidation. As will be pointed out (see 3.3.1), the stress in the polysilicon is relieved through void formation. The deposition conditions of the polysilicon play a very important role in the stress-relief process and if not properly optimized, may lead to extensive defect formation. While the void formation is necessary to relieve the process-induced stress, it causes many additional problems that make this isolation structure difficult to optimize: there is a strong grain size dependence on the roughening of the active area edge during field oxide growth and the PBL structure is prone to substrate pitting during polysilicon removal. These two effects can cause severe gate-oxide reliability
problems and are to be avoided.

2.2.1.3 Bird’s beak: influence of process parameters

Due to the availability of an oxidant diffusion path under the nitride mask (the pad oxide), lateral oxidation can take place. As shown in figure 2.4, the lateral encroachment, also called the bird’s beak, can be characterized by a length ($L_{bb}$) and a height ($H_{bb}$) in semi-recessed structures. In fully recessed structures (where a shallow trench is etched into the silicon before field oxidation, see 2.2.2), two additional parameters are needed to fully describe the shape of the bird’s beak ($H_{bh1}$, and $H_{bh2}$). The length of the bird’s beak determines the amount of active device area loss and should be minimized for maximum packing density. The amount of nitride lifting ($H_{bb}$) and the height of the bird’s head ($H_{bh1}$, $H_{bh2}$) are important with respect to surface topography: a smooth surface, i.e. small topography, allows good step coverage of polysilicon and metal layers. Several process parameters influence the shape of the field oxide near the mask edge:

1. In figure 2.5 and 2.6, the influence of the pad oxide and nitride thickness on the bird’s beak length and height respectively, is illustrated for a semi-recessed LOCOS structure having a field oxide thickness of 600 nm grown in steam at 950 °C. It is clear that length of the bird’s beak is much more sensitive to a change in pad oxide thickness than the bird’s beak height. A decrease in pad oxide thickness leads to a significant reduction in bird’s beak. However, the need for a pad oxide to reduce the oxidation- and nitride-induced stress poses a lower limit on the thickness. The pad oxide thickness dependence of the bird’s beak arises from the fact that thicker pad oxides present a wider diffusion channel, making it easier for the oxidants to diffuse under the nitride mask.

2. A very strong influence of both $L_{bb}$ and $H_{bb}$ on the nitride thickness is observed. From bending moment considerations, the force required to lift up a beam a certain distance is

FIGURE 2.4: Parameters describing the bird’s beak in a semi-recessed LOCOS and the bird’s beak and bird’s head in a fully recessed LOCOS structure.
proportional to the third power of the thickness of the beam [2.17]. Although the mechanism involved during oxidation is more complicated than just lifting a film of nitride, the basic ideas can still be applied. Another way of looking at it is by realizing that
thicker nitride layers are more resistant to bending (they are stiffer), which leads to a shorter bird’s beak.

(3) The length of the bird’s beak is dependent on crystal orientation. \(<111>\) silicon wafers show a shorter bird’s beak then \(<100>\) wafers. In addition, it has been found that when no pad oxide is present in the LOCOS structure, the bird’s beak also depends on the mask orientation due to the fact that the surface reaction rate is orientation dependent.

(4) The ratio of \(L_{bb}\) to field oxide thickness decreases with increasing field oxide thickness until a constant value is reached. In the beginning of the field oxidation, the oxide growth is limited by the surface reaction rate and the oxidation rate under the nitride mask will be approximately equal to the oxidation rate in the field region. As the oxide thickness increases, the oxidation becomes diffusion limited and the amount of oxidants reaching the silicon surface under the nitride mask is limited by the lifting of the nitride mask. Hence the oxidant concentration under the mask edge will be lower as compared to that in the field region, reducing the ratio of \(L_{bb}\) to the field oxide thickness.

(5) Higher oxidation temperatures lead to a shorter bird’s beak as well as a reduced amount of nitride lifting. Since the reaction rate increases more rapidly with increasing temperature than the oxidant diffusivity, a shorter bird’s beak is expected and indeed observed. The temperature dependence can also be explained using the following argument. Since at higher temperatures the oxide viscosity is reduced, it presents a smaller pressure on the nitride masking layer and hence causes less nitride lifting.

2.2.1.4 The Kooi or “white ribbon” effect

The existence of the bird’s beak is not the only drawback of the LOCOS process. After the field oxidation and nitride removal, a “white ribbon” is often observed along the edge of the active area. Kooi et al. [2.18] proposed that the ribbon formation was due to localized nitridation of the silicon surface during the field oxidation. In their model, as shown in see figure 2.7, it is assumed that the diffusing species (\(H_2O\)) oxidize the Si\(_3\)N\(_4\) mask to form SiO\(_2\) and NH\(_3\). The ammonia can diffuse to the Si-SiO\(_2\) interface and form Si\(_3\)N\(_4\) or an oxynitride. This reaction is only effective in the regions removed from the mask edge where the concentration of \(H_2O\) is low enough so that nitridation may occur. When this locally nitrided region is not removed before gate oxidation, severe gate oxide thinning may occur. Indeed, the locally nitridized region prevents or retards the oxidation of the silicon surface. The amount of thinning observed is found to be dependent on the processing conditions. In general, gate oxide thinning is more severe for thicker field oxides and thinner pad oxides.

Other models based on the two-dimensional nature of the isolation edge and the corresponding stress dependent oxidation have been proposed to explain the thinning effect [2.19]. Depending on the length of the bird’s beak and the amount of overetch that is per-
formed on the pad oxide, the curvature of the silicon surface can be quite pronounced after removal of the isolation stack. This curvature may result in a significant gate-oxide thinning due to the fact that the non-planar oxide growth rate is reduced in the presence of stress. These models however, underpredict the amount of thinning that is experimentally observed.

The formation of the white ribbon does not only occur at the LOCOS edge. Nakajima et al. [2.20] showed that NH$_3$ may diffuse through the Si$_3$N$_4$ layer and nitridize the silicon at weak spots in the nitride. A detailed study of the process parameters that influence the ribbon formation was carried out by Isumi and Kiyosumi [2.21]. In contrast to the formation of a interfacial (oxy)nitride, defects or weak spots in the Si$_3$N$_4$ (e.g. pinholes, microscopic cracks) may lead to oxide growth (and a corresponding bird’s beak) in the active device region [2.22].

It is clear that both the white ribbon and the oxide islands due to nitride defects have to be removed before gate-oxide growth, in order to prevent low device yield. Overetching the pad oxide has proven successful but the most common way to reduce or eliminate these effects is a sacrificial oxidation, followed by an HF etch. More recently, high pressure dry oxidation has proven to be free of the white ribbon problem [2.23]. This finding supports the model proposed by Kooi that H$_2$O is an essential part in the formation of the interfacial nitride.

2.2.2 Fully-recessed LOCOS

The recessed LOCOS concept was developed to increase the field oxide substrate recess and reduce the topography. The technique consists of etching a shallow trench in the silicon after defining the active area but before the field oxidation (see figure 2.2). The depth of the trench is usually chosen to be about half the final field oxide thickness. Depending on the recess depth, these structures can suffer from severe topography due to the formation of the so-called bird’s head (see figure 2.4). Planarization can be accomplished in several ways: dry
etching of resist, CVD oxide or phosphosilicate glass and more recently by chemical mechanical polishing (CMP). An interesting wet-etch planarization technique was proposed by Burton et al. [2.33]. They observed that the etch rate of phosphogermanosilicate glass (PVXII - 52% SiO₂ + 43% GeO₂ + 5% P₂O₅) and thermally grown SiO₂ in HF show opposite trends with regards to the etchant composition and that at a ratio of 53% BHF: (10:1) HF both etch rates are equal. After deposition of the PVXII and reflow at 1000 ºC the oxide layers are etched, leaving behind an essentially planar surface.

In addition to the formation of the bird’s head, fully recessed oxide isolation structures suffer from a substantial increase in bird’s beak length as compared to identical non-recessed structures. The main advantage of the fully recessed isolation structures is their superior electrical isolation performance. Goodwin [2.34] has shown that the increased isolation length and curved Si-SiO₂ surface results in a dramatic decrease in off-state leakage current of field transistors due to the formation of a potential barrier for minority carriers near the field oxide corners.

### 2.2.3 Advanced LOCOS isolation structures

Due to the formation of the bird’s beak, the conventional LOCOS isolation structure does not scale well. Other physical phenomena that limit the scalability of this technology are field oxide thinning, pad oxide punchthrough and enhanced end-of-line encroachment. These will be discussed in more detail in chapter 3. From an electrical point of view, it is sometimes also desirable to limit the scaling of the field oxide thickness for capacitance considerations.

One of the claims often made is that conventional LOCOS cannot be used beyond 0.8 μm active area pitch. Naturally, this depends entirely on the required electrical performance and the final field oxide thickness. As technology advances, well concentrations tend to increase and the supply voltage to reduce so that the thickness requirement of the LOCOS can be relaxed. Nevertheless, numerous isolation structures have been proposed to reduce the bird’s beak, improve the topography and improve the electrical isolation performance.

#### 2.2.3.1 Sealed interface localized oxidation (SILO)

One of the earliest enhancements to the conventional LOCOS process was the sealed interface localized oxidation (SILO) concept reported by Hui et al.[2.13]. They proposed a process that completely seals the silicon surface under the nitride mask by nitridizing the silicon. This prevents the bird’s beak formation by blocking the lateral diffusion and reaction of oxidant molecules. Several processes to accomplish this were reported and will be briefly
discussed. They found that thermal and plasma nitridation of the silicon and SiO₂ and low energy nitrogen implantation are processes able to retard the oxidation of nitrided areas. Of all the techniques studied, it was found that nitrogen ion implantation and plasma nitridation yielded the best films in terms of oxidation resistance. The plasma and the ion implanted nitride completely seal the silicon surface and minimize the bird’s beak formation: a bird’s beak reduction of 65% as compared to a conventional LOCOS (100 nm Si₃N₄, 80 nm SiO₂) was observed in their experiment. In addition, low defect densities were obtained using these isolation schemes.

Modifications to the original SILO concept include replacing the pad oxide in the LOCOS structure with a nitrided SiO₂, formed by thermally nitriding a thin thermal oxide in NH₃ at high temperature before depositing the Si₃N₄ [2.14]. The pad oxide effectively becomes an oxynitride, presenting a higher oxidation resistance during the field oxide formation. Even more aggressive bird’s beak profiles can be obtained using the SILO/RTN concept [2.24]. In this process, the interface sealing layer is formed by rapid thermal nitridation (RTN) of the bare silicon followed by the deposition of a very thin LPCVD Si₃N₄. An oxide and second (thick) nitride are then deposited in order to achieve an efficient oxidation mask. The effectiveness of the nitridation was found to be extremely sensitive to the amount of SiO₂ present on the silicon surface prior to nitridation, e.g. for a 1200 °C nitridation, the amount of Si₃N₄ grown decreases from 3.5 nm on an atomically clean surface to 2.3 nm when a native oxide is present [2.24]. A further improvement to the SILO/RTN isolation scheme, SUPERSILO [2.10], is aimed at reducing the surface topography. After the field oxidation using the SILO/RTN scheme, a polysilicon layer is deposited and oxidized. Subsequently, a high pressure reactive ion etch (RIE) using a fluorine chemistry is carried out to remove the oxidized poly and planarize the surface.

Even though the SILO/RTN and SUPERSILO isolation method can yield impressive results for dimensions typical of 0.5 μm and 0.35 μm technology [2.27],[2.26], the use of a sealing nitride can severely degrade gate oxide integrity and area diode leakage if not properly removed after field oxidation. Both dry and wet nitride removal methods have been investigated [2.27]. The best performance is obtained by oxidizing the sealing nitride in a 170 °C H₂SO₄:H₂O₂ 2:1 mixture followed by a dilute HF etch to remove the oxide. In addition to the gate oxide integrity issues, the ability to reproducibly form the thin nitride by RTN may pose a potential manufacturability issue.

### 2.2.3.2 Poly-buffered LOCOS (PBL)

In a conventional LOCOS, the bird’s beak can be reduced by decreasing the pad oxide thickness or increasing the nitride thickness as pointed out in section 2.2.1.3. This has several disadvantages, the most important one being an increase in oxidation-induced stress. In the
poly-buffered LOCOS isolation structure [2.28], the increased stress is relieved by inserting a polysilicon layer between the pad oxide and the nitride. As a result, thinner pad oxides and thicker nitrides can be used to reduce the bird’s beak while keeping the process-induced stress low. The lateral encroachment can easily be reduced to 0.1 μm/per side for a field oxide of 800 nm [2.29].

The polysilicon layer complicates the fabrication of defect free active device surfaces following field oxidation since in addition to the nitride strip, there now needs to be an extra step for removing the unoxidized polysilicon under the nitride mask. This is typically done by plasma etching or oxidation and etchback [2.30]. Depending on the grain size of the polysilicon, it can leave behind very rough active area edges and etch pits in the substrate (due to voids in the polysilicon, see 3.3.1) which can lead to defective gate oxides. By using amorphous silicon as the buffer layer, the edge roughening can be reduced significantly and the pitting problem alleviated [2.31]. The pitting problem is directly related to the grain size of the polysilicon during the field oxidation. Recently, a method to prevent the recrystallization of the amorphous silicon by implanting it with nitrogen before nitride deposition has been proven successful in reducing the pitting problem [2.32]. Amorphous silicon does not relieve the stress as easily however. Substrate pitting and the mechanism for polysilicon void formation and stress relaxation in PBL structures will be discussed in section 3.3.1.

2.2.3.3 SWAMI

Many of the problems associated with the recessed LOCOS structures can be alleviated by using the SideWall Mask Isolation (SWAMI) isolation structure [2.35,2.36]. It incorporates many ideas that have led to the implementation of state of the art isolation structures used in today’s deep submicron processes. In the original structure, RIE etching of the Si₃N₄ and SiO₂ is used to define the active area. A shallow trench is then etched, followed by a high temperature re-oxidation to smooth the trench corners. Subsequently, a second Si₃N₄ and an SiO₂ layer are deposited and spacers are etched. The isolation structure is completed by a

FIGURE 2.8: Schematic representation of the poly buffered LOCOS isolation structure, before and after field oxidation.
steam oxidation to grow the field oxide. The SWAMI isolation structure is characterized by a small bird’s beak, smooth surface topography after field oxidation and a low substrate defect density. Since the demonstration of the original structure, several modifications have been evaluated and implemented successfully (see fig. 2.9).

The original SWAMI structure was rather sensitive to defect generation due to the vertical trench sidewalls and the thick nitride at the bottom of the trench. This problem can be eliminated by using the sloped sidewall approach as shown in figure 2.9a. By performing a second silicon etch after the oxide spacer formation, the double etch SWAMI structure results (Fig. 2.9b). Sawada et al. [2.37] showed that the latter structure, although more complex from a processing standpoint, results in much lower leakage currents. The reason for the increased performance is the smoother field oxide silicon interface in the double etched SWAMI structure. A smoother bird’s beak profile generally leads to less substrate stress and hence reduces the propensity to form defects.

A detailed transmission electron microscope (TEM) and electrical analysis of the sloped single and double etch SWAMI process was carried out by Claeys et al. [2.38]. In the double etch SWAMI structure, no near surface defects were observed. Also, the bulk defect density remained much lower than in the single etch SWAMI case and no dense dislocation networks are observed. These results corroborate the idea that a smoother field oxide profile
indeed results in less substrate stress.

2.2.3.4 Sidewall spacer LOCOS structures

Because of the increased process complexity, the SWAMI concept never made it into mainstream processes. Several “simple swami” structures that rely on blocking the lateral oxidant diffusion under the nitride mask have been demonstrated. These techniques can be classified into two groups depending on the material used to seal the mask edge, as shown in figure 2.10: i) nitride spacers to block the lateral oxidation [2.39-2.43]; and ii) poly-Si spacers to retard the diffusion of oxidants under the mask edge [2.33, 2.5, 2.44, 2.45].

The nitride spacer processes generally lead to somewhat more severe field oxide thinning (see section 3.1) due to the fact that the effective oxidation window is reduced. Critical steps in all the nitride spacer processes are the re-oxidation of the silicon before depositing the spacer nitride, and the initial nitride masking layer thickness. Without proper optimization of these parameters, high defect densities are generally observed. The most advanced nitride spacer process, the Nitride-Clad LOCOS (NCL), is due to Pfiester et al. [2.43] and has shown compatibility with 0.25 µm design rules. It uses an undercut of the pad oxide (15 nm), which is filled with a thin second nitride (10 nm) after a re-oxidation (5.5 nm) of the silicon substrate. The net result is that at the mask edge, the local pad oxide thickness is reduced and the nitride thickness increased by about 10 nm. This is sufficient to reduce the oxidant diffusion under the mask edge, resulting in a shorter bird’s beak. One interesting feature of the nitride-clad LOCOS is the fact that the spacer nitride is not etched but oxidized away during the field oxidation, keeping the process complexity low. Due to the very thin second nitride,
the NCL isolation structure is less susceptible to field oxide thinning as compared to other spacer technologies.

The poly-spacer concept was first introduced by Burton et al. [2.33]. It consists of the deposition of a polysilicon layer after the isolation mask has been etched. Spacers are then formed and the field oxide is grown. Due to the fact that the polysilicon has to oxidize before the field oxide can protrude under the nitride mask, a very short bird’s beak results (dependent on the re-oxide thickness). This concept, without using the re-oxidation step, has successfully been applied to an isolation structure for a 256 Mbit DRAM process [2.5]. A modified poly-spacer LOCOS process, which includes a polysilicon filled cavity, is the PELOX process [2.44]. In this process, the re-oxide thickness is critical in determining the final bird’s beak and substrate defect density: when the re-oxidation is omitted, a very short bird’s beak results but excessive diode leakage current and poor gate oxide integrity is observed. This illustrates well the trade-offs involved when optimizing an isolation structure. The significant bird’s beak reduction in the PELOX process, even for very thick field oxides is thought to be due to the reduction in oxidation rate of the highly stressed polysilicon filled cavity. One of the drawbacks of PELOX is the reduced field oxide recess and the corresponding reduction in isolation voltage, caused by the fact that the oxidized polysilicon has to be removed before stripping the nitride. As a result, compared to the simple spacer processes or the nitride-clad LOCOS, PELOX is harder to scale down.

2.2.4 Sealed Nitride Plug Poly-Buffered LOCOS

We have investigated a novel isolation structure, the sealed nitride-plug poly-buffered LOCOS (Sealed-NPPBL) isolation structure, that combines many of the features discussed in previous sections and have compared its electrical performance in terms of leakage currents with conventional PBL. In this isolation scheme, the bird’s beak is kept minimal by using nitride spacers and a modified SILO technique. Stress relief is provided by an encapsulated polysilicon layer.

2.2.4.1 Isolation structure

The Sealed-NPPBL process sequence is illustrated in figure 2.11. After growing a 15 nm pad oxide at 950 °C in O₂, a polysilicon layer (50 nm or 75 nm) is deposited followed by LPCVD of Si₃N₄ (150 nm or 200 nm). Subsequently, the isolation stack is patterned and the polysilicon etched isotropically using a CF₄/O₂ plasma to create a cavity of approximately 100 nm long. To avoid direct contact between the nitride spacers and the silicon substrate, a thin reoxidation is carried out to increase the pad oxide thickness back to 10 nm. Before
depositing the spacer nitride (50 nm) and etching it anisotropically, thermal nitridation was carried out to locally seal the interface. To verify that the Si$_3$N$_4$ completely filled the cavity, a deposition experiment on the overhang test structure [2.46], was carried out. Figure 2.12 clearly shows that nitride deposition by LPCVD is very conformal and should pose no problem in filling the cavity. After a field implant, the field oxide was grown in steam ambient at 975 °C to a thickness of 600 nm.

The Sealed-NPPBL isolation structure can be thought of as two isolation structures in parallel: in the beginning of the field oxidation, the structure acts as a conventional LOCOS structure. Once the nitride starts lifting due to the lateral oxidation, the poly-buffered

![FIGURE 2.11: Schematic representation of the Sealed-NPPBL process sequence: (a) pad oxide growth and optional nitridation is followed by the deposition and patterning of a polysilicon and nitride layer. (b) Undercut of polysilicon layer (c) and nitride spacers formation.](image)

![FIGURE 2.12: Silicon nitride deposition on overhang test structure. Note the very conformal deposition of Si$_3$N$_4$, indicating a very low sticking coefficient.](image)
LOCOS dominates the isolation structure and the process-induced stress is relieved.

As stated in the previous paragraph, in order to obtain an even further reduction of the lateral encroachment in the Sealed-NPPBL structure, a modified SILO technique has been investigated. In the conventional SILO/RTN process, the nitridation of the pad oxide or silicon is done prior to deposition of the masking stack. Upon removal of the masking layers after oxidation, this (oxy)nitride has to be removed as well. This complicates the isolation process and often leads to enhanced area leakage currents and reduced gate oxide integrity. An alternative that avoids these problems and is just as effective as the conventional process, is the localized SILO/RTN. In this technique, the rapid thermal nitridation is carried out as the final step of the isolation structure formation. It relies on the lateral diffusion of the NH$_3$ under the nitride mask. This way, only the edges of the active device region are nitridized. In order to characterize the effectiveness of the localized nitridation, an experiment was set up to measure the effective nitridation distance under a mask edge. The test structure consists of a conventional LOCOS structure that is exposed to NH$_3$ after the nitride RIE etch. Before stripping the nitride, a shallow trench is etched to delineate the mask edge. The nitride is then stripped and a thin oxide is grown on the silicon wafer. Because in the nitridized region of the pad oxide the oxidation will be retarded, the effective nitridation distance under the nitride mask can be measured by recording the surface profile using e.g. atomic force microscopy, as shown in figure 2.13. This measurement clearly shows a nitridation distance of approximately 0.15 μm for a 14 minute NH$_3$ anneal at 1000 °C.

An isolation structure similar to the Sealed-NPPBL structure has been reported by
Sung et al. [2.34]. In the “reverse L-shape sealed poly-buffer LOCOS” (RLSPBL), an undercut of the pad oxide is created instead of the polysilicon buffer layer. Creating the cavity by etching the polysilicon allows more process flexibility. In the Sealed-NPPBL structure, the “edge- LOCOS” composition can be more easily optimized by using different polysilicon buffer layer thicknesses and the re-oxide thickness is not limited by the initial pad oxide thickness. In addition, the localized SILO/RTN provides complete sealing of the interface, something that can only be accomplished in the RLSPBL structure by dramatically increasing the nitride thickness or reducing the pad oxide thickness.

2.2.4.2 Geometrical and electrical characterization

Cross sectional SEM micrographs of the Sealed-NPPBL structure with and without nitridation are shown in figure 2.14. Clearly, localized nitridation of the pad oxide is extremely effective in reducing the as-grown bird’s beak. However, as will be pointed out later, this leads to an increase in diode leakage currents. While the as-grown bird’s beak in the non-nitrided Sealed-NPPBL structure is of the order of 0.25 μm, after the nitride and polysilicon masking stack is removed and the pad oxide is etched back, an effective lateral encroachment of approximately 50 nm is obtained. This is mainly due to the very sharp and

FIGURE 2.14: SEM micrograph of the Sealed-NPPBL structure without nitridation (a) and with localized nitridation for 14’ in NH₃ atmosphere at 1040 °C (b).
2.2 Isolation structures

well defined oxide-silicon profile.

The electrical performance of the isolation structure was investigated by measuring the leakage current of n\textsuperscript{+}-p junction diodes for the different process splits and comparing it with PBL isolated diodes. Diodes with a constant area of 10\textsuperscript{5} \textmu m\textsuperscript{2} and a perimeter length of 1300 or 20200 \textmu m were measured on 42 devices per split. Leakage currents were recorded at a reverse bias of 5 V in all cases. The cumulative distribution of leakage currents, measured on diodes fabricated with a conventional poly-buffered LOCOS process, are presented in figure 2.15. In this figure, data for two nitride (150 and 200 nm) and two polysilicon (50 and 75 nm) thicknesses is plotted. The open symbols represent the leakage current of diodes having an area of 10\textsuperscript{5} \textmu m\textsuperscript{2} and a perimeter of 1300 \textmu m while the solid symbols represent data for perimeter intensive diodes having an area of 10\textsuperscript{5} \textmu m\textsuperscript{2} and a perimeter of 20200 \textmu m. The same convention has been adopted for all the data to be presented in the remainder of this section. For the conventional PBL, the leakage of the area intensive diodes is practically independent of the process split. The perimeter intensive diode leakage current is found to be a function of process splits however. Since the area leakage component is not affected by a change in isolation structure composition, the leakage current difference must be related to the field oxide edge. Two major trends can be observed. First of all, an increase in leakage current is observed with decreasing polysilicon buffer layer thickness. For the 150 nm nitride split, the median value of the leakage current increases from 7.8 pA for the 75 nm poly to 14 pA for the 50 nm poly split. The same trend is observed for the PBL diodes with a 200 nm nitride mask: the leakage current increases from 12 pA to 19 pA when the polysilicon thick-
isolation structures

ness is changed from 75 nm to 50 nm. The second trend is related to the nitride thickness. Increasing the nitride thickness for a constant polysilicon thickness results in an increase in leakage current. For the polysilicon thickness of 50 nm, an increase of 5 pA is observed when the nitride thickness is changed from 150 nm to 200 nm. For the thicker poly buffer layer, the change in leakage current is reduced to 4.2 pA. These results can be explained based on the fact that thicker nitrides and thinner polysilicon layers lead to larger process-induced stresses. A more detailed treatment of this effect will be deferred to chapter 6 where we will present a quantitative analysis of the relationship between leakage currents and process-induced stress. A similar plot for the Sealed-NPPBL structure is shown in figure 2.16. Again, very little difference is observed in the leakage current measured on area diodes. The change in leakage current for the perimeter diodes is reduced in comparison with the PBL diodes however. This is possibly related to a larger process-induced stress for the Sealed-NPPBL structure and indicates that the isolation performance is entirely dominated by the aggressive edge LOCOS structure. As a result, the parallel PBL stack is less effective in relieving the stress. In addition, it is worth noting that the median value of the leakage currents for all process splits has increased significantly in comparison with the PBL diodes. Thinner nitrides and thinner polysilicon layers do still give a lower perimeter leakage current, in agreement with the process-induced stress related argument.

Nitridation by the localized SILO/RTN technique results in an increase of the leakage current measured on perimeter diodes for all process splits we have investigated. The leakage current measurement results for the various splits are summarized in figure 2.17. The follow-

FIGURE 2.16: Cumulative distribution of the leakage current of diodes fabricated with Sealed-NPPBL isolation and without nitridation. Symbol convention is the same as in figure 2.15.
I so\textit{lation structures}

Longer nitridation times generally lead to increased degradation of the leakage current. For conventional PBL diodes and the most relaxed Sealed-NPPBL structure (75 nm poly, 150 nm nitride) however, the leakage current degradation is not as pronounced and acceptable values are obtained. Increasing the nitride thickness in the Sealed-NPPBL structure leads to a dramatic increase in perimeter diode leakage with increasing nitridation time. It was found that increasing the polysilicon thickness to 75 nm improved the leakage current performance for the shorter nitridation (7 minutes). No effect of the nitridation on the leakage current of area diodes is observed, except for the Sealed-NPPBL structure with the thinnest polysilicon and thickest nitride layer (50 nm poly, 200 nm nitride). This is the most aggressive isolation structure and sealing the interface leads to the formation of a large number of extended defects, spreading out into the area

\textbf{FIGURE 2.17:} Effect of nitridation by localized SILO/RTN on leakage current of area (open symbols) and perimeter (closed symbols) PBL and NPPBL isolated diodes.
The nitridation is used to seal the pad oxide/silicon interface and hence reduce the bird’s beak. In doing so, a much more abrupt field oxide profile results which leads to an increase in process-induced stress and possibly extended defects. We have measured the amount of bird’s beak reduction for the PBL structure and the Sealed-NPPBL structure having a polysilicon thickness of 50 nm and a nitride thickness of 150 nm. For the PBL structure, a reduction in the length of the as-grown bird’s beak 0.1 μm is observed after a 14’ nitridation at 1040 °C. In case of the Sealed-NPPBL isolation structure, the as-grown bird’s beak is reduced by about 0.25 μm after a 14’ nitridation. This big difference in the effectiveness of the nitridation between PBL and Sealed-NPPBL may also explain why the leakage currents in the PBL diodes did not change dramatically for the nitrided samples.

It is clear from these results that while nitridation reduces the lateral encroachment, it often leads to an increase in leakage current, especially in very aggressive isolation structures. The results suggest however that for the Sealed-NPPBL isolation scheme an optimal structure composition can be found that minimizes the bird’s beak and yields low leakage currents, comparable to standard PBL isolated diodes.

2.2.5 Role of trench isolation

As mentioned in section 2.2, the design rule for n+ to p+ spacing is much larger than the n+ to n+ spacing rule due to the fact that the well isolation region has to support a well boundary and lithography misalignment of the active regions to the well boundary. This fact has stimulated the development of shallow and deep trench-based isolation approaches for device and well isolation respectively. The trench isolation concept is schematically illustrated in figure 2.18. Even though trench isolation has successfully been implemented in sub-
micrometer processes, it is still not a mainstream process due to high process complexity and manufacturing cost. From a reliability point of view, trench isolation edges are much more sensitive to hot-carrier damage than LOCOS, probably due to poorer oxide quality at the trench edges [2.48]. In addition, trench isolation suffers from parasitic n-channel inversion along the trench sidewall. This is especially detrimental for memory applications which require low device leakage currents. In chapter 6, it will be shown that trench isolation is not free of substrate stress generation and that oxidation performed after the shallow trench formation can lead to large stresses as the active area pitch is reduced.

There is strong evidence that LOCOS continues to be regarded as a serious alternative for the intrawell device isolation for 0.35 μm and beyond. On the other hand, trench isolation is definitely a viable candidate for deep submicron isolation and the general trend has been to introduce deep trenches only for well isolation in order to improve latch-up performance and keep using LOCOS for intrawell isolation. It should be noted that the device and well isolation may not always be the limiting factor in scaling CMOS but that the actual packing density is often limited by the interconnects.

2.3 Conclusions

An overview of the general technological features of LOCOS based isolation technologies was given and the problems associated with scaling device isolation technologies were addressed. A novel isolation structure, the Sealed Nitride-Plug Poly-buffered LOCOS, has been developed and characterized in terms of geometry aspects and diode leakage. Acceptable perimeter and area leakage currents have been demonstrated. The concept of localized nitridation was introduced to minimize the active device area exposure to the nitridation reaction, a process known to cause reduced gate oxide integrity and increased area diode leakage. Sealing the interface of a LOCOS structure using nitridation of the pad oxide is extremely effective in reducing the bird’s beak but in already highly stressed structures leads to extensive defect generation. From these results, it can be concluded that nitridation of the interface should probably be avoided in isolation structures using spacer technology to block the lateral oxidation. For standard PBL structures however, acceptable results have been obtained.
2.4 References

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