Into the Core ...

Pat Gelsinger
Senior Vice President
Intel Corporation

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In 2001, I made a prediction ...

Thankfully it didn’t come true ...
Power Density Will Get Even Worse

- Sun’s Surface
- Rocket Nozzle
- Nuclear Reactor
- Hot Plate
- Pentium® processors

Need to Keep the Junctions Cool
- Performance (Higher Frequency)
- Lower leakage (Exponential)
- Better reliability (Exponential)
Energy: The Next Frontier
Historical Driving Forces

Increased Performance via Increased Frequency

- Frequency (MHz)
- 1970: 1 MHz
- 1980: 10 MHz
- 1990: 100 MHz
- 2000: 1 GHz
- 2020: 10 GHz

Shrinking Geometry

- Feature Size (um)
- 1970: 10 um
- 1980: 1 um
- 1990: 0.1 um
- 2000: 0.01 um
- 2020: 0.001 um

Intel

1946
20 Numbers in Main Memory

1971
8004 Processor
2300 Transistors

2005
65nm
1B+ Transistors

Source: Intel
The Challenges

Power Limitations

- CPU Power (W)


Diminishing Voltage Scaling

- Supply Voltage (V)


0.7um, 0.5um, 0.35um, 0.25um, 0.18um, 0.13um, 90nm, 65nm, 45nm, 30nm

~30%

Power = Capacitance x Voltage$^2$ x Frequency
also
Power $\sim$ Voltage$^3$

Source: Intel
The Classic Tradeoff

Higher
Top Speed and Acceleration

Increased
Range and Economy

OR
A New Era...

THE OLD
- Performance
- Equals
- Frequency
- Unconstrained
- Power
- Voltage Scaling

THE NEW
- Performance Equals IPC
- Multi-Core
- Power Efficiency
- Microarchitecture Advancements
Intel® Core™ Microarchitecture

Energy-Efficient Performance

Critical Capabilities

Next-Generation Processors for Mobile, Desktop and Server
Intel® Core™ Microarchitecture

Instruction Fetch and PreDecode

Instruction Queue

Decode

Rename/Alloc

2M/4M Shared L2 Cache

Up to 10.6 GB/s FSB

Retirement Unit (ReOrder Buffer)

Out of Order

Micro-op Schedule

Micro-op Execute

Schedulers

ALU
Branch
MMX/SSE
FPmove

ALU
FAdd
MMX/SSE
FPmove

ALU
FMul
MMX/SSE
FPmove

L1 D-Cache and D-TLB

Memory Order Unit

Load

Store
Intel® Core™ Microarchitecture

Instruction Fetch And PreDecode

Instruction Queue

2M/4M Shared L2 Cache
Up to 10.6 GB/s FSB

uCode ROM

Decode

Rename/Alloc

Out of Order
Memory Pipelines

Retirement Unit (ReOrder Buffer)

Schedulers

Memory Order Unit

ALU Branch MMX/SSE FPMove
ALU Add MMX/SSE FPMove
ALU FMul MMX/SSE FPMove

L1 D-Cache and D-TLB

Load Store

Memory Order Unit Maintains Architectural Ordering Requirements
Intel® Core™ Microarchitecture

In Order
Micro-op Retirement
Fault Handling
Retirement Unit
Maintains Illusion
Of In Order
Instruction Retirement

Retirement Unit (ReOrder Buffer)
Five Key Innovations

- Intel® Wide Dynamic Execution
- Intel® Advanced Digital Media Boost
- Intel® Intelligent Power Capability
- Intel® Smart Memory Access
- Intel® Advanced Smart Cache
Intel® Wide Dynamic Execution

**EACH CORE**
- Efficient 14 Stage Pipeline
- Deeper Buffers
- 4 Wide - Decode to Execute
- 4 Wide - Micro-op Execute
- Micro and Macro Fusion
- Enhanced ALUs

**CORE 1**
- Instruction Fetch and Pre-Decide
- Instruction Queue
- Decode
- Rename / Alloc
- Retirement Unit (Reorder Buffer)
- Schedulers
- Execute

**CORE 2**
- Instruction Fetch and Pre-Decide
- Instruction Queue
- Decode
- Rename / Alloc
- Retirement Unit (Reorder Buffer)
- Schedulers
- Execute

**ADVANTAGE**
- 33% Wider Execution over Previous Gen
- Comprehensive Advancements
- Enabled In Each Core
Intel® Wide Dynamic Execution
Micro and Macro Fusion

**EXAMPLE:** CMP+JMP IN 1 CLOCK

**WITHOUT MACRO FUSION**
- INSTRUCTION 3
- INSTRUCTION 2
- INSTRUCTION 1

**WITH MACRO FUSION**
- INSTRUCTION 3
- INSTRUCTION 2
- INSTRUCTION 1

**DECODE**
- INTERNAL INST 3
- INTERNAL INST 2
- INTERNAL INST 1

**EXECUTE**
- COMPLETED INST 3
- COMPLETED INST 2
- COMPLETED INST 1

**ADVANTAGE**
- Instruction Load Reduced ~ 15%**
- Micro-Ops Reduced ~ 10%**

*Graphics not representative of actual die photo or relative size; **Workload dependent
Intel® Advanced Digital Media Boost
Single Cycle SSE

In Each Core
- Fusion Support
- Single Cycle SSE

SSE Operation (SSE/SSE2/SSE3)
- SOURCE
- SSE/2/3 OP
- DEST

Previous
- CLOCK CYCLE 1: X2opY2, X1opY1
- CLOCK CYCLE 2: X4opY4, X3opY3

Core™ μarch
- CLOCK CYCLE 1: X4opY4, X3opY3, X2opY2, X1opY1

ADVANTAGE
- Increased Performance
- 128 bit Single Cycle in each core
- Improved Energy Efficiency

Perf ↑
Energy ↓

*Graphics not representative of actual die photo or relative size*
Intel® Advanced Smart Cache
Dynamic L2 Cache Usage

- **Independent L2**
  - Increased Traffic
  - Not Shareable
  - L1 CACHE (CORE 1)
  - L1 CACHE (CORE 2)

- **Shared L2**
  - Decreased Traffic
  - Dynamically, Bi-Directionally Available
  - L1 CACHE (CORE 1)
  - L1 CACHE (CORE 2)

**ADVANTAGE**
- Higher Cache Hit Rate
- Reduced BUS Traffic
- Lower Latency to Data

*Graphics not representative of actual die photo or relative size*
Intel® Smart Memory Access
Hardware-based Memory Disambiguation

**Previous Microarchitecture**
- INST 2 - LOAD [Y]
- INST 1 - STORE [X]

**Core™ Microarchitecture**
- INST 2 - LOAD [Y]
- INST 1 - STORE [X]

**Advantage**
- Higher Utilization of Pipeline
- Masks latency to data access
- Higher Performance

**Perf**

**Energy**
Intel® Intelligent Power Capability

- Process
  - 65nm
  - Strained Silicon
  - Low-K Dielectric
  - More Metal Layers

- Coarse Grained
  - Aggressive Clock Gating
  - Enhanced Speed-Step

- Ultra Fine Grained
  - Low VCC Arrays
  - Blocks Controlled Via Sleep Transistors

- Transistor
  - Low Leakage Transistors

Energy Advantage
- Mobile-Level Power Management
- Energy Efficient Performance

*Graphics not representative of actual die photo or relative size*
Why Multi-Core?

1.00x

Max Frequency

Relative to single-core frequency and Vcc
Increasing Frequency

Over-clocked (+20%)

Max Frequency

Relative to single-core frequency and Vcc
Decreasing Frequency

- Increased Freq (+20%)
  - Performance: 1.73x
  - Power: 1.13x

- Max Frequency
  - Performance: 1.00x
  - Power: 1.00x

- Decreased Freq (-20%)
  - Performance: 0.87x
  - Power: 0.51x

Relative to single-core frequency and Vcc
Multi-Core Energy-Efficient Performance

Increased Freq (+20%) 1.13x
Max Frequency 1.00x
Decreased Freq (-20%) Dual Core 1.02x

Relative to single-core frequency and Vcc
Multi-Core Trajectory

Dual-Core

2006

Quad-Core

2007

*Graphics not representative of actual die photo or relative size*
Result: Breakthrough Energy Efficiency

Specint rate2k; source: Intel; some data estimated.
Result: Breakthrough Energy Efficiency

Specint rate2k; source: Intel; some data estimated.
Comprehensive Platform Architecture
Example: The Memory Controller

Rapid Adoption Of Technology Transitions

Business + Technical

RELIABILITY
PERFORMANCE
MEMORY ACCESS REDUCTION
POWER MANAGEMENT
PROCESS SCALING RATES
PLATFORM-LEVEL ENHANCEMENTS

Market Segments Require Different Technologies
MOBILE DESKTOP SERVER

intel
Comprehensive Platform Architecture
Example: The Memory Controller

Memory Controller in Chipset
- Extended RAS for Servers
- Memory Closer to Integrated GFX, Smart Cache and Smart Memory Access
- CPU Power States w/ Memory Alive
- MC vs Processor Device Scaling
- IO Acceleration Technology

Technical
- RELIABILITY
- PERFORMANCE
- MEMORY ACCESS REDUCTION
- POWER MANAGEMENT
- PROCESS SCALING RATES
- PLATFORM-LEVEL ENHANCEMENTS
Challenges Ahead
Variability
Scaling
Reliability
Variations: The Impact

130nm

30%

Frequency
~30%

Leakage
~5-10X

Today:
Local Optimization
Single Variable
(Frequency)

Tomorrow:
Global Optimization
Multi-variate
(yield, power, frequency)

Source: Intel
Scaling: Speculations

- Tox Scaling (Relative)
  - Technology Node (nm): 250, 180, 130, 90, 65, 45, 32, 16, 11
  - Scaling Values: 1, 0.8, 0.6, 0.4, 0.2, 0.1

- Vcc Scaling (Relative)
  - Technology Node (nm): 250, 180, 130, 90, 65, 45, 32, 16, 11
  - Scaling Values: 1, 0.8, 0.6, 0.4, 0.2, 0.1

- Frequency (Relative)
  - Technology Node (nm): 250, 180, 130, 90, 65, 45, 32, 16, 11
  - Frequency Values: 2, 4, 6, 8, 10, 12

- Logic Power (Relative)
  - Technology Node (nm): 250, 180, 130, 90, 65, 45, 32, 16, 11
  - Power Values: 1, 2, 3, 4, 5

Source: Intel
Reliable Systems with Unreliability Components

Soft Error FIT/Chip (Logic & Mem)

Extreme Device Variations

Time Dependent Device Degradation

Burn-in May Phase Out…?

Source: Intel
Research Targets

- Ever Increasing Parallelism
- Increased Energy Efficiency
- Resilient Circuits and Architectures
Questions?