Design for Yield Using Statistical Design

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Outline

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About P.A. Semi

- Santa Clara-based fabless processor company
  - Power Architecture™ Licensee
    - Design our own Power Architecture processors
    - Only 3rd company after IBM and Freescale
  - Noted industry veterans combine in 150-strong organization
  - Venture backed by Bessemer, Venrock, and Highland Capital
  - Currently engaged with over 100 customers across different market segments

- Strategically partnered with IBM

- Breakthrough processor solution focused on low power @ high performance
  - Scalable 64-Bit Power multicore architecture
  - Redefines high performance (2GHz) at ultra low power (4W)
  - 39 patents filed and 11 more patents in progress towards filing
Target Markets

Critical Requirements
- Power Efficiency
- High Performance
- Cost Efficiency
- Throughput Efficiency
- Open source OS/Tools etc

Target Markets:
- Compute Server Blades
- Digital Entertainment
- Embedded Boards
- Routers
- Game Players
- Switches
- Imaging Systems
- Storage Systems
- Wireless Basestations
The Challenge

Power Management

Process Variability
Three main reasons why process variability has become so important:

- **Moore's law:**
  - Exponential growth in device integration
  - Billions of devices per die in 65nm and beyond

- **Shrinking devices:**
  - Gate oxides approaching a few Angstroms
  - Fewer dopants under the gate (~10^2)

- **Ultra low VDD:**
  - VDD scaling < 1V to manage power.
  - Vt not scaling, limited by leakage.
  - Less headroom, more sensitivity to ΔVt.
Process Variation

- **Global**: die-to-die, wfr-to-wfr, and lot-to-lot variations caused by changes in:
  - Tox
  - Xtor W & L
  - N/PWELL doping
  - N/PMOS flatband voltage
  - Stress-induced effects

- **Local**: within-the-die variations caused by:
  - Xtor W & L mismatch
  - Vt mismatch
  - ACLV
Width and Length Mismatch

- Caused by variations in the lithographic process
- Width and Length variations are uncorrelated
- Small transistors more sensitive to W/L changes

65nm CMOS NAND cell

Intel 65nm 6T SRAM cell
Vth Mismatch

- Random fluctuations due to relatively small number of dopants in the channel
- Vth variance is inversely proportional to transistor area
- Pelgrom's Law:

\[
\sigma(V_{th}) = K / \sqrt{W \times L}
\]

- Provided by most foundries
- More realistic than corner models.
- Cover the full design space.
- Foundries typically offer a $3\sigma$ process.
- The number of local sigma is determined by the designer.
Monte Carlo

- Monte Carlo involves simulating a circuit over a wide range of randomly chosen devices parameters.
- The result is a distribution plot of design constraints, e.g., delay or noise margin.
- Typically tens of thousands simulations needed, including Vdd and Temp sweeps.

![Graph showing distribution of delay vs. Vth.](image-url)
When to use statistical analysis

- Usage limited to **process-sensitive** circuits:
  - Races
  - Contention
  - Mismatch

- Usage limited to **high-usage** circuits:
  - SRAM cells
  - Register file cells
  - Flip-flops
  - Sensamps

- Usage limited to **highly-critical** circuits:
  - Max and min critical paths
How many Sigmas?

Failure criteria:

\[(\mu - N \sigma - M \sigma_L) > \text{Safe Margin}\]

where:

- \(\mu\) is the mean
- \(N\) is determined by the foundry and is typically 3.
- \(M\) is determined by the number of instances of the circuit being analyzed:

<table>
<thead>
<tr>
<th># of instances</th>
<th>M</th>
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<tr>
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<tr>
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</tbody>
</table>

Example: 1MB SRAM needs \(M=5\) sigma for the bit design.
Example 1: 6T SRAM Cell

- Find stable VDD window for 6T SRAM cell (1MB)

Flow:
- Run Monte Carlo SNM sims
- Find \( \mu, \sigma_G, \) & \( \sigma_L \) across VDD
- Define safe margin
- Plot 3\( \sigma_G \) and 5\( \sigma_L \) curves
- Find Vdd window where SNM > Safe margin.
Example 2: Sense Amplifier

- Find min $V_{\text{DIFF}}$ for sensamp

Flow

- Run Monte Carlo
- Plot passing ratio vs. $\Delta V_{\text{in}}$
- Find $\mu$ & $\sigma_L$ for sensamp
- Find $\mu$ & $\sigma_L$ for SRAM $I_{\text{read}}$
- Min $V_{\text{DIFF}}$:

$$V_{\text{DIFF}} = \frac{\sigma_{\text{SA}}}{\sqrt{1 - (M \times \sigma_{\text{Iread}} / \mu_{\text{Iread}})^2}}$$
Other Circuits

Other possible applications for statistical circuit design:
- Dynamic logic
- Latches
- Register files cells
- Pulsed flops
- Level shifters
- Analog circuits

Advantages:
- All circuits designed to a target sigma
- Avoid weak links
- Avoid overdesign
Statistical Timing

- Each gate has a mean and sigma. Sigmas can be computed using Monte Carlo.
- The sigma of a path is determined by adding (i.e., sum-square) the sigmas of individual gates.

\[ \sigma_{\text{Path}} = \sqrt{\sigma_1^2 + \sigma_2^2 + \ldots + \sigma_n^2} \]
Speed Distribution

- Each chip has a local distribution on top of the global distribution due to local variations.
- Not all parts within a $[+3\sigma, -3\sigma]$ window will yield above target due to local variations.
OCV Ratio and Yield

- On-chip Variability (OCV) = $\sigma_{\text{Local}}$
- OCV Ratio = $\frac{\sigma_{\text{Local}}}{\sigma_{\text{Global}}}$
- Speed yield strongly dependent on OCV ratio
Yield Examples

- Speed yield is affected by the shape of the timing histogram:

These three histograms have very different speed yields (OCV Ratio=1.5):

These three histograms have the same speed yield (OCV Ratio=0.9):
Margining Races

- Races need to be margined for PVT variations.
- Fixed PVT margin (conventional):

\[ D_{21} = D_2 - D_1 + m \times (D_1 + D_2 + D_{21}) \]

- Fixed PVT sigma:

\[ D_{21} = D_2 - D_1 + M \sigma \sqrt{(D_1 + D_2 + D_{21})} \]

- Drawbacks of fixed margin:
  - Pessimistic for long delays
  - Optimistic for short delays

- Advantages of fixed sigma:
  - Accurate (pseudo-statistical)
  - M can be tuned for a specific design
Fixed sigma:
- PVT margin varies with the logic depth
- PVT margin varies with Vdd

![Graph showing PVT margin variation with logic depth and Vdd](image-url)
Test structures were developed to measure process variability.

A testchip was built in a 65nm, triple-Vt, dual-oxide CMOS process.

Data was collected across dies, wafers, lots, and across voltage and temperature.

Measured data was used to:

- Validate statistical SPICE models
- Monitor process development
- Determine design margins
- Predict circuit limited yield
A Racer circuit measures on-die process variations in Si.

> 100 copies of the Racer module are placed across the die.

The spread in the location of the leading “1” provides an indication of the process variability.
Racer Results

- Racer data shows large spreads at low Vdd.
- Data can be used to predict circuit yield across Vdd.
- Low Vdd is the yield limiter!
A Leaker Circuit

A Leaker circuit measures leakage spread (Ioff/Ion) in Si.

It measures Ioff/Ion by sensing a tied-off skewed inverter with a 2P:1N inverter and latching to a flop.

Multiples copies of the leaker module are placed on the die.

Separate modules are used for standard Vt, low Vt, and high Vt devices.
Leaker Results

- Leaker data was collected across voltage and temperature.
- Distributions were generated and $\mu/\sigma$ data was obtained.
- $I_{off}/I_{on}$ ratio worse at low Vdd for all Vt devices
- $I_{off}/I_{on}$ ratio worse at high temperature for all Vt devices
CAD Challenges

Applications for statistical design:
- Timing
- Power
- ERC
- Reliability

Main Challenges:
- Run time: Running Monte Carlo on a library would take years!
- Tools need to be 'context aware': Ex: Timing optimization depends on the shape of the timing histogram

Pseudo-statistical approach
- Using statistical methods without running Monte Carlo.
CAD Challenges (cont.)

- Cell based designs
  - Library characterization should produce $\mu, \sigma$.
  - Timing analyzer output should be speed yield.

- Transistor level design
  - In-situ characterization to generate $\mu, \sigma$
  - Timing analyzer to create $\mu, \sigma$ for macro

- ERC/Reliability
  - Statistically derived design rules
  - Waivers based on distributions and yield impact

- Yield, Yield, Yield
  - Tools should predict yield as a metric for signoff.
Tool Integration

- Integration of DFM and DFY tools to predict:
  - Manufacturing yield
  - Functional Yield
  - Speed yield
  - Overall product yield

Validation

- Validation of DFY tools in Silicon
- Justification of investment
Summary

- Ignoring process variability may lead to non-functional designs or suboptimal yields.
- DFY will become more relevant as Vdd continues to scale and device geometries keep shrinking.
- Circuit solutions alone will not be sufficient if Moore's law continues.
- Process variability need to be handled at higher levels of the design process
- Future designs will incorporate:
  - Self-checking logic
  - Self-correcting logic
  - Redundant logic (besides SRAMs)
  - Wearout compensation mechanisms.
Thank You

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