



Carbon Nanotube Imperfection-Immune Digital VLSI

Subhasish Mitra

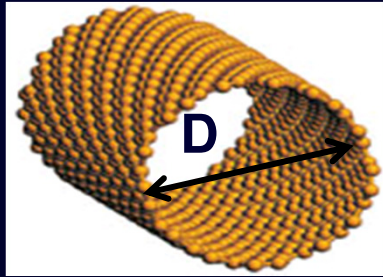
Robust Systems Group

Department of EE & Department of CS

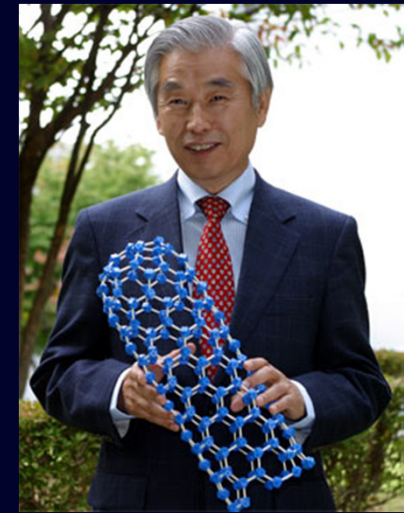
Stanford University

H. Chen, J. Deng, A. Hazeghi, A. Lin, N. Patil, M. Shulaker, L. Wei, H. Wei, Prof. H.-S. P. Wong, J. Zhang

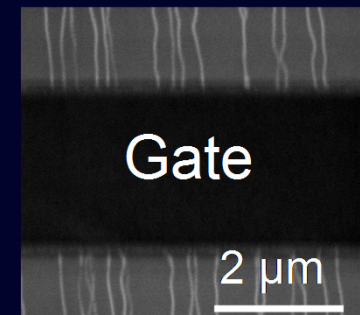
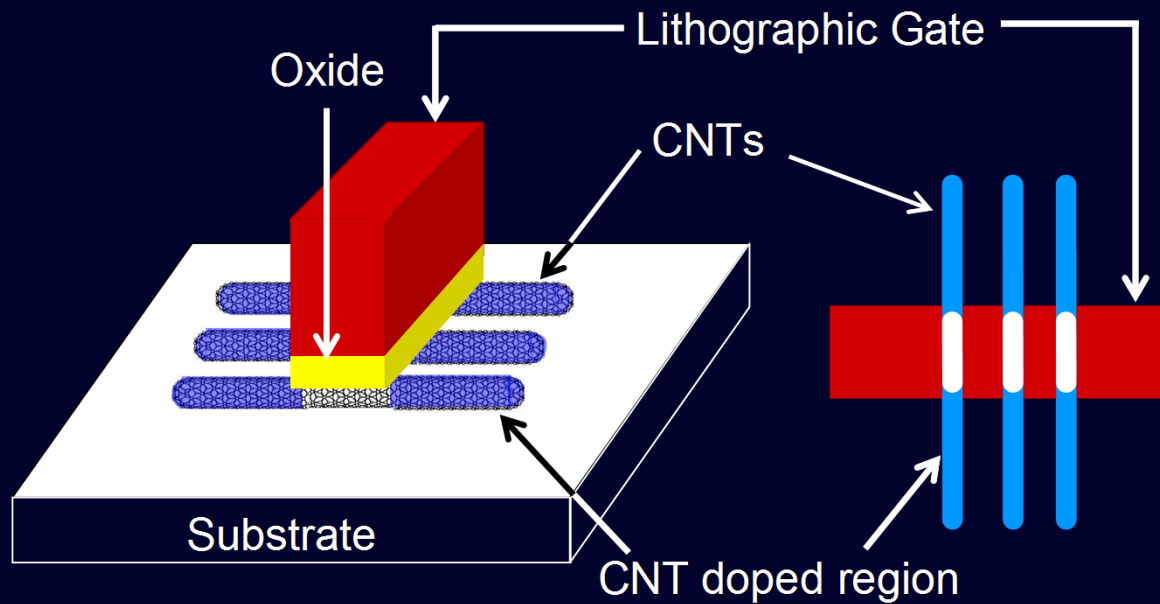
Carbon Nanotube FET (CNFET)



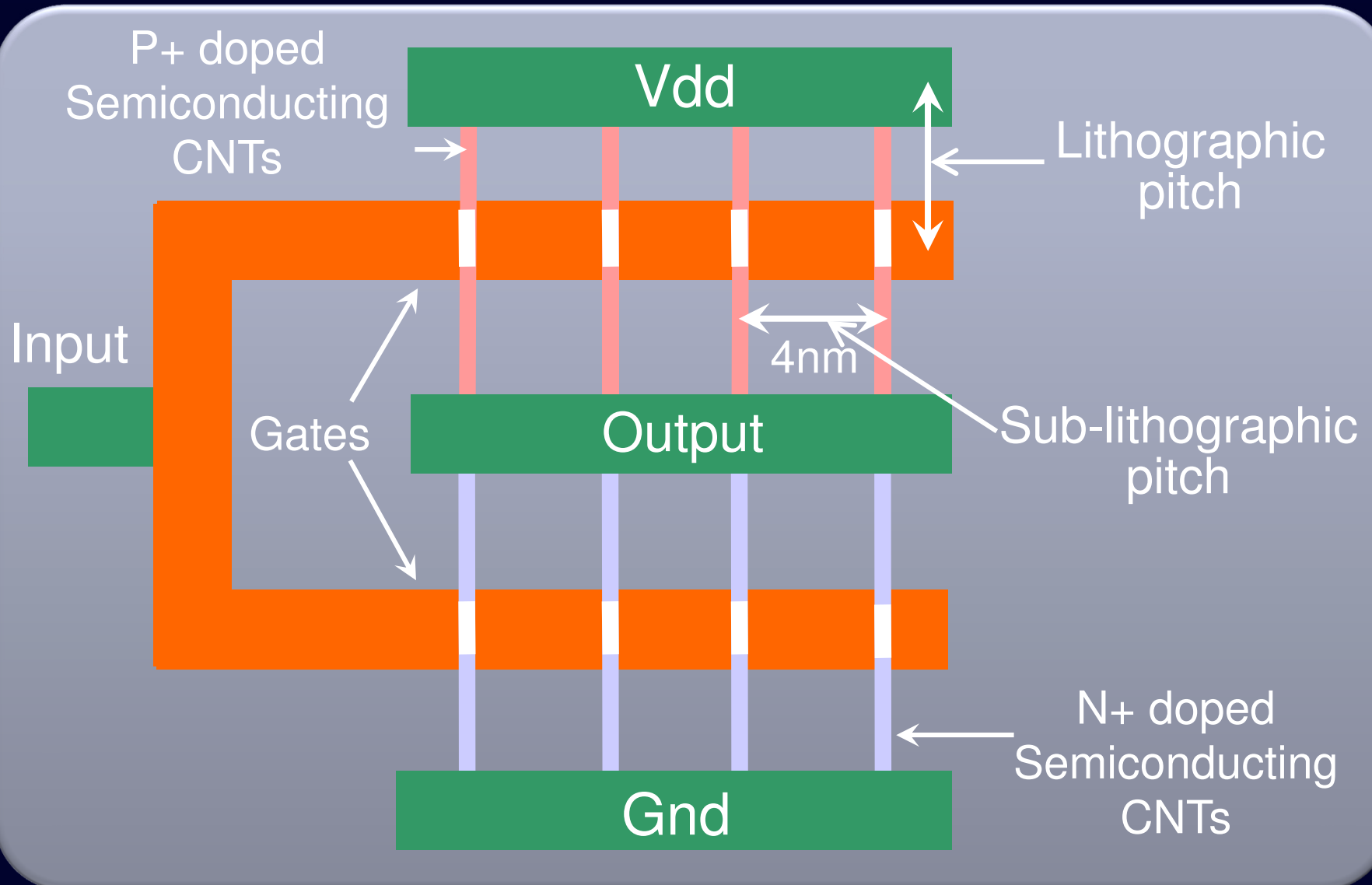
Carbon Nanotube (CNT)
Diameter (D) : 0.5 - 3 nm



S. Iijima

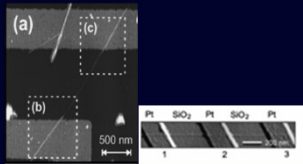


Ideal CNFET Inverter



CNFET Technology Milestones

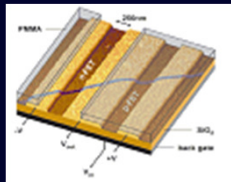
1998
First CNFET demonstration
[Delft, IBM]



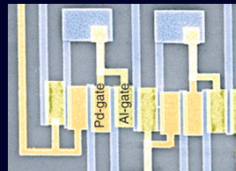
2004
Best single-CNT CNFET
[Stanford]



2001
Single-CNT logic gates
[IBM]

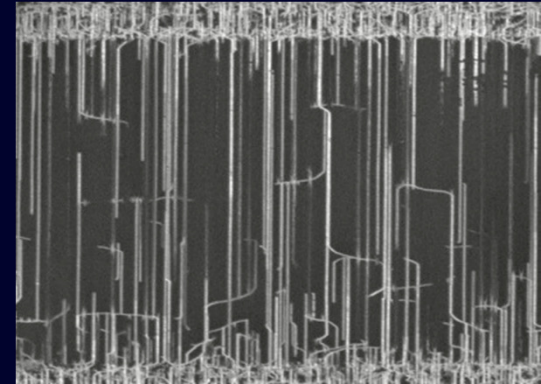


2006
Single-CNT ring osc.
[IBM]

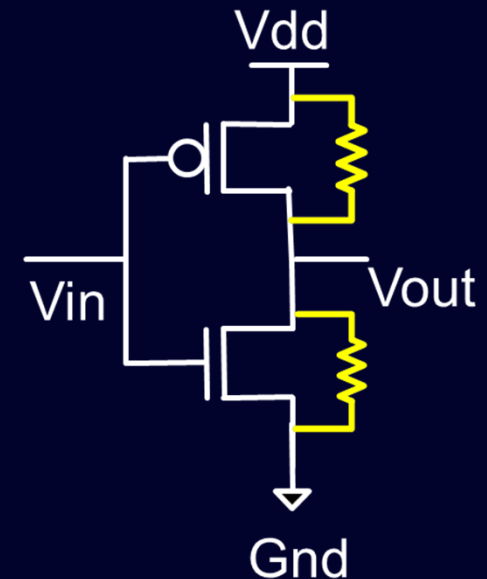


CNFETs: BIG Promise, BUT

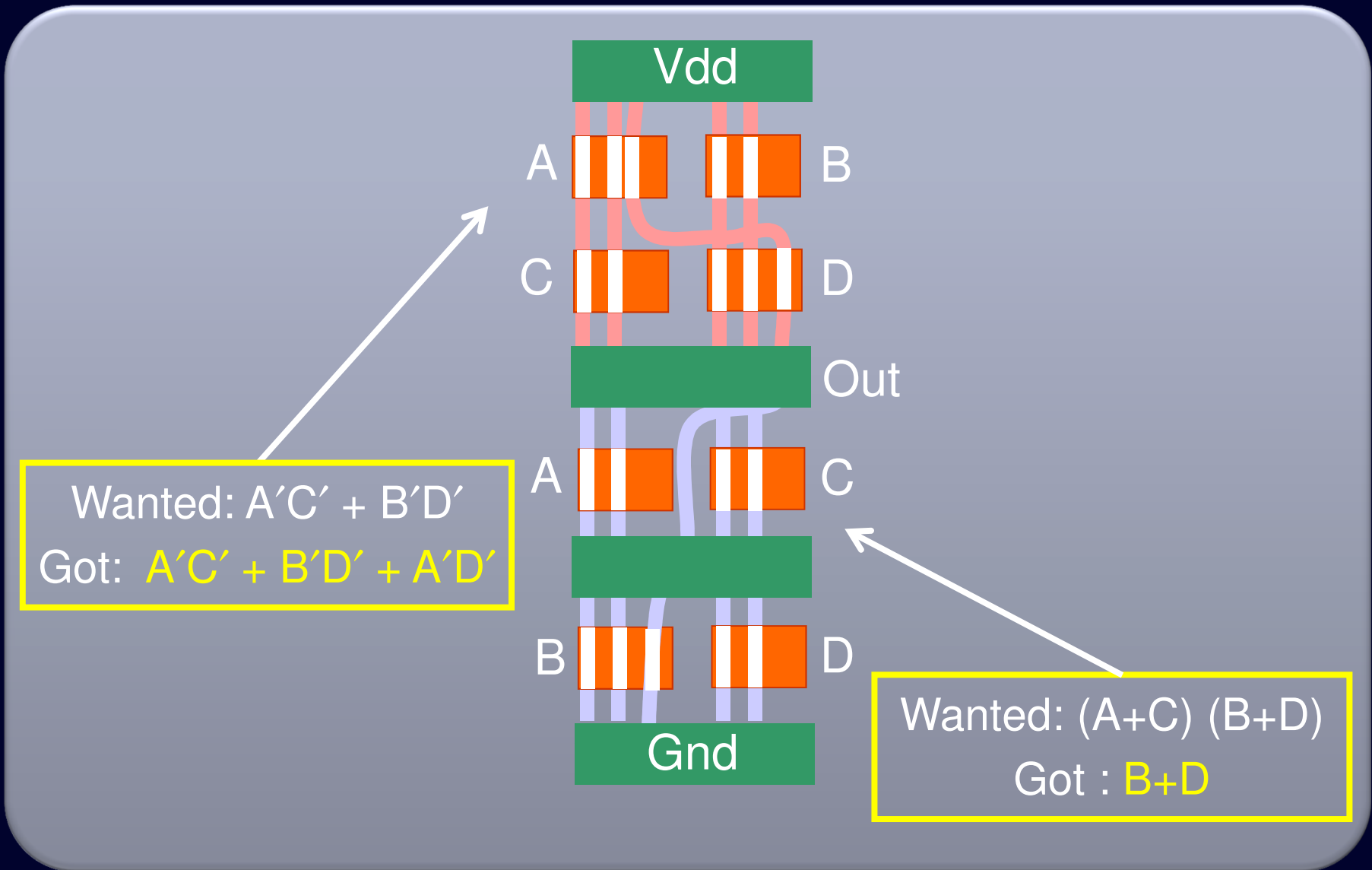
- Major barriers for a decade
 - Mis-positioned nanotubes
 - Metallic nanotubes
- Processing alone inadequate



**Imperfection-immune
design essential**

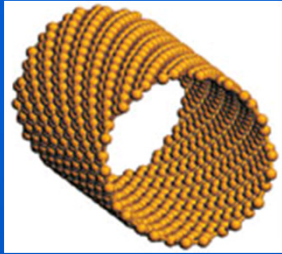


Mis-positioned CNTs → Incorrect Logic

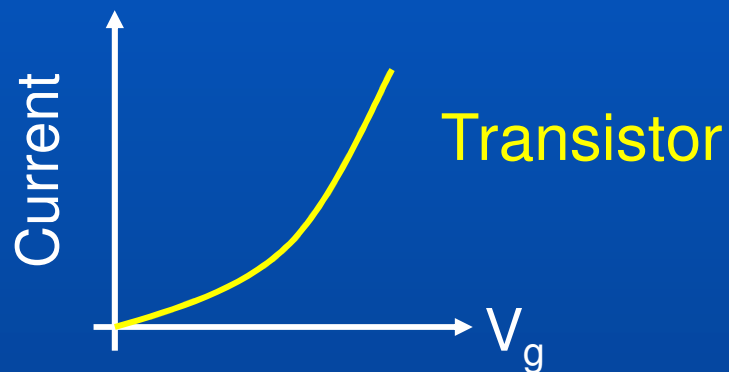


Metallic CNTs

Semiconducting CNT (s-CNT)



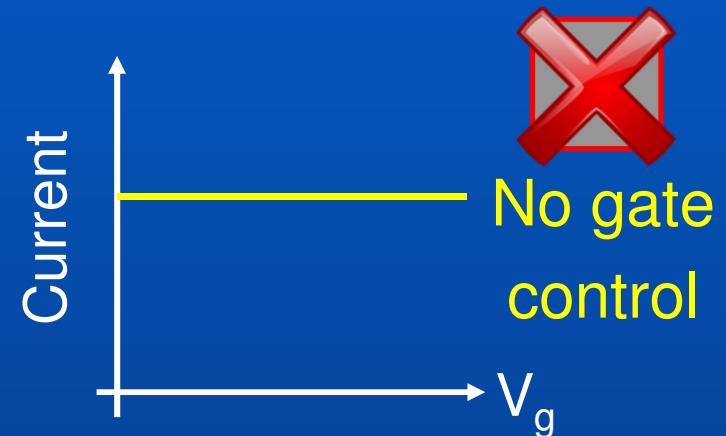
CNFET with s-CNT



Metallic CNT (m-CNT)



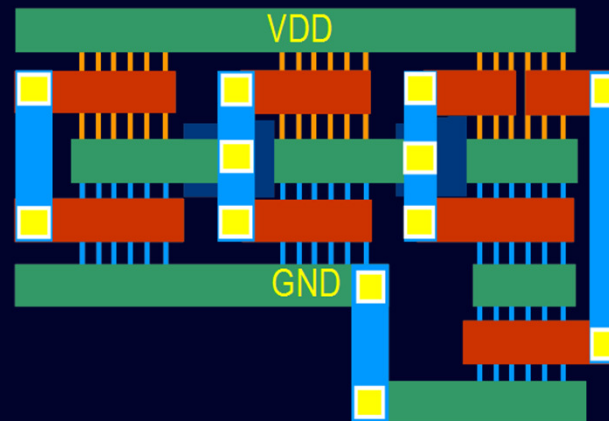
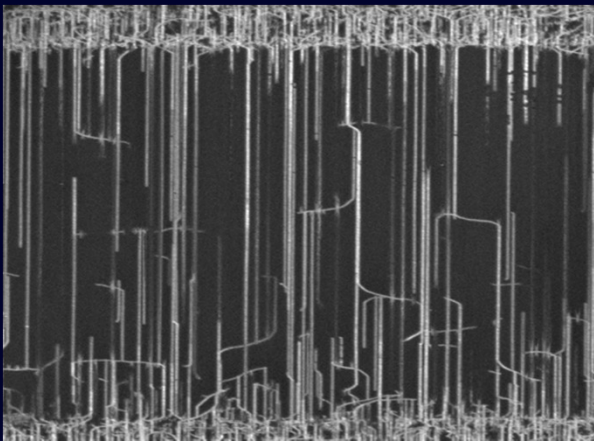
CNFET with m-CNT



Typical: 10 – 50% grown CNTs metallic

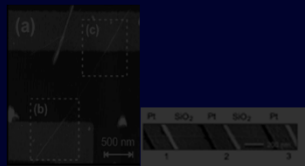
Results

- Yesterday
 - SSI single-CNT ring oscillator
- Today
 - Imperfection-immune VLSI circuits



CNFET Technology Milestones

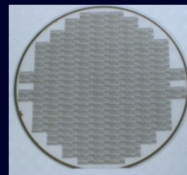
1998
First CNFET demonstration
[Delft, IBM]



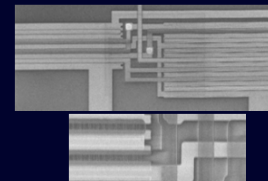
2004
Best single-CNT CNFET
[Stanford]



2008
Mis-positioned-CNT-immune VLSI logic gates
[Stanford]



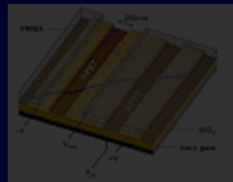
2009
Imperfection-immune adders & latches
[Stanford]



2009
Monolithic 3D CNT circuits
[Stanford]



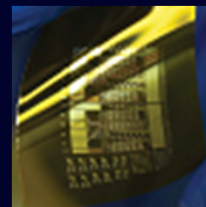
2001
Single-CNT logic gates
[IBM]



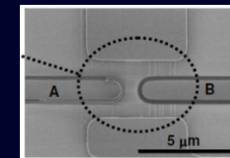
2006
Single-CNT ring osc.
[IBM]



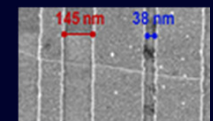
2008
Flexible CNT circuits
[UIUC]



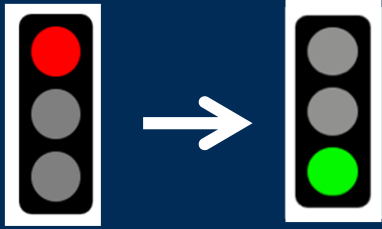
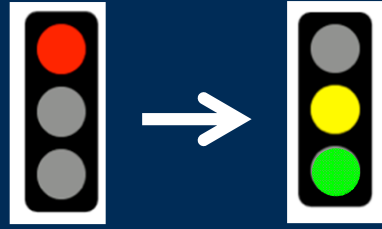
2009
Defect-tolerant logic gates
[USC]



2010
Ultra-short channel CNFETs
[IBM]



CNFET Technology Outlook

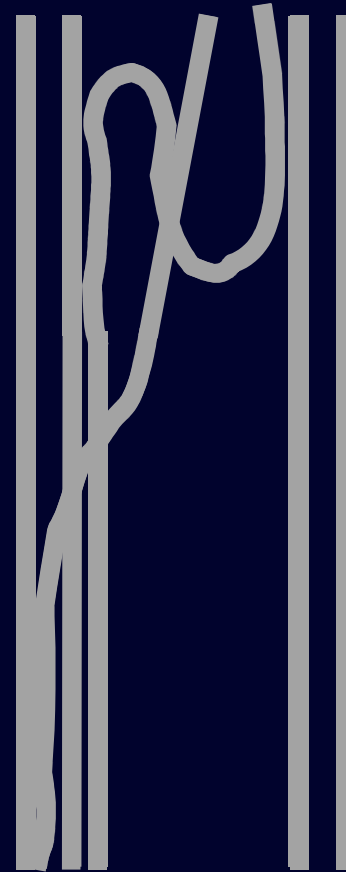
Problem	Challenge	Status
CNT alignment & positioning	Correct function	
Metallic CNT	Correct function Low leakage	
CNT density	High current density	
CNT doping	Complementary CNFETs	

Outline

- Introduction
- Mis-positioned-CNT-immune logic
- Metallic-CNT-immune logic
- CNT variations
- Conclusion

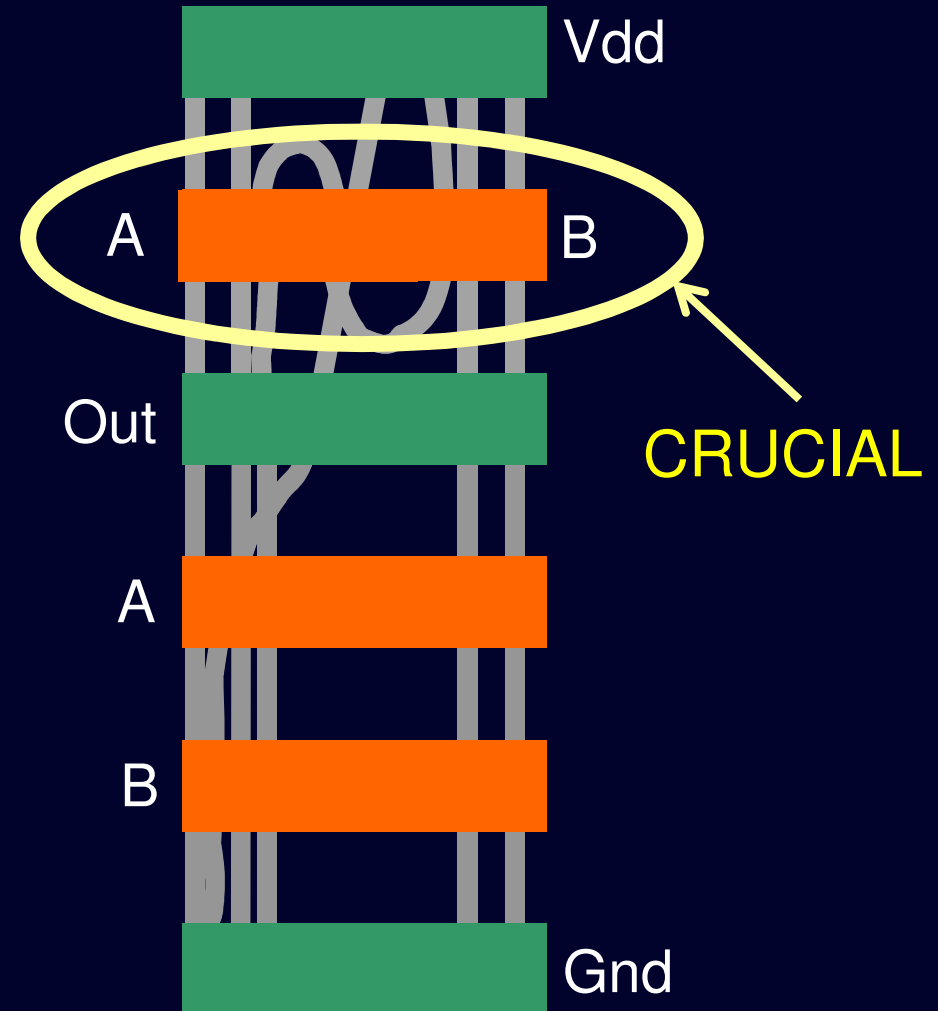
Mis-positioned-CNT-Immune NAND

1. Grow CNTs



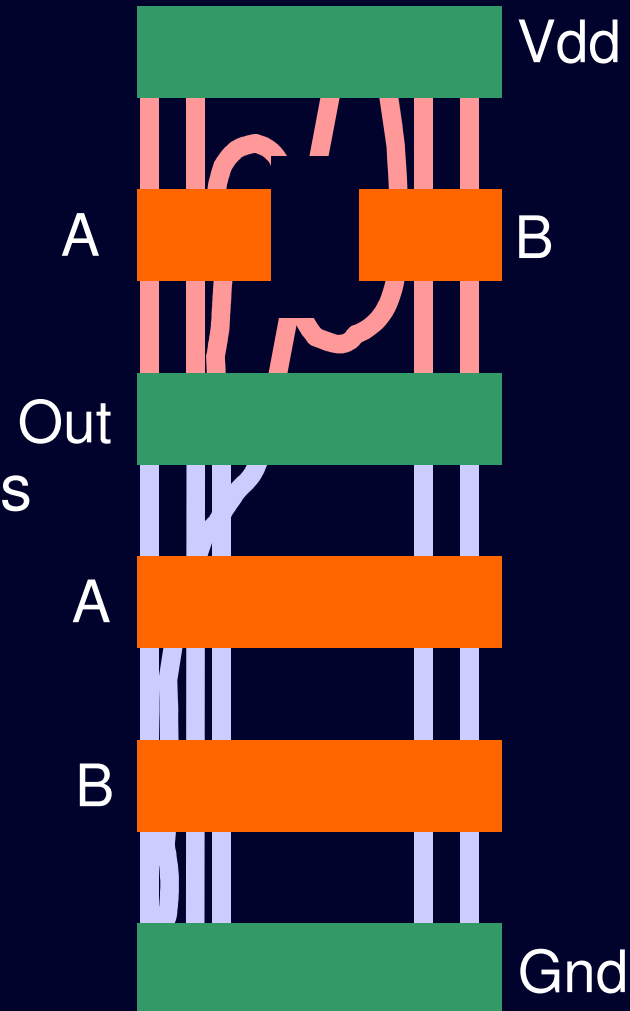
Mis-positioned-CNT-Immune NAND

1. Grow CNTs
2. Extended gate & contacts



Mis-positioned-CNT-Immune NAND

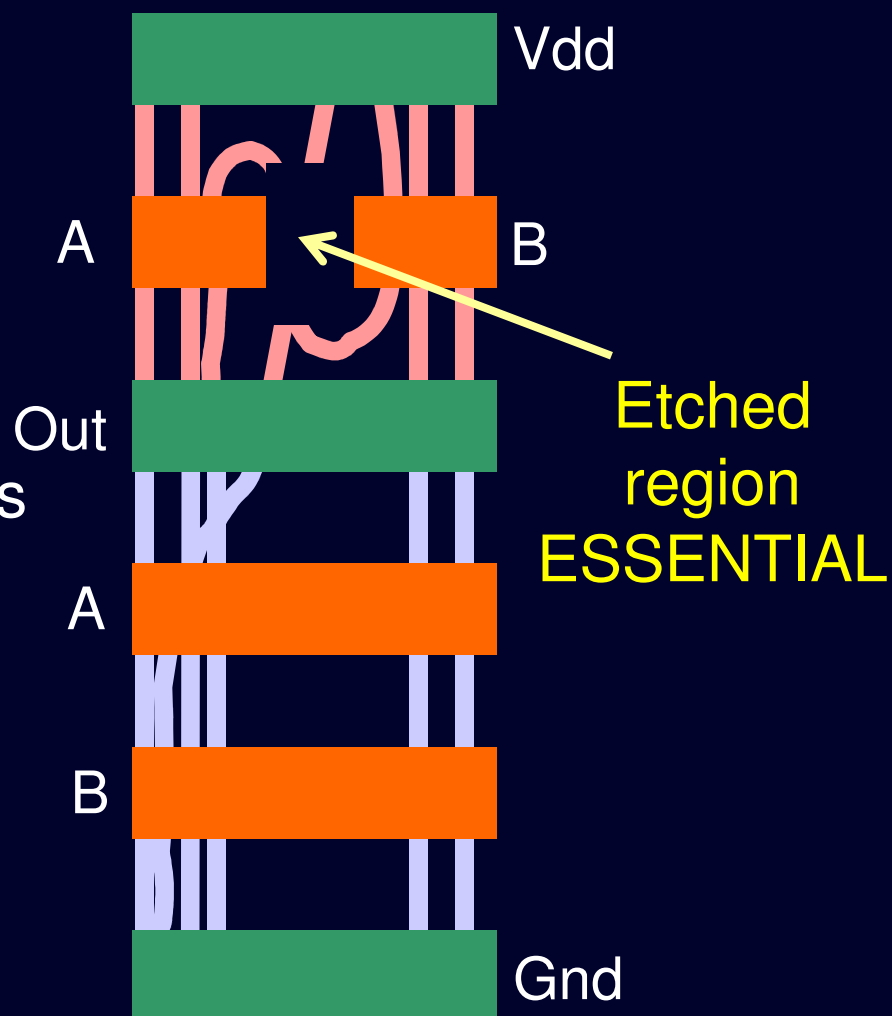
1. Grow CNTs
2. Extended gate & contacts
3. Etch gate & CNTs
4. Chemically dope P & N regions



Mis-positioned-CNT-Immune NAND

1. Grow CNTs
2. Extended gate & contacts
3. Etch gate & CNTs
4. Chemically dope P & N regions

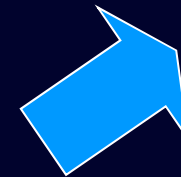
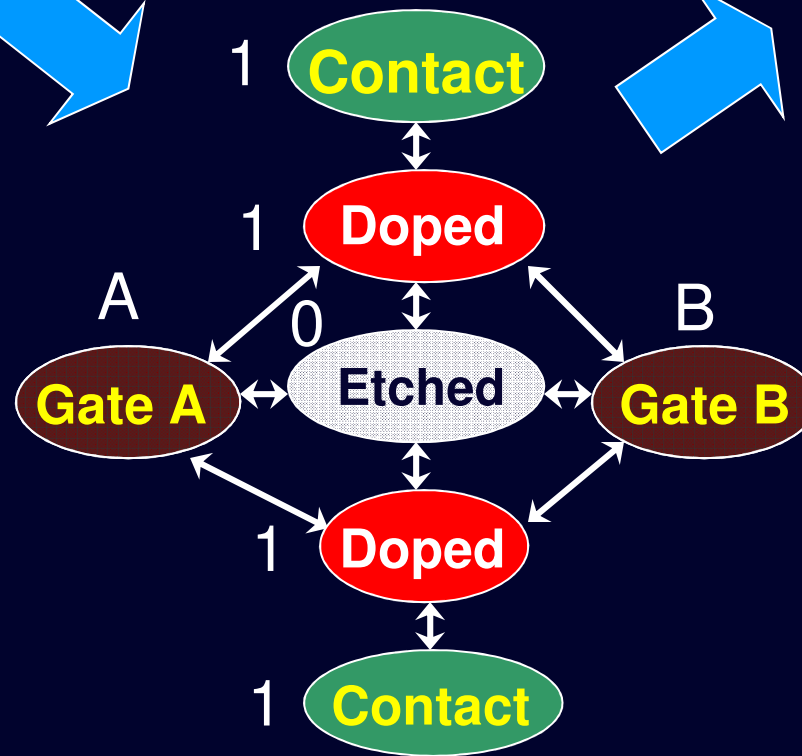
- Graph algorithms
 - All possible functions



Automated Algorithms

- Given: Layout
 - Determine
 - Mis-positioned-CNT immune ?

Mis-positioned-CNT-Immune NAND



Contact

A   B

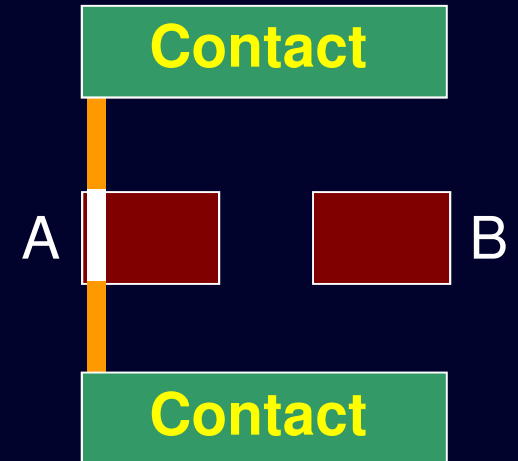
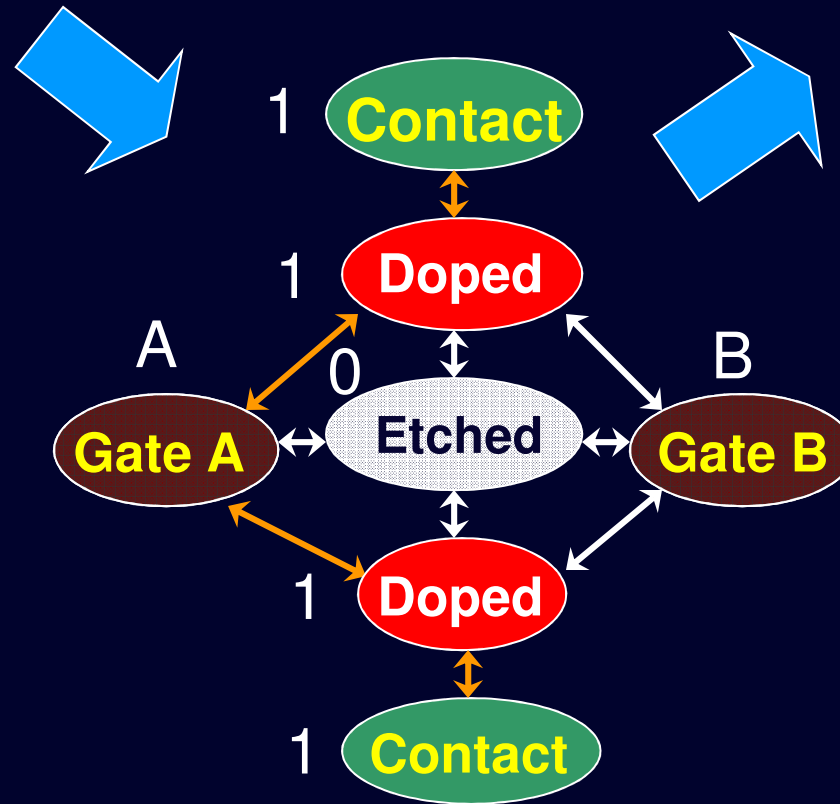
Contact

Intended:
A or B

Mis-positioned-CNT-Immune NAND



C-D-A-D-C : A



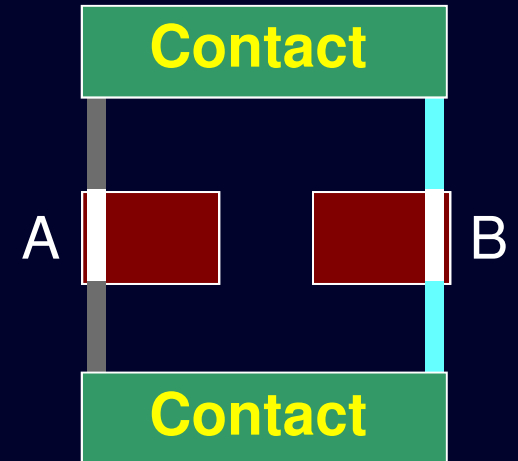
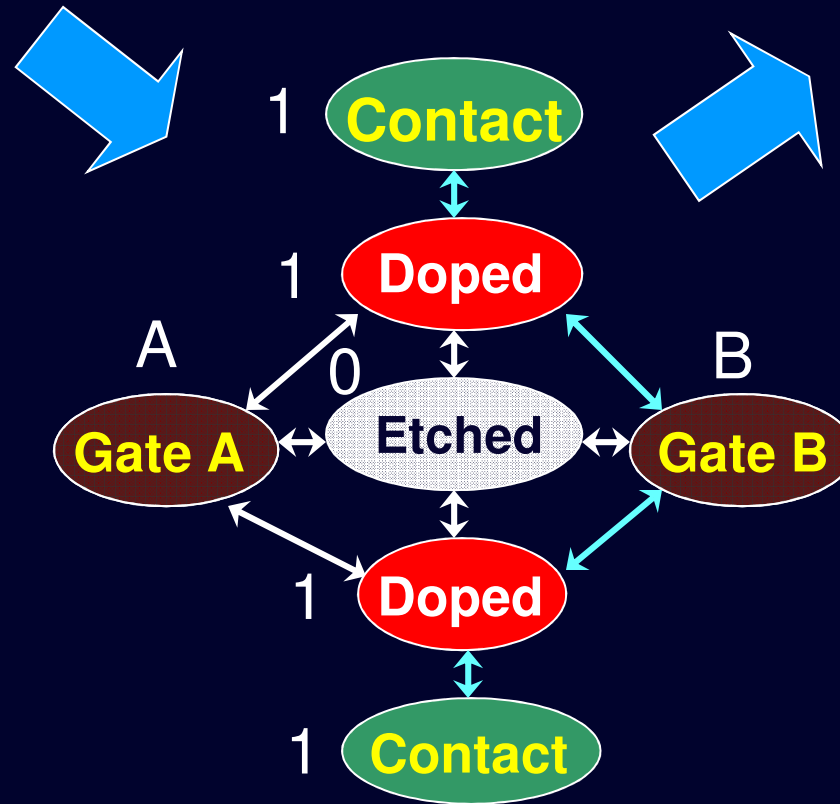
Intended:
A or B

Mis-positioned-CNT-Immune NAND



C-D-A-D-C : A

C-D-B-D-C : B

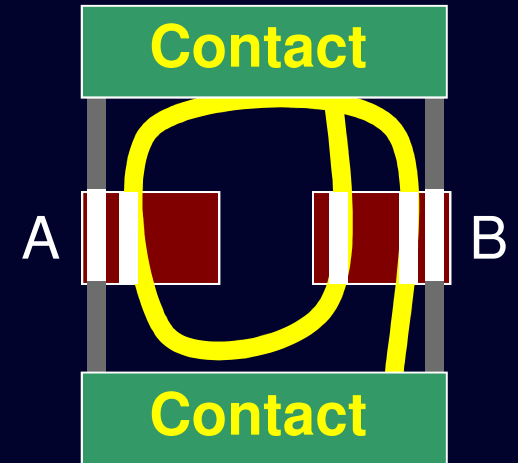
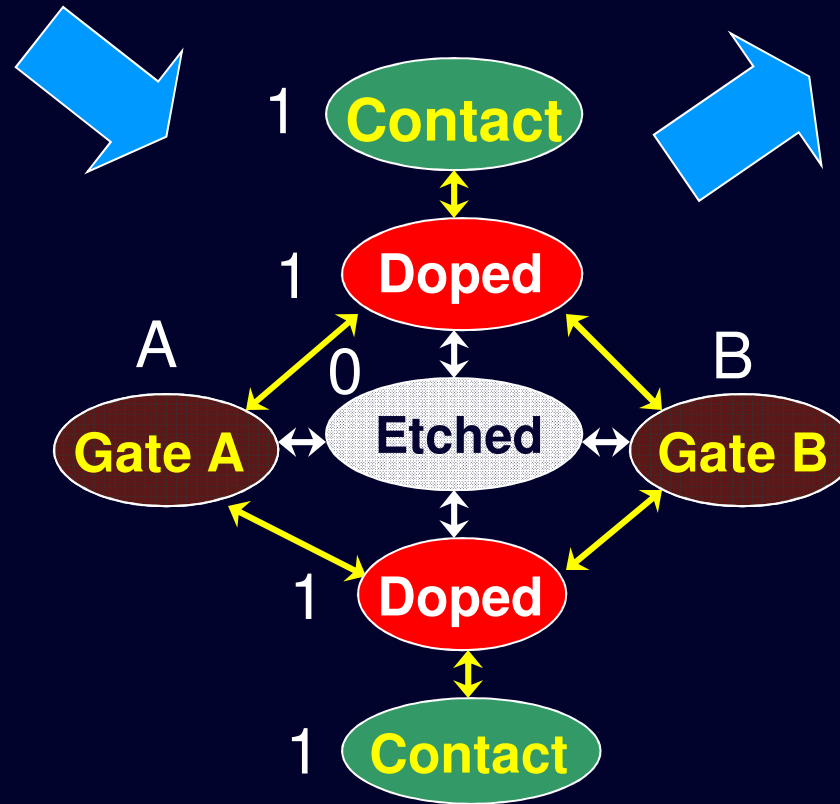


Intended:
A or B

Mis-positioned-CNT-Immune NAND



C-D-A-D-C : A
 C-D-B-D-C : B
 C-D-B-D-A-D-B-D-C : A & B

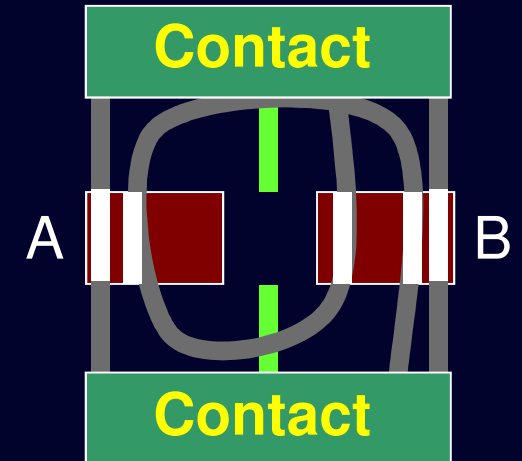
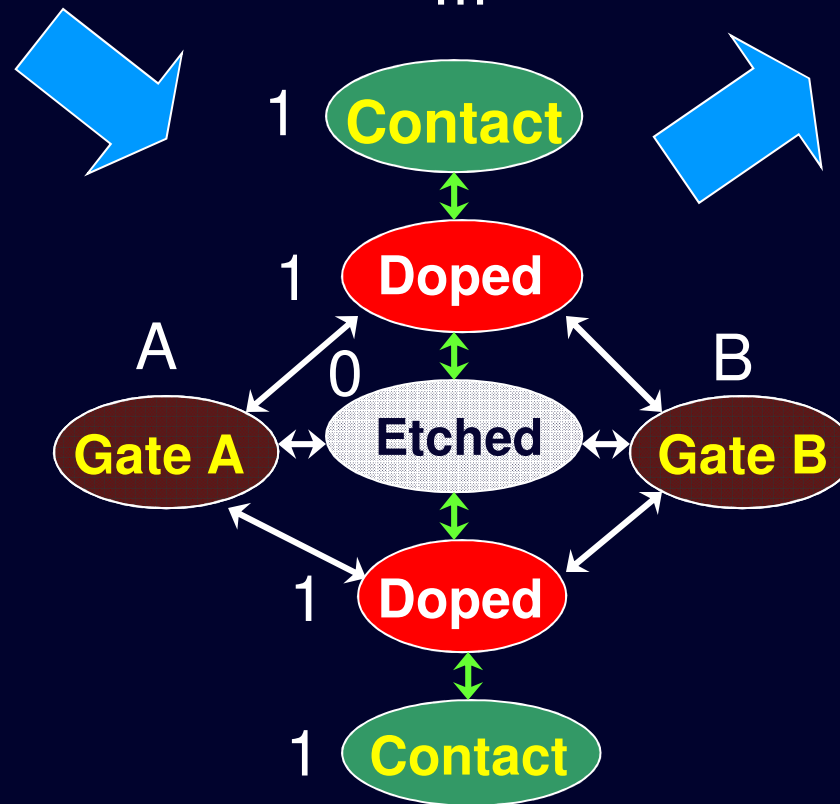


Intended:
A or B

Mis-positioned-CNT-Immune NAND



C-D-A-D-C : A
 C-D-B-D-C : B
 C-D-B-D-A-D-B-D-C : A & B
 C-D-E-D-C : 0

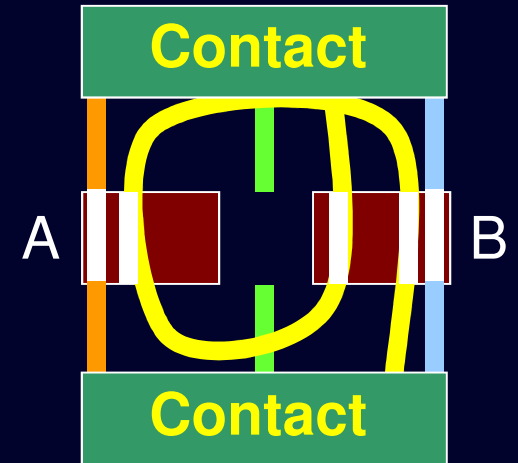
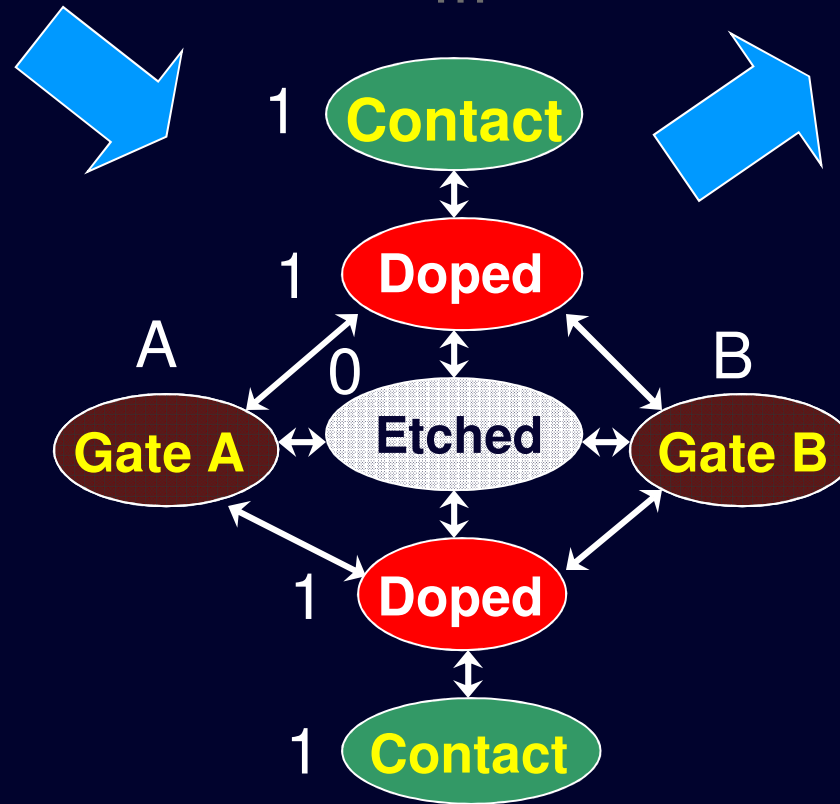


Intended:
A or B

Mis-positioned-CNT-Immune NAND



C-D-A-D-C : A
 C-D-B-D-C : B
 C-D-B-D-A-D-B-D-C : A & B
 C-D-E-D-C : 0



Intended:

A or B

Implemented:

A or B or (A & B) or 0

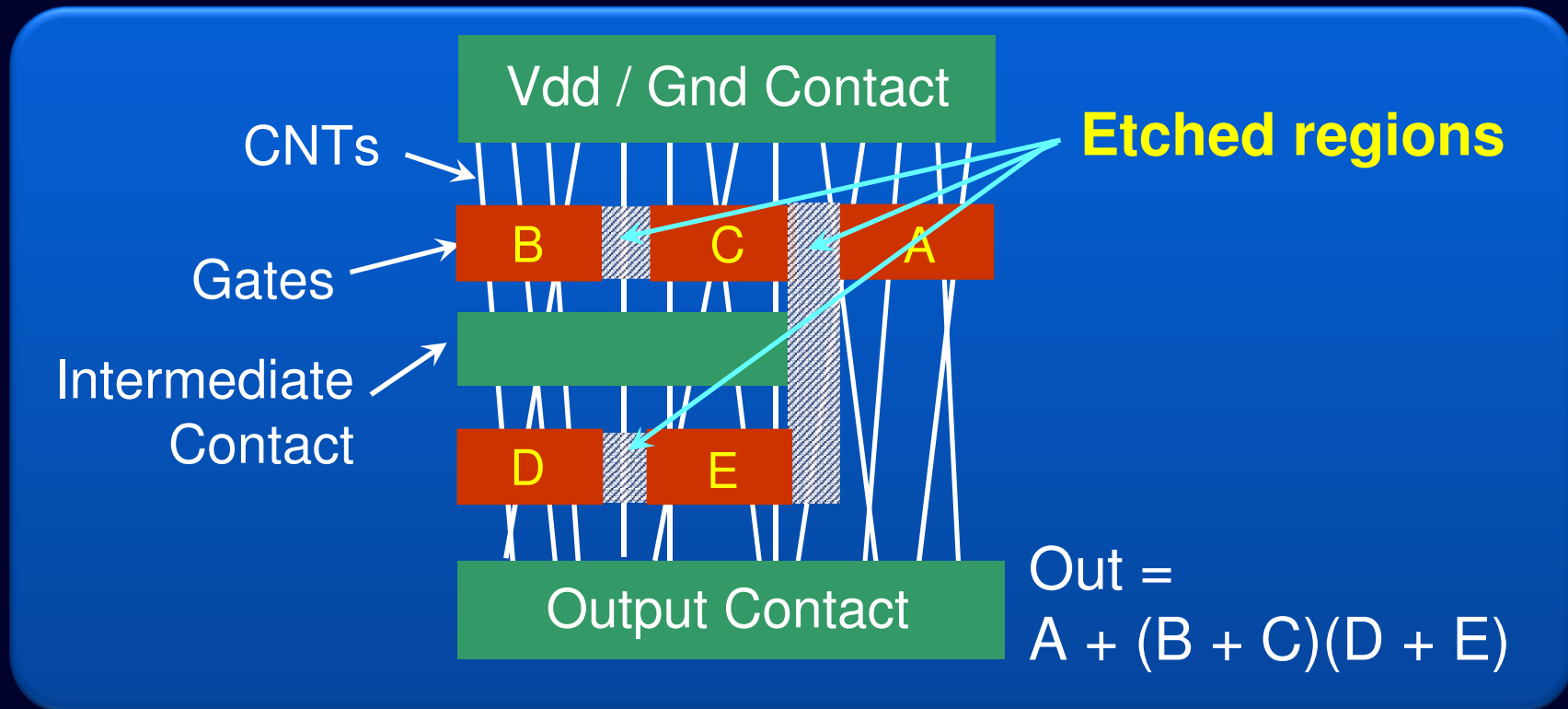
==

A or B

Automated Algorithms

- Given: Logic function
 - Produce
 - Mis-positioned-CNT immune layout

Mis-positioned-CNT-Immune Layout



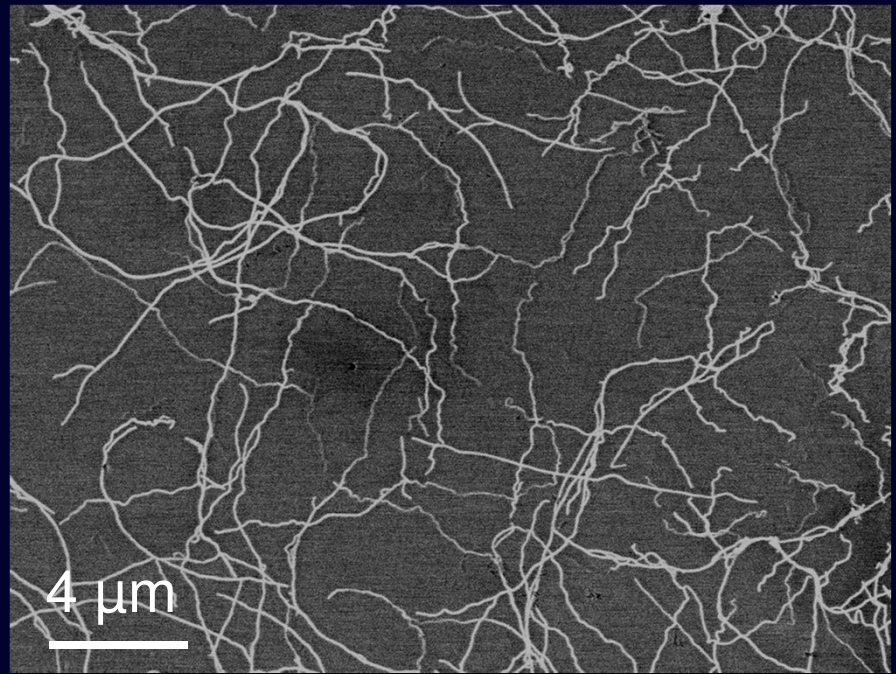
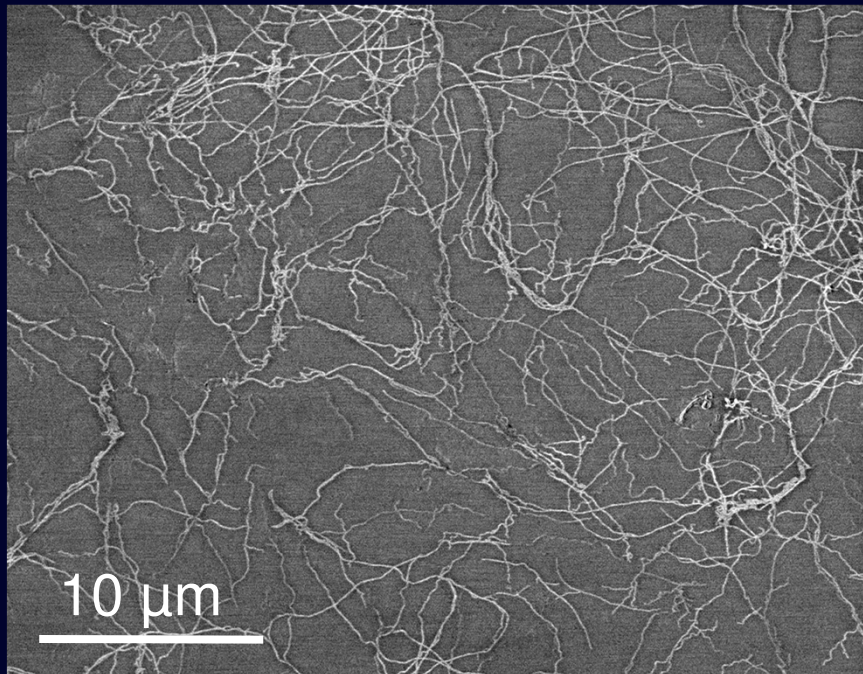
- Immune to **LARGE** number of mis-positioned CNTs
- Efficient

Most Importantly

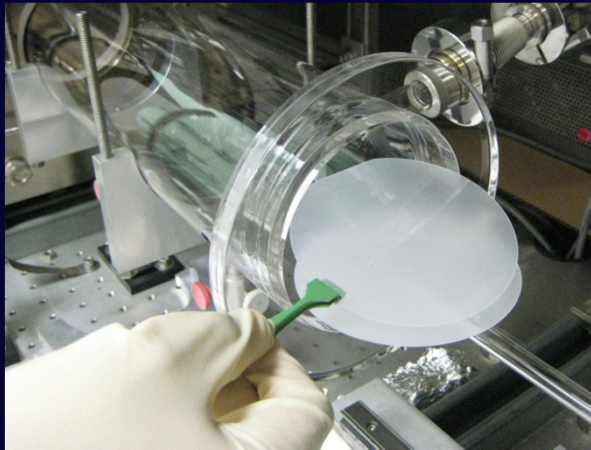
- VLSI processing
 - No die-specific customization
- VLSI design flow
 - Immune library cells

CNT Growth on Silicon Substrates

- Highly mis-positioned
 - Not desirable for VLSI



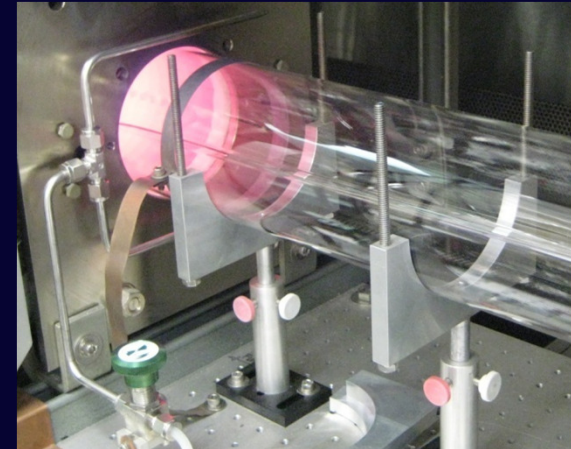
First Wafer-Scale Aligned CNT Growth



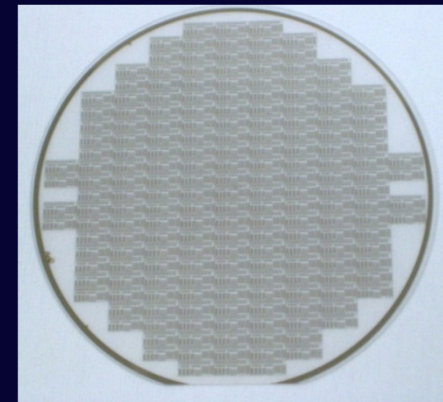
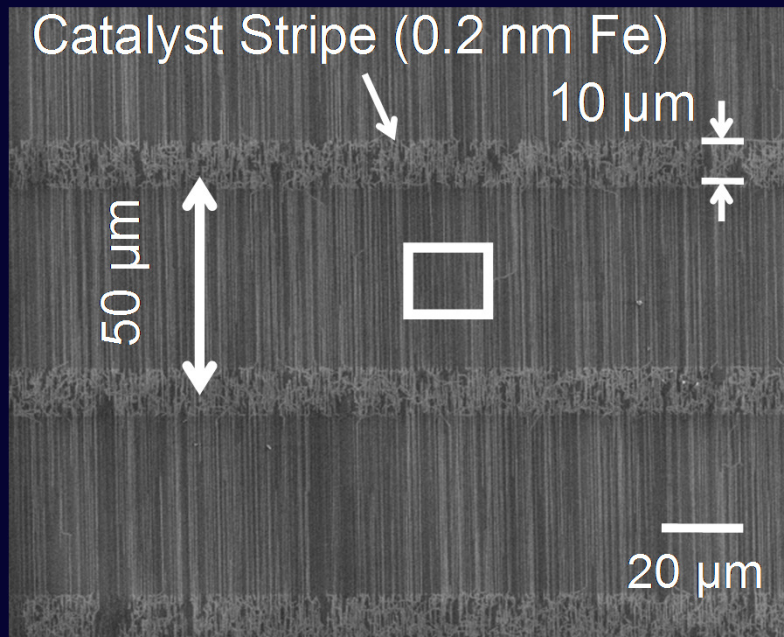
Quartz wafer
with catalyst



Aligned
CNT growth



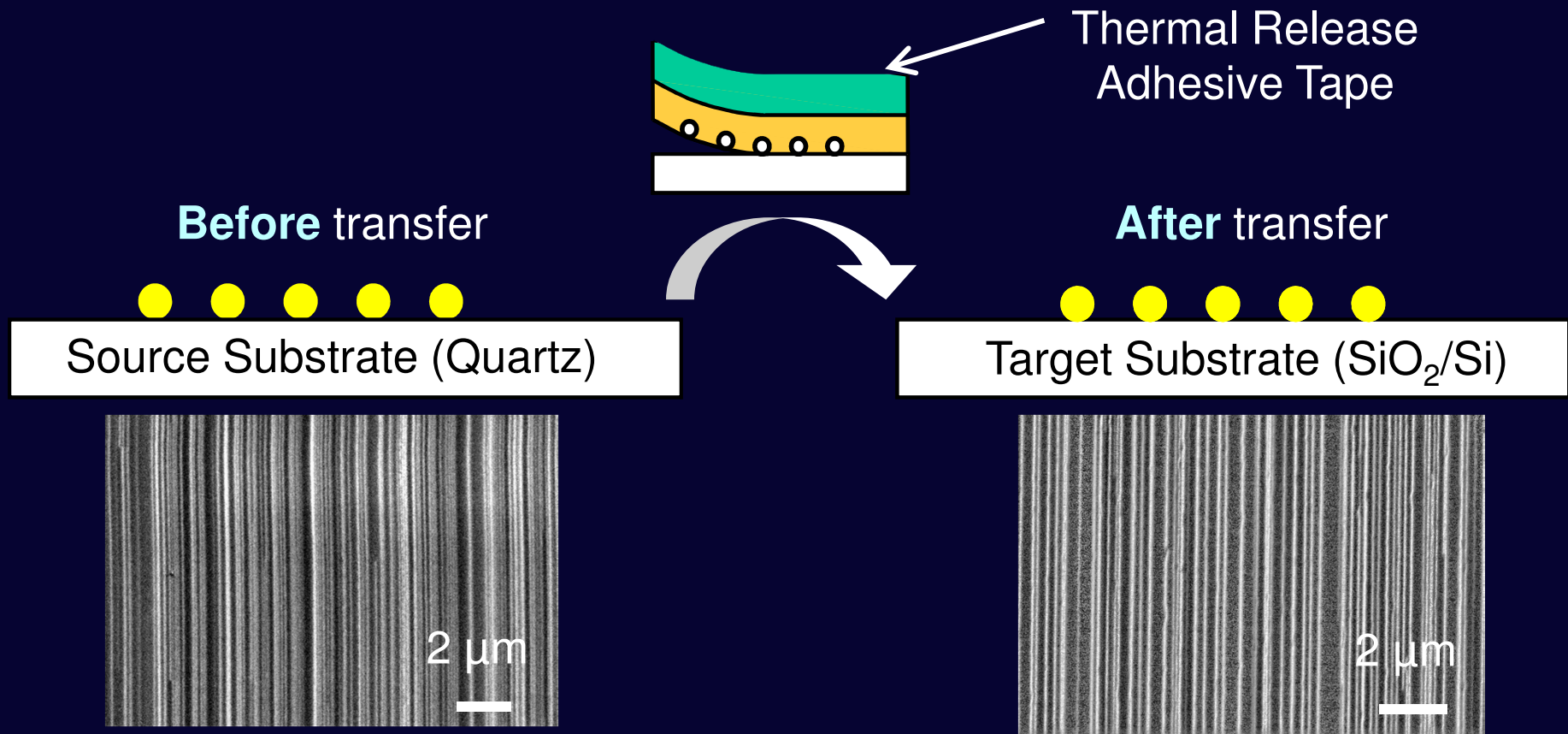
SEM image (grown CNTs)



Quartz wafer
99.5% CNTs aligned

Wafer-Scale CNT Transfer

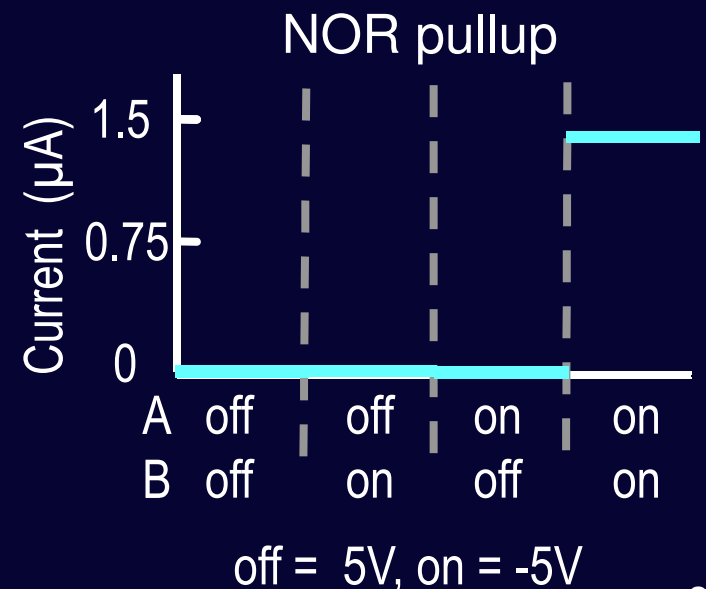
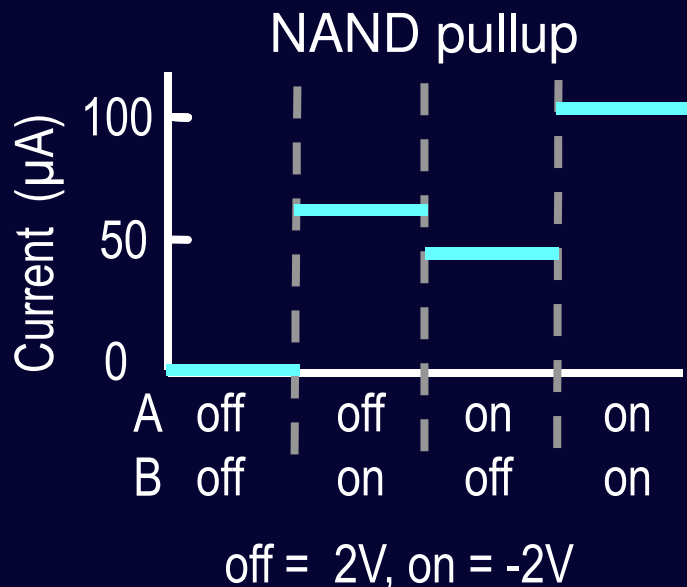
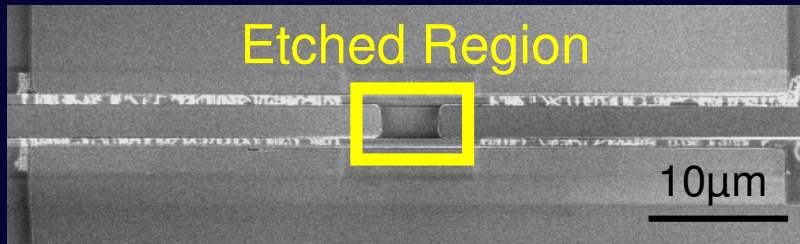
- Silicon substrates for VLSI
- Low temperature (90°C – 120°C) processing



First VLSI Demonstration

Mis-positioned-CNT-immune logic gates

NAND, NOR, AND-OR-INV, OR-AND-INV



Outline

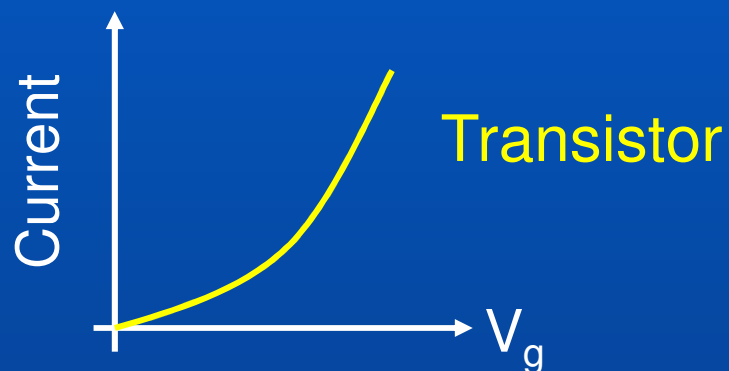
- Introduction
- Mis-positioned-CNT-immune logic
- **Metallic-CNT-immune logic**
- CNT variations
- Conclusion

Metallic CNTs

Semiconducting CNT (s-CNT)



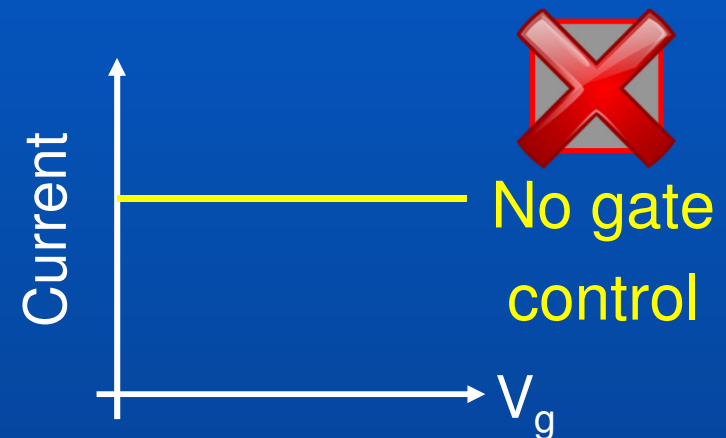
CNFET with s-CNT



Metallic CNT (m-CNT)



CNFET with m-CNT



Typical: 10 – 50% grown CNTs metallic

m-CNT Processing Options

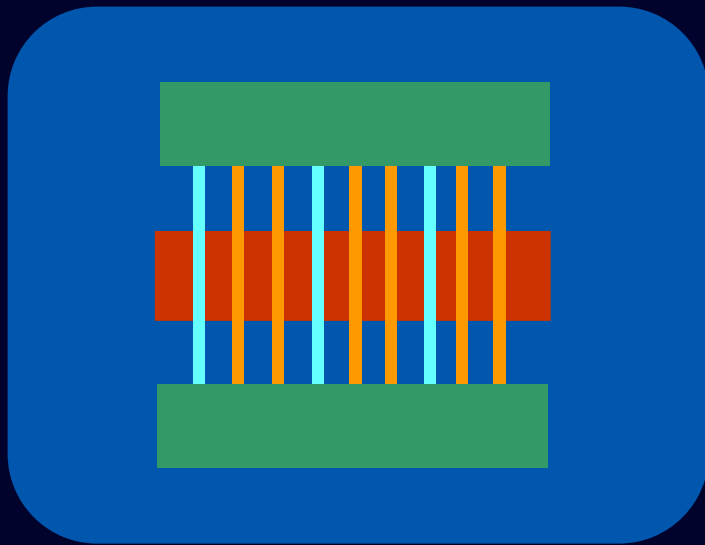
- Grow 0% m-CNTs
 - Open challenge
- Remove m-CNTs after growth
 - 99.99% removal required

Existing m-CNT Removal

- Sort CNTs
 - Inadequate 
- SDB
 - Single Device electrical Breakdown
 - Not scalable 

SDB Technique

- Current-induced m-CNT breakdown
 - Single-device level



— s-CNTs
— m-CNTs

Collins, Science 2001

SDB Technique

- Current-induced m-CNT breakdown
 - Single-device level

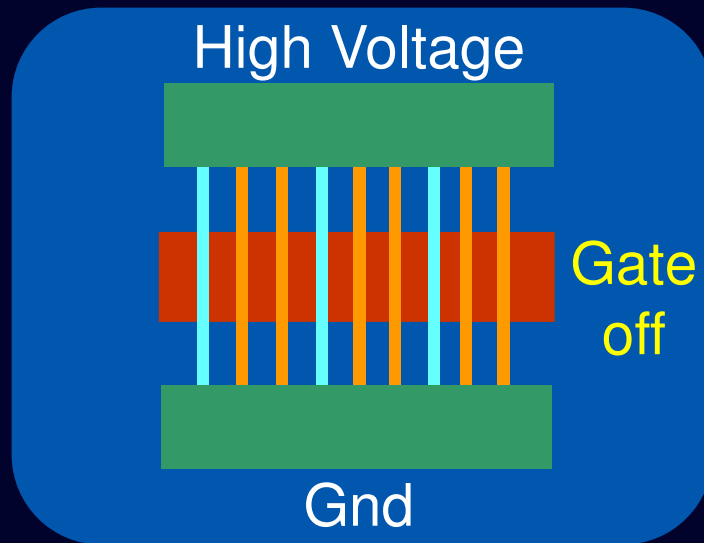


— s-CNTs
— m-CNTs

Collins, Science 2001

SDB Technique

- Current-induced m-CNT breakdown
 - Single-device level

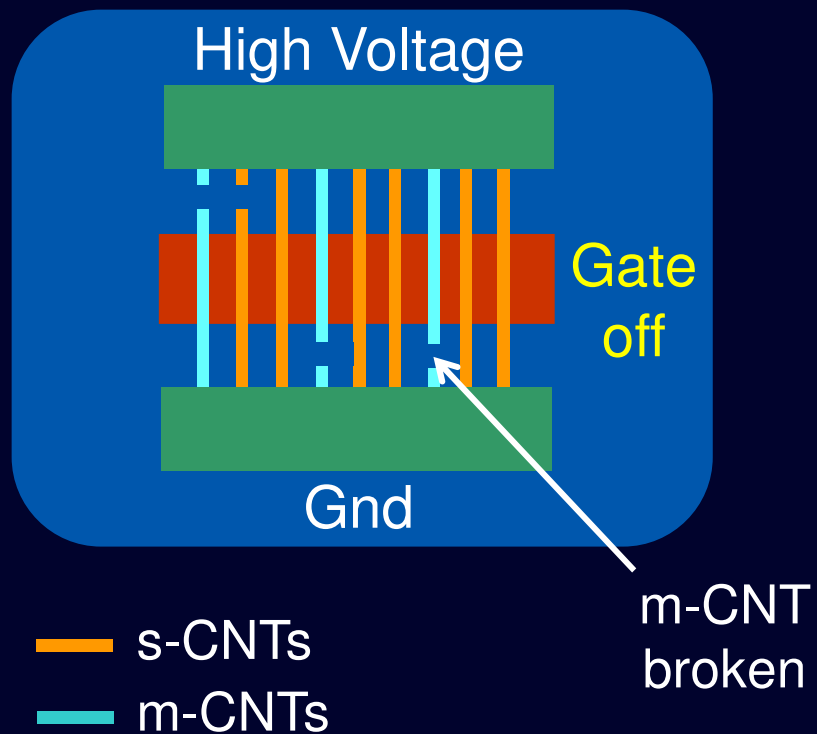


— s-CNTs
— m-CNTs

Collins, Science 2001

SDB Technique

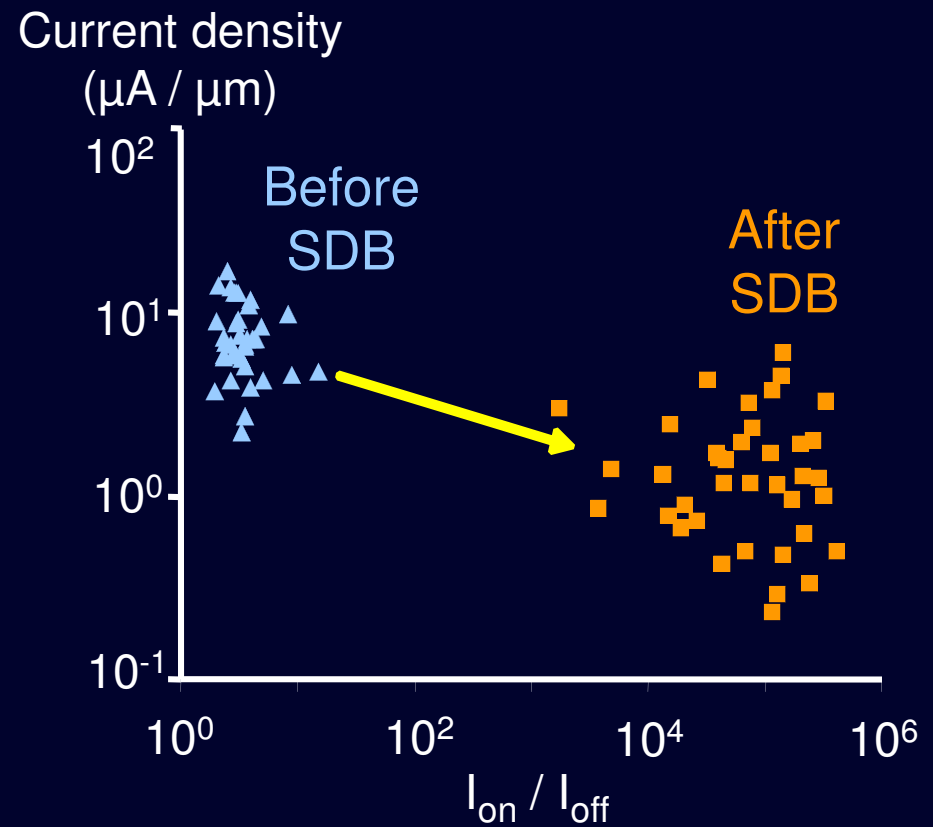
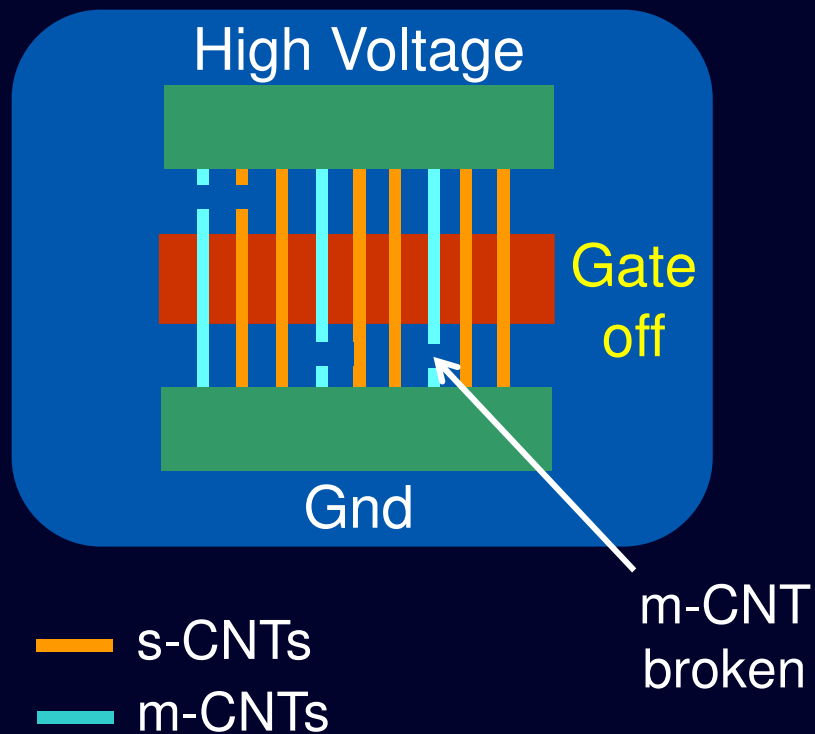
- Current-induced m-CNT breakdown
 - Single-device level



Collins, Science 2001

SDB Technique

- Current-induced m-CNT breakdown
 - Single-device level



Collins, Science 2001

Major SDB Challenges

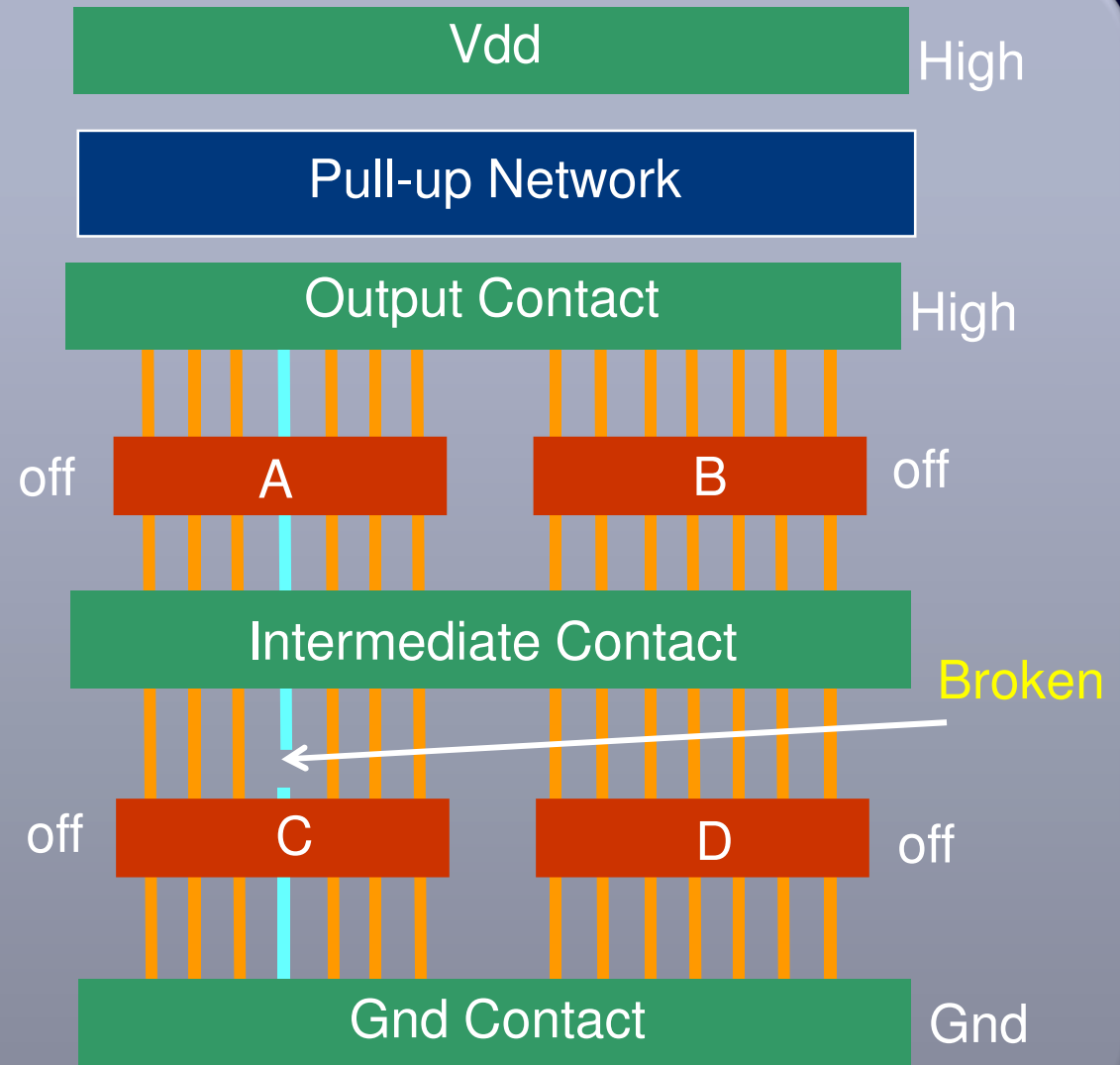
- Incorrect logic
 - m-CNT fragments
- Impractical for giga-scale ICs
 - Internal node access

Incorrect Logic with SDB

Wanted:
 $(A + B) \cdot (C + D)$

Got:
 $(C + D)$

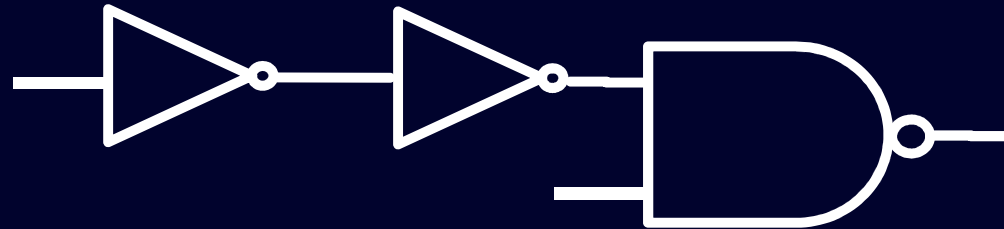
Incorrect Logic !



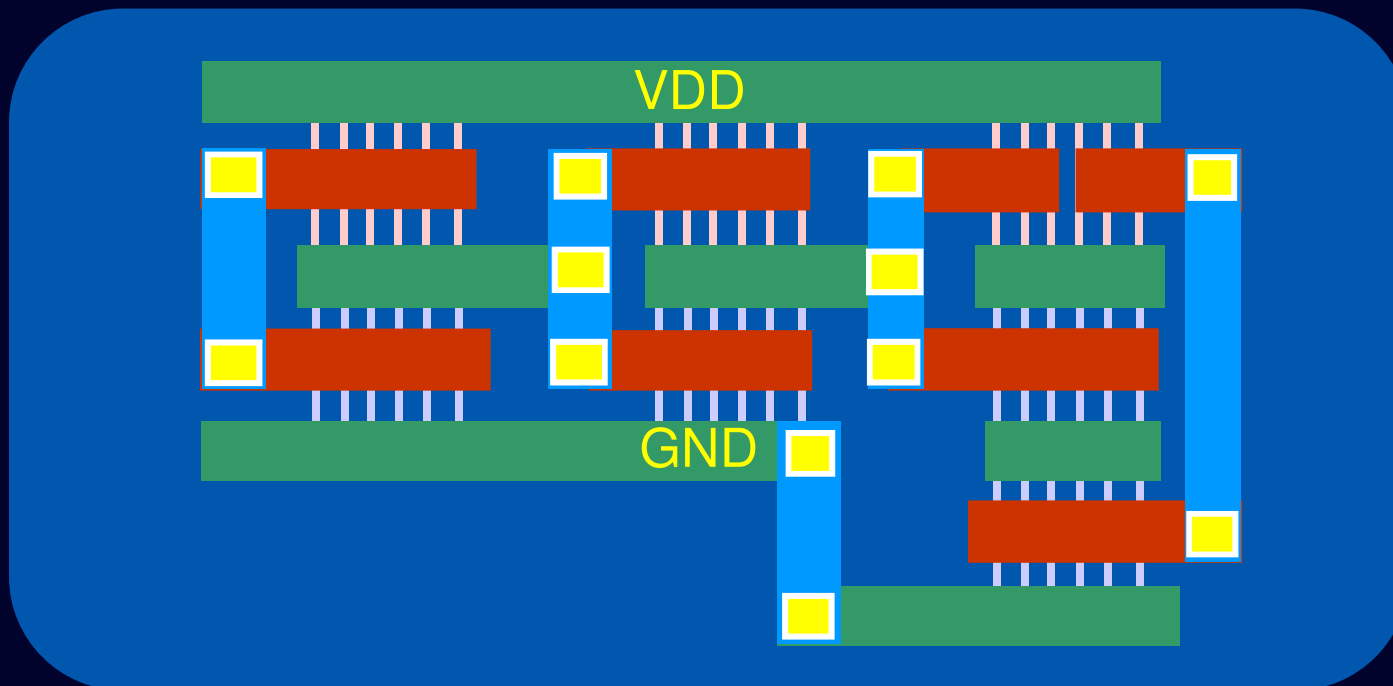
VMR: m-CNT Immune Design

- New approach: VLSI Metallic CNT Removal
 - Sufficient
 - All logic designs
 - VLSI processing & design flows

VMR Example



Final intended design



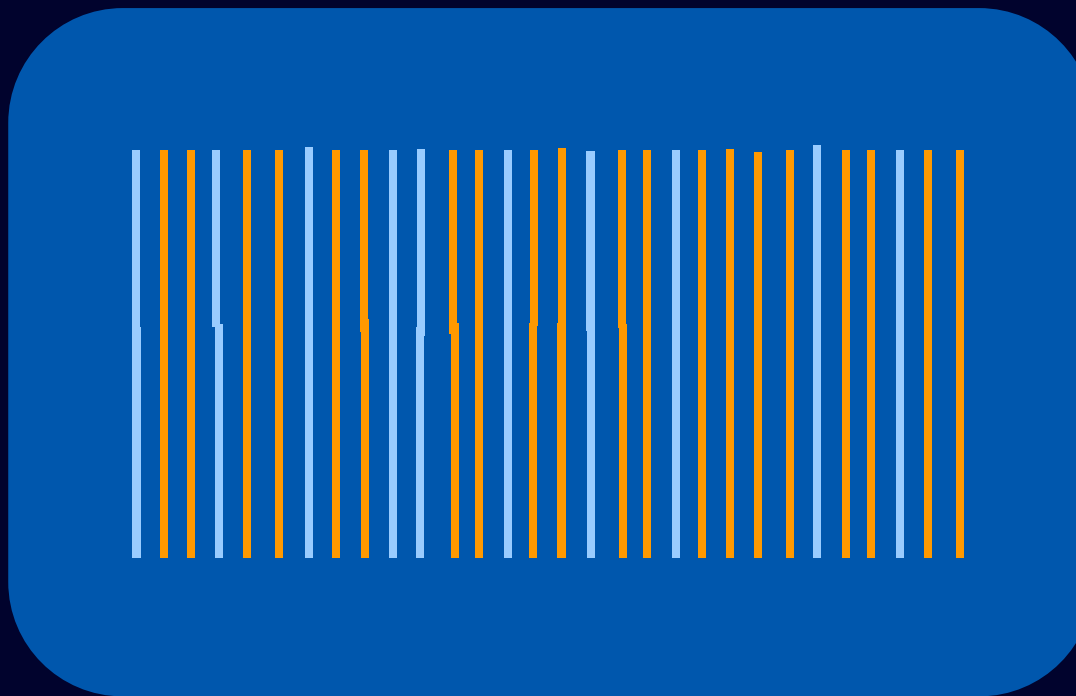
VMR Steps

1. Grow and transfer CNTs

- s-CNTs
- m-CNTs
(no gate control)

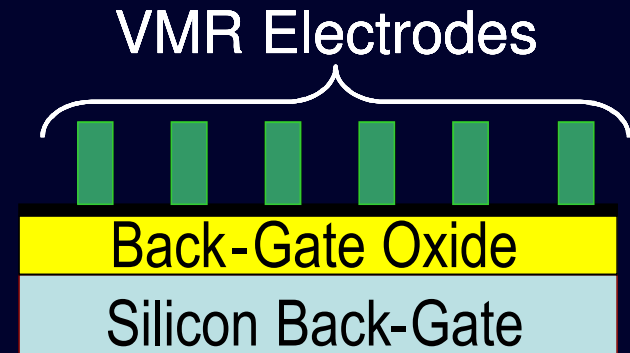
Back-Gate Oxide

Silicon Back-Gate



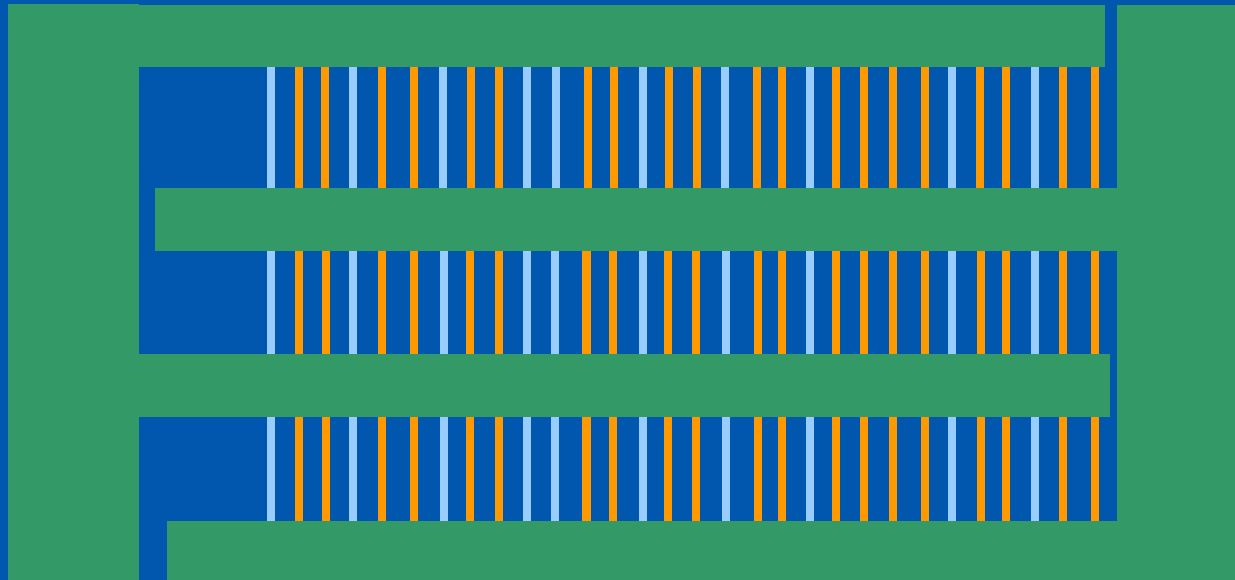
VMR Steps

1. Grow and transfer CNTs
2. Fabricate VMR electrodes



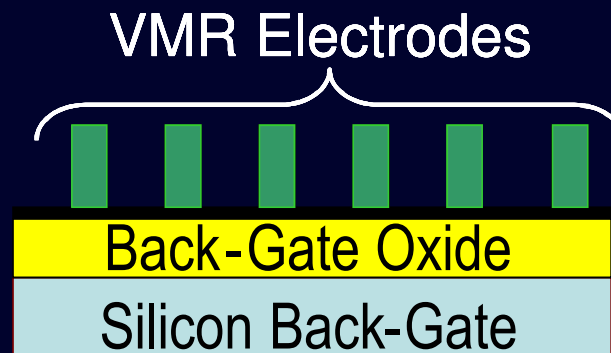
Inter-digitated VMR electrodes

Electrical breakdown friendly



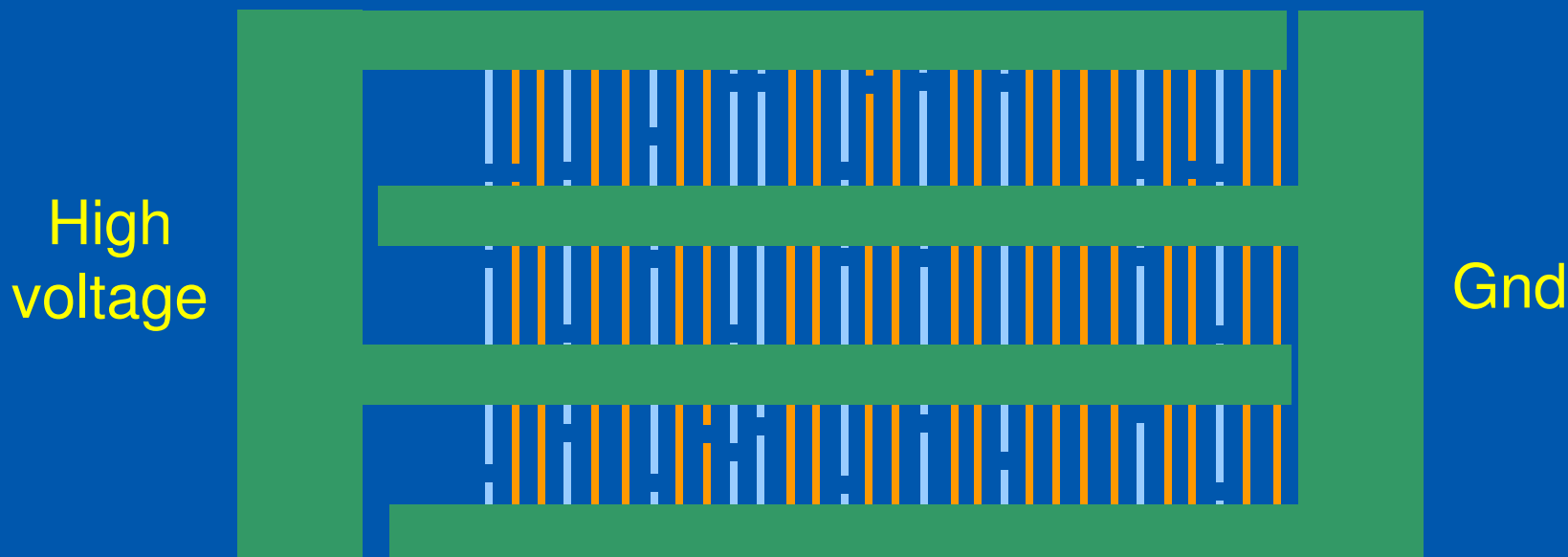
VMR Steps

1. Grow and transfer CNTs
2. Fabricate VMR electrodes
3. Electrical breakdown (back-gate)



Inter-digitated VMR electrodes

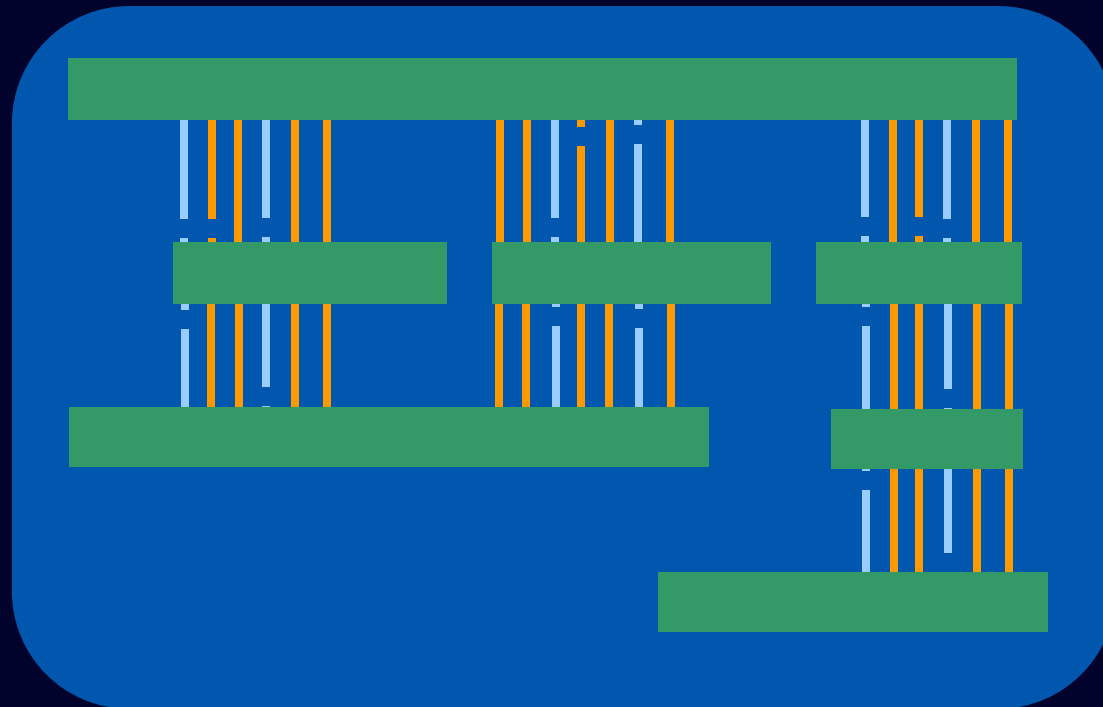
Electrical breakdown friendly



VMR Steps

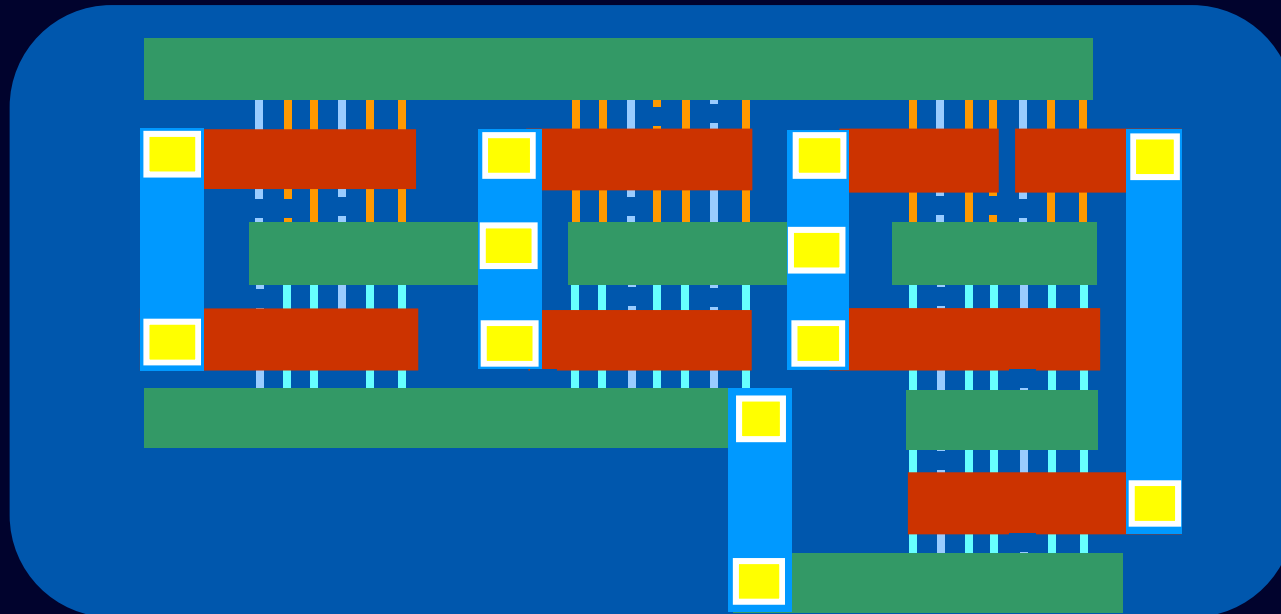
1. Grow and transfer CNTs
2. Fabricate VMR electrodes
3. Electrical breakdown (back-gate)
4. Etch CNTs : predefined regions
(mis-positioned-CNT-immune design)
5. Etch unneeded VMR electrodes

CNFET
contacts
not
removed



VMR Steps

1. Grow and transfer CNTs
2. Fabricate VMR electrodes
3. Electrical breakdown (back-gate)
4. Etch CNTs : predefined regions
(mis-positioned-CNT-immune design)
5. Etch unneeded VMR electrodes
6. Top-gates (mis-positioned-CNT-immune design), doping, wires



Theorem

- VMR works for arbitrary logic design

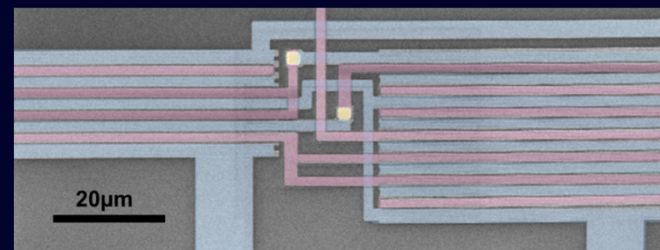
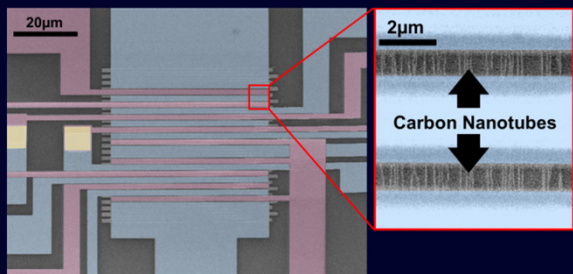
if

- Any two transistors in series
 - Connected through contact
 - Minimum pitch
- Immune library cells: very small impact

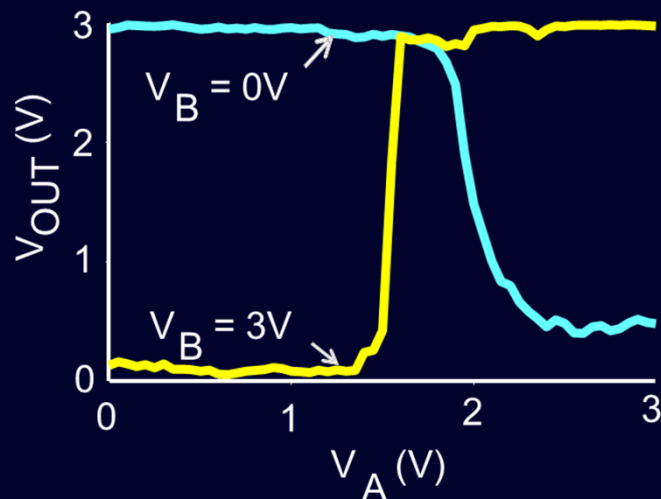
First Experimental Demonstration

Imperfection-immune CNT VLSI circuits

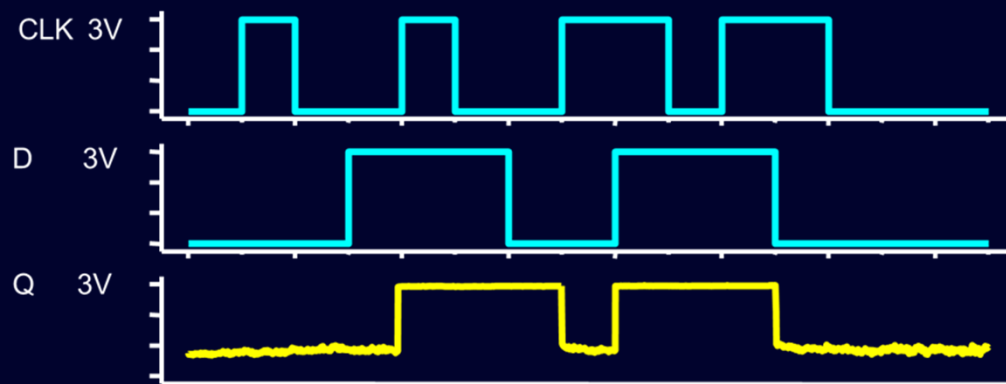
Arithmetic & storage elements



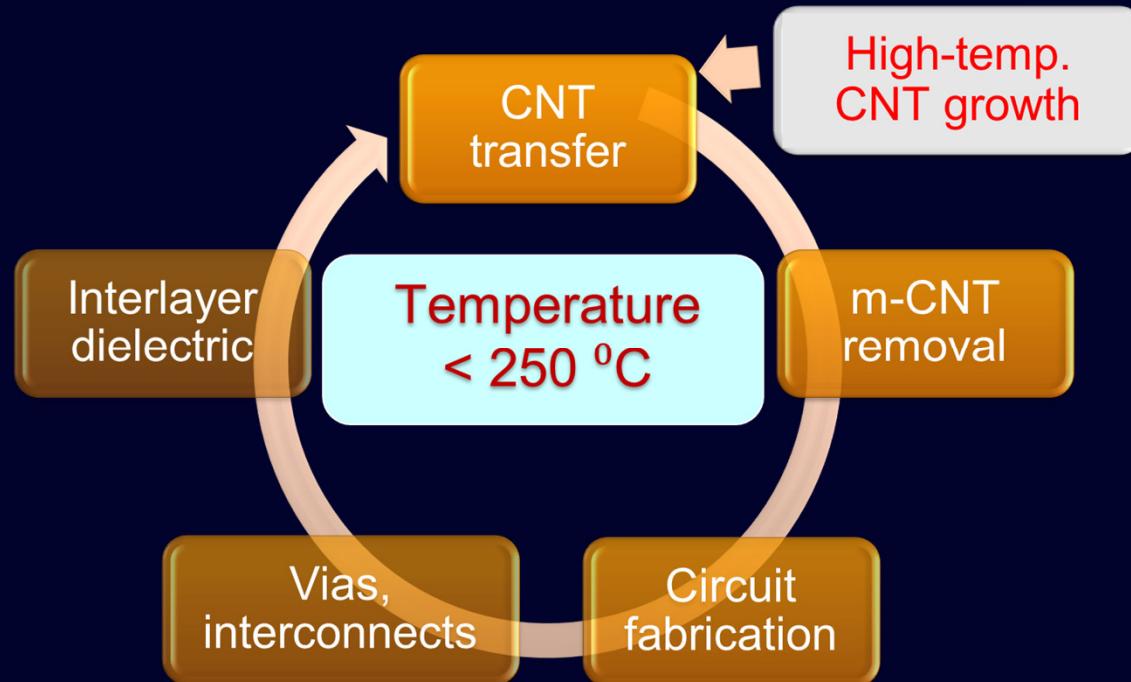
Half-adder Sum



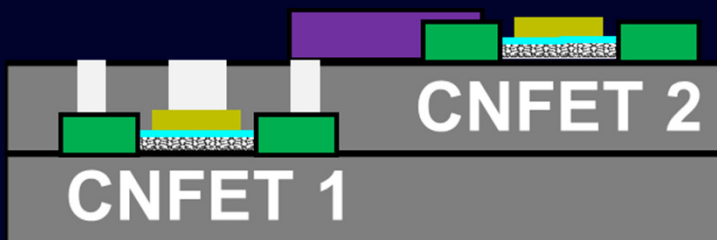
D-latch



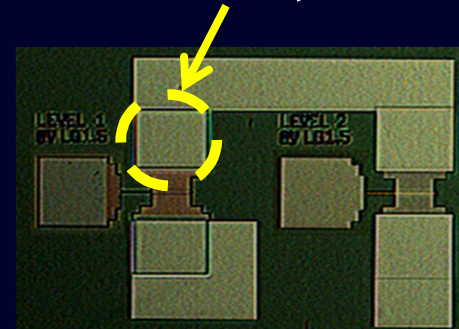
First Monolithic CNT 3D ICs



2-layer CNT XOR



Conventional via, NOT TSV



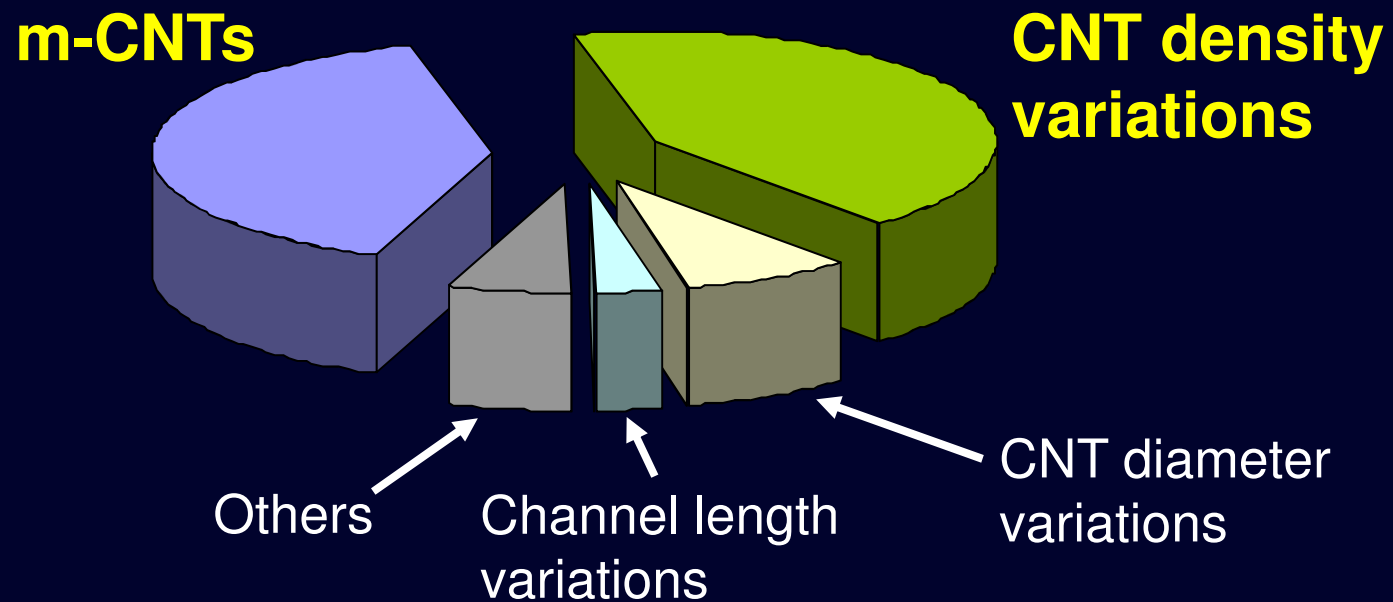
Outline

- Introduction
- Mis-positioned-CNT-immune logic
- Metallic-CNT-immune logic
- CNT variations
- Conclusion

CNT Variations Challenging

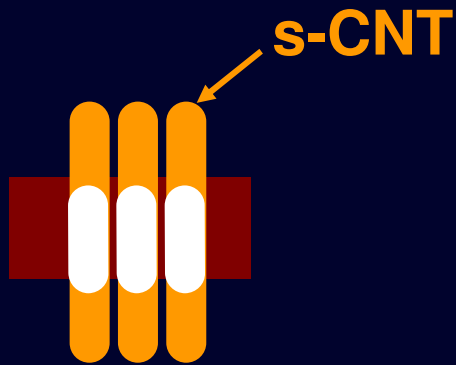
- Probabilistic modeling essential [Borkar 07]

CNFET I_{on} variations

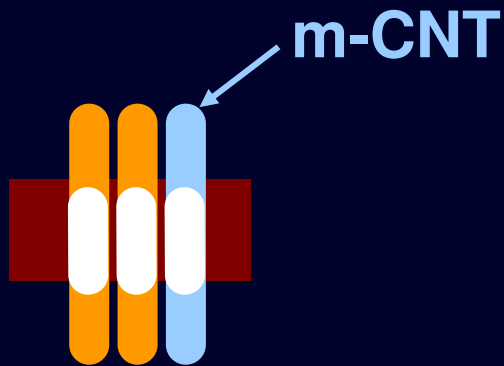


Probabilistic CNT Growth Model

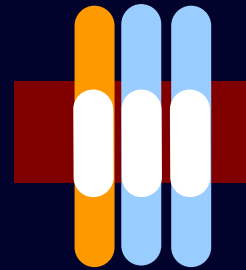
- Probability (m-CNT) = p_m
- Probability (s-CNT) = $p_s = 1 - p_m$



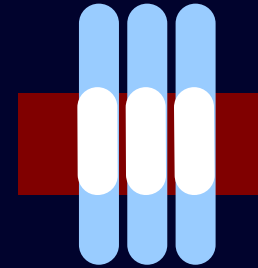
$$\left(\frac{2}{3}\right)^3 = 0.3$$



$$3 \left(\frac{1}{3}\right) \left(\frac{2}{3}\right)^2 = 0.44$$

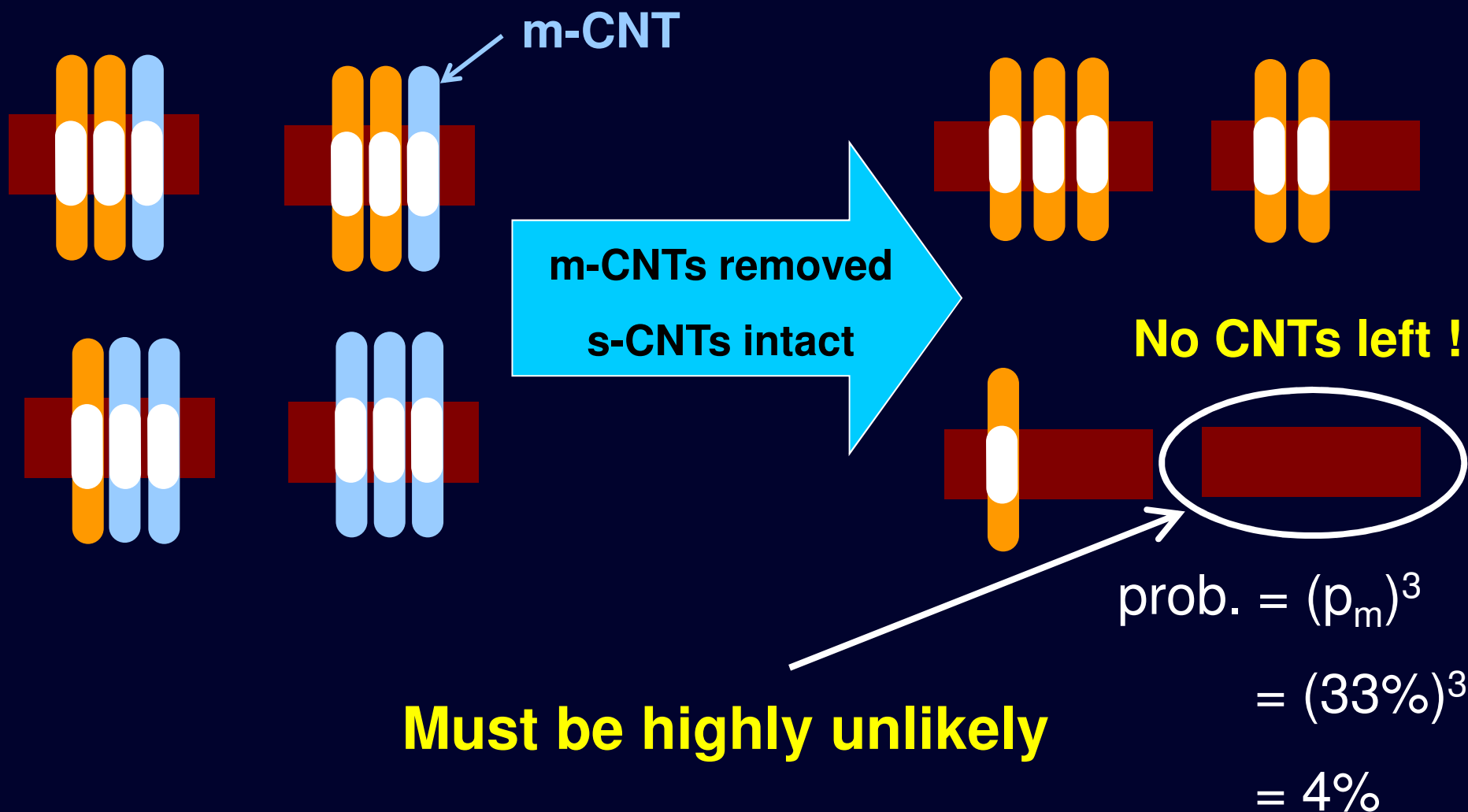


$$3 \left(\frac{2}{3}\right) \left(\frac{1}{3}\right)^2 = 0.22$$



$$\left(\frac{1}{3}\right)^3 = 0.04$$

m-CNT Removal Alone Inadequate



Probabilistic Design a MUST

Processing



- % grown m-CNTs
- CNT density variations

Design



- Special layouts
- CNFET sizing

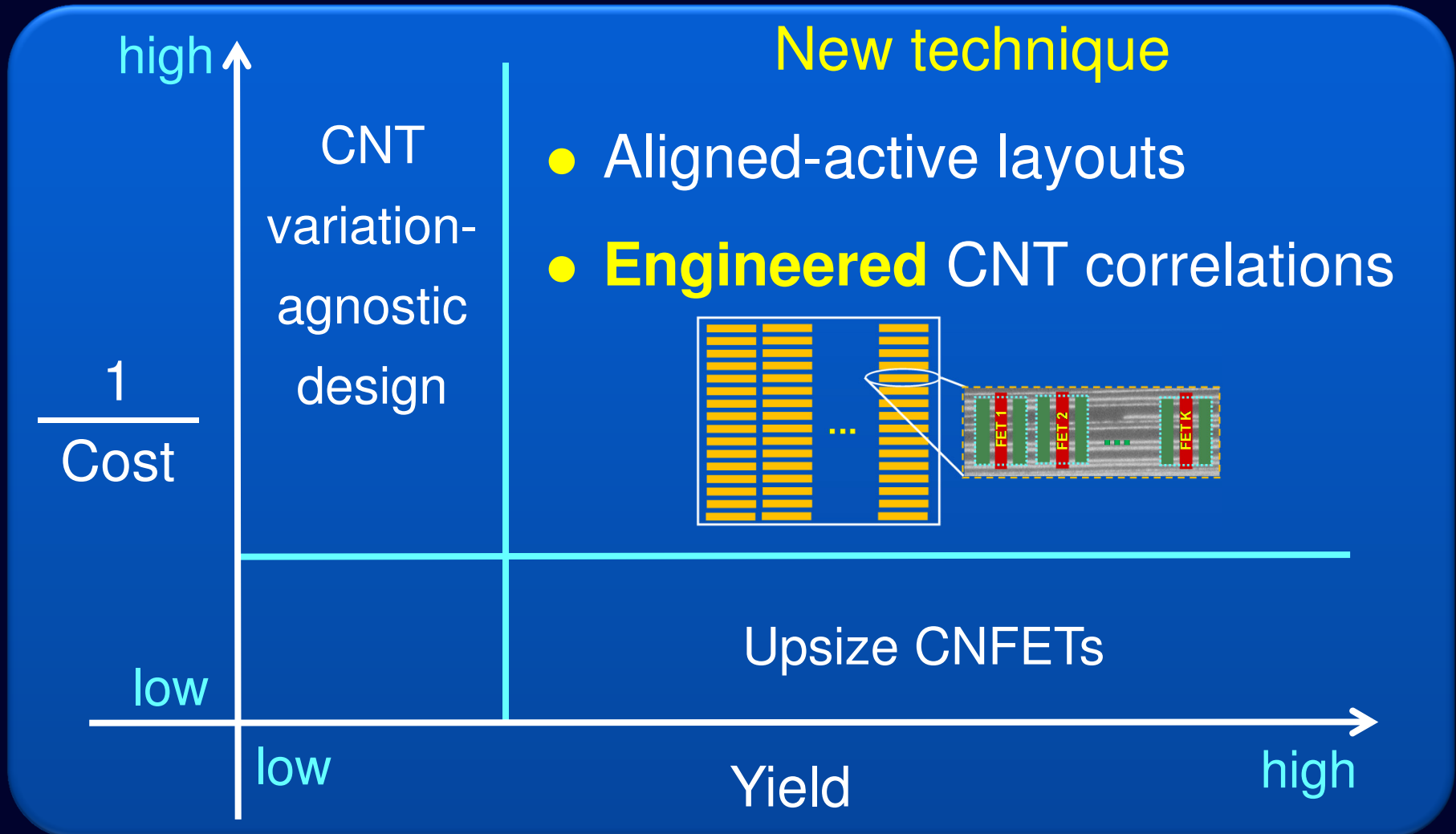
Processing & Design Co-Optimization

Noise margin

Leakage

Delay variations

Special Layouts



Outline

- Introduction
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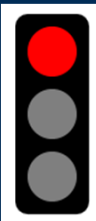
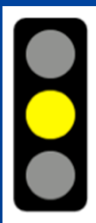
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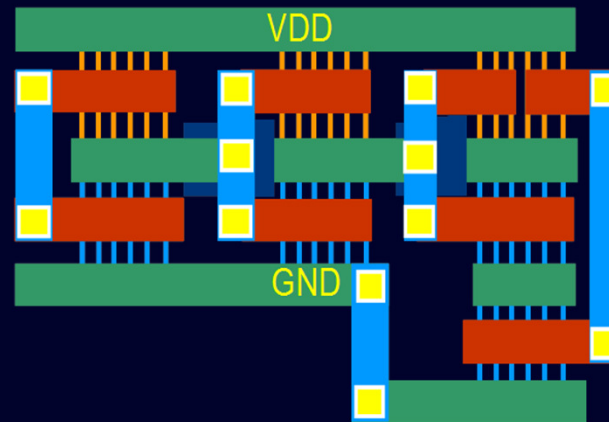
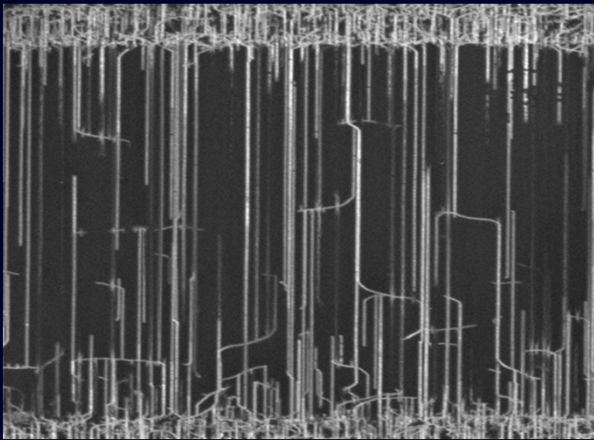
H. Dai, ibm.com, Nanoletters, Nature, Science, Stanford, Wikipedia

CNFET Technology Outlook

Problem	Challenge	Status
CNT alignment & positioning	Correct function	 → 
Metallic CNT	Correct function Low leakage	 → 
CNT density	High current density	
CNT doping	Complementary CNFETs	

Conclusion

- Imperfection-immune design essential
 - New solutions: practical, elegantly simple



- Next challenge: CNT variations
 - CNT correlation → unique layouts