

Finding the Missing Memristor

Stan Williams
HP Senior Fellow



People who did the work:

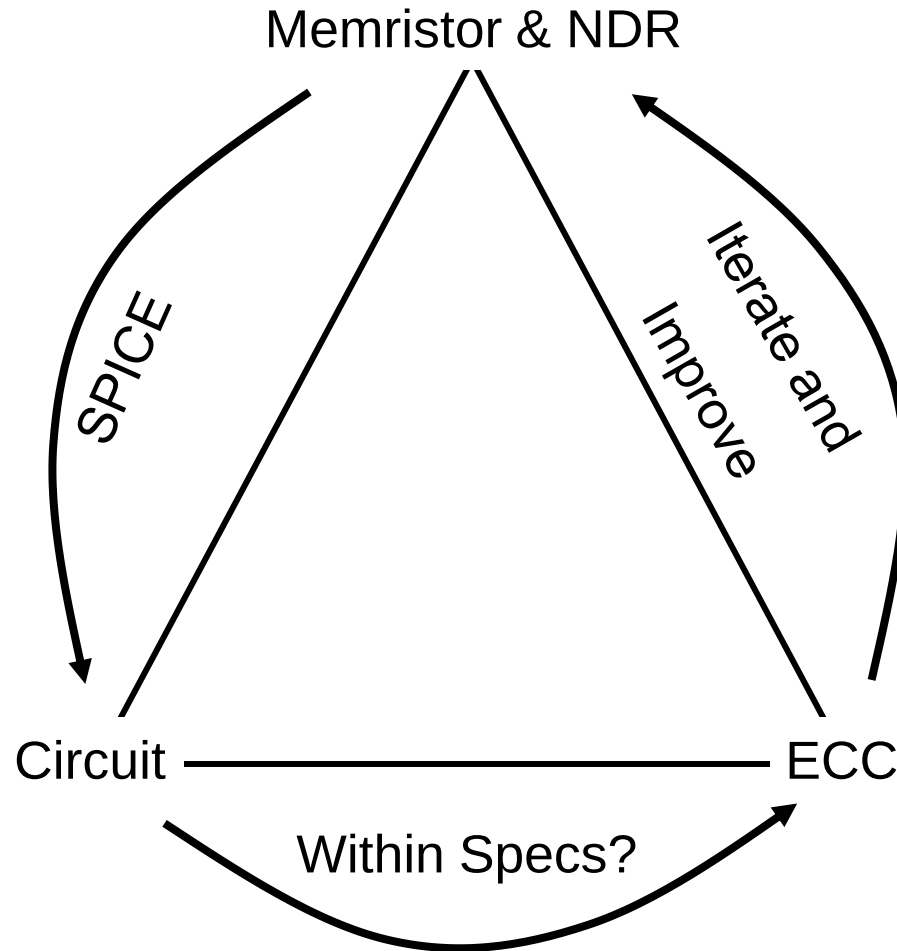
Over 60 current and former members of the IQS Lab and 40 members of other HP orgs –

esp. Greg Snider, Phil Kuekes,
Duncan Stewart, Dimitri Strukov,
Matthew Pickett, Julien Borghetti,
Jianhua Yang, John Paul Strachan,
Gilberto Ribeiro & many others!

Our partners at LBNL and NIST

Supported in part by DARPA

Device Physics and Mathematical Model



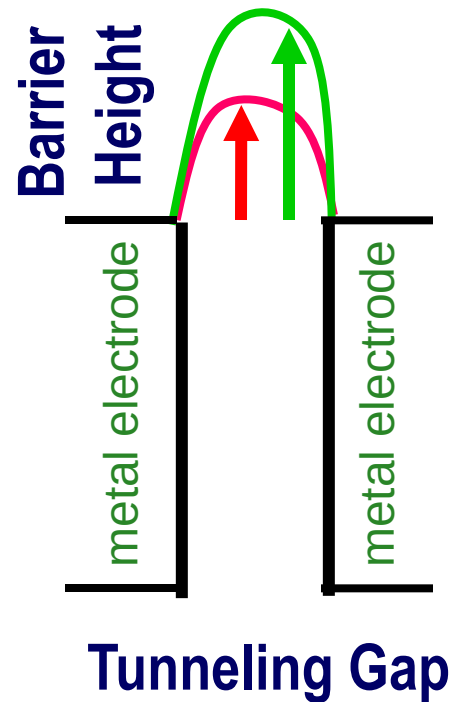
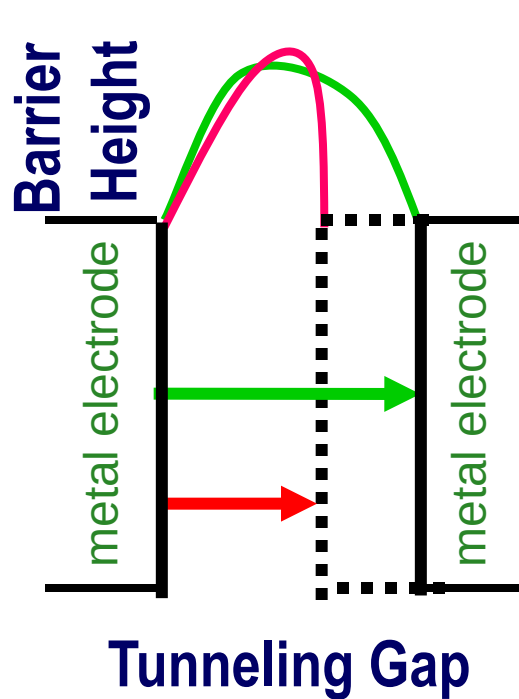
Architecture and Circuit Design

THE COMMERCIAL EFFORT



Janice Nickel with first 300 mm memristor wafer

Tunneling Probability Depends Exponentially on the Barrier Width and Height - Molecular isomerization leads to switching

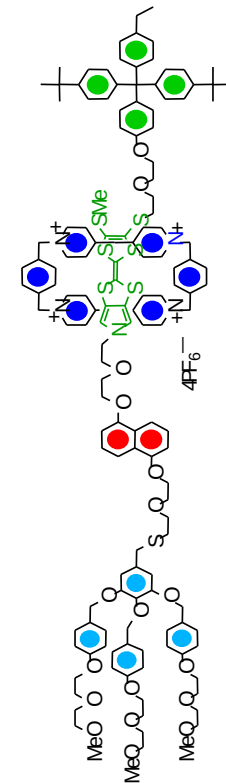
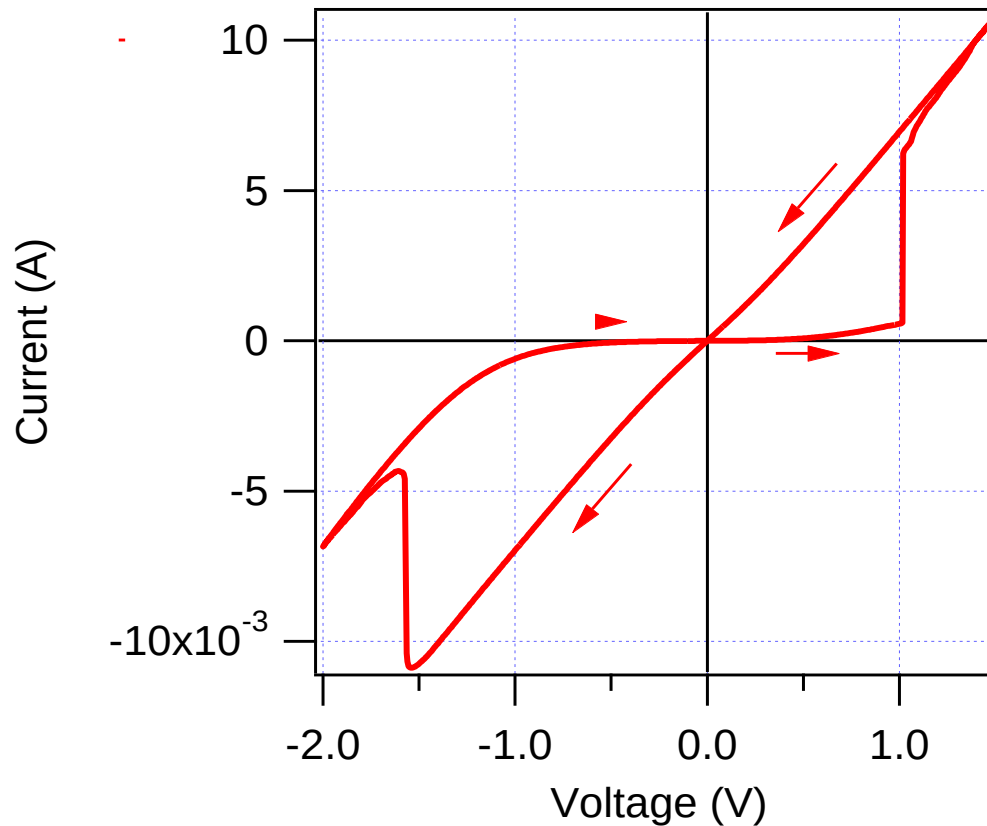


Slide from a talk given in 2002

Hysteretic switch: on/off states

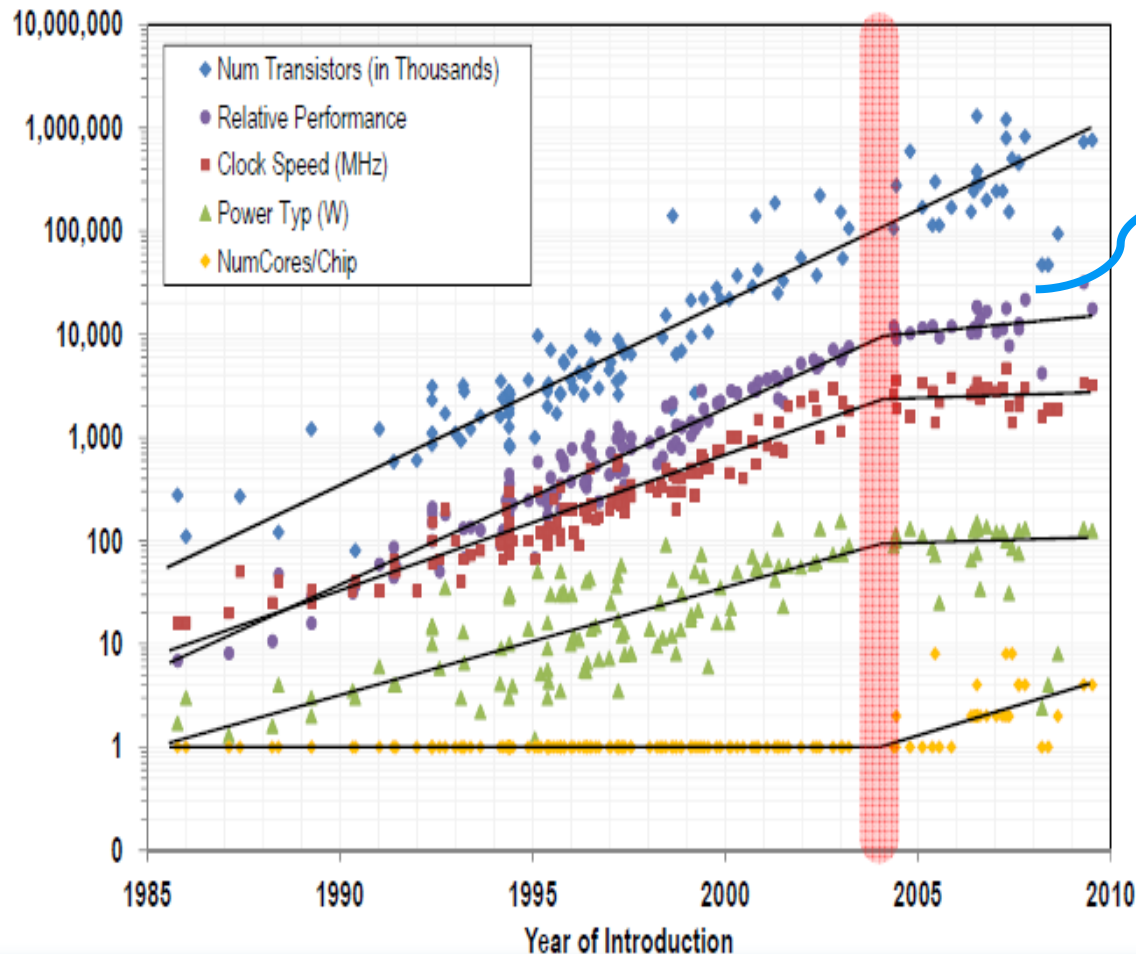
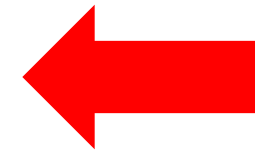


voltage-configured on/off switch



The “sharp right turn”

Single core performance
plateauing after
decades of exponential
growth !



Memristor History

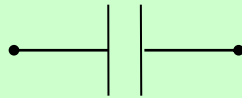


3 FUNDAMENTAL PASSIVE LINEAR CIRCUIT ELEMENTS

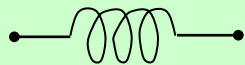
Resistor – 1827
Georg Ohm



RESISTOR
 $v = \mathcal{R} i$



CAPACITOR
 $q = C v$



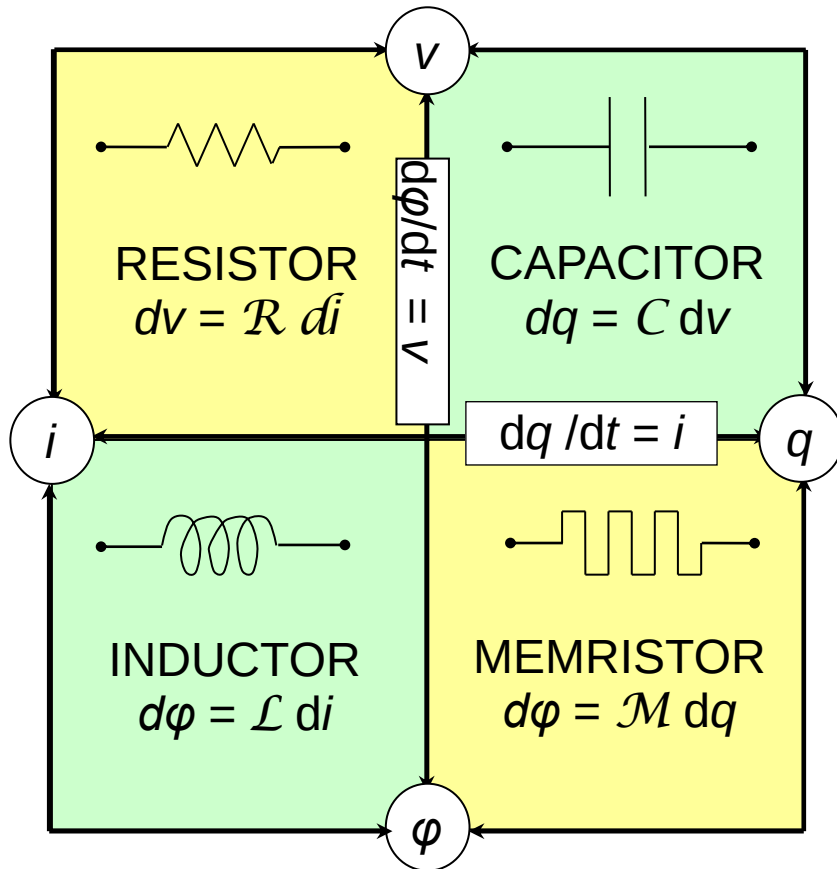
INDUCTOR
 $\varphi = \mathcal{L} i$



Capacitor - 1745
Volta / von Kleist & van Musschenbroek
Benjamin Franklin

Inductor – 1831
Michael Faraday
Joseph Henry

CHUA DEFINED THE MEMRISTOR IN 1971 BUT DID NOT KNOW A PHYSICAL EXAMPLE



“Memristor - the missing circuit element,”
IEEE Trans. Circuit Theory **18**, 507 (1971)

Formal mathematical proofs:

Not physics based

No causality implied by definition

Relation between ϕ and q an effect,
not the cause, of memristance!

$\mathcal{M}$ is a “memory resistor” –
it is a nonvolatile resistive memory!

Proved that no equivalent circuit to $\mathcal{M}$
could be made using any $\mathcal{R}$, $\mathcal{C}$ and $\mathcal{L}$ –
is a new and unique ‘basis function’

Built equivalent circuit using transistors

EXPANDED THE CONCEPT TO 'MEMRISTIVE SYSTEM' IN 1976

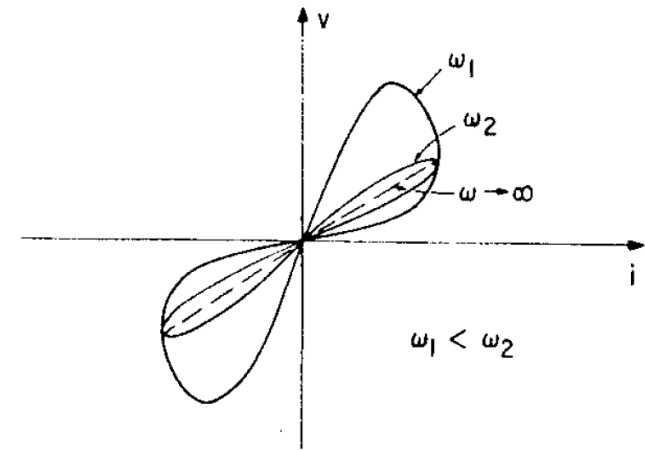
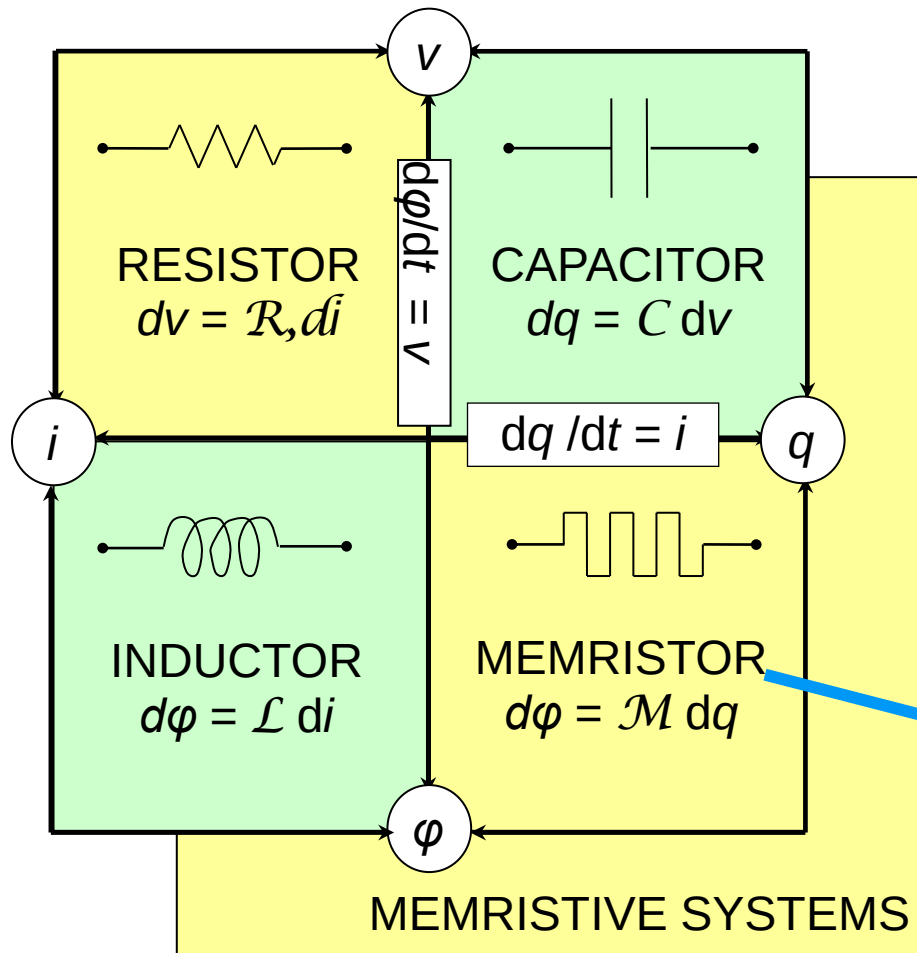


Fig. 6. Frequency response of Lissajous figures.

The pinched hysteresis loop

$$v = R(w)i$$

$$\frac{dw}{dt} = f(i)$$

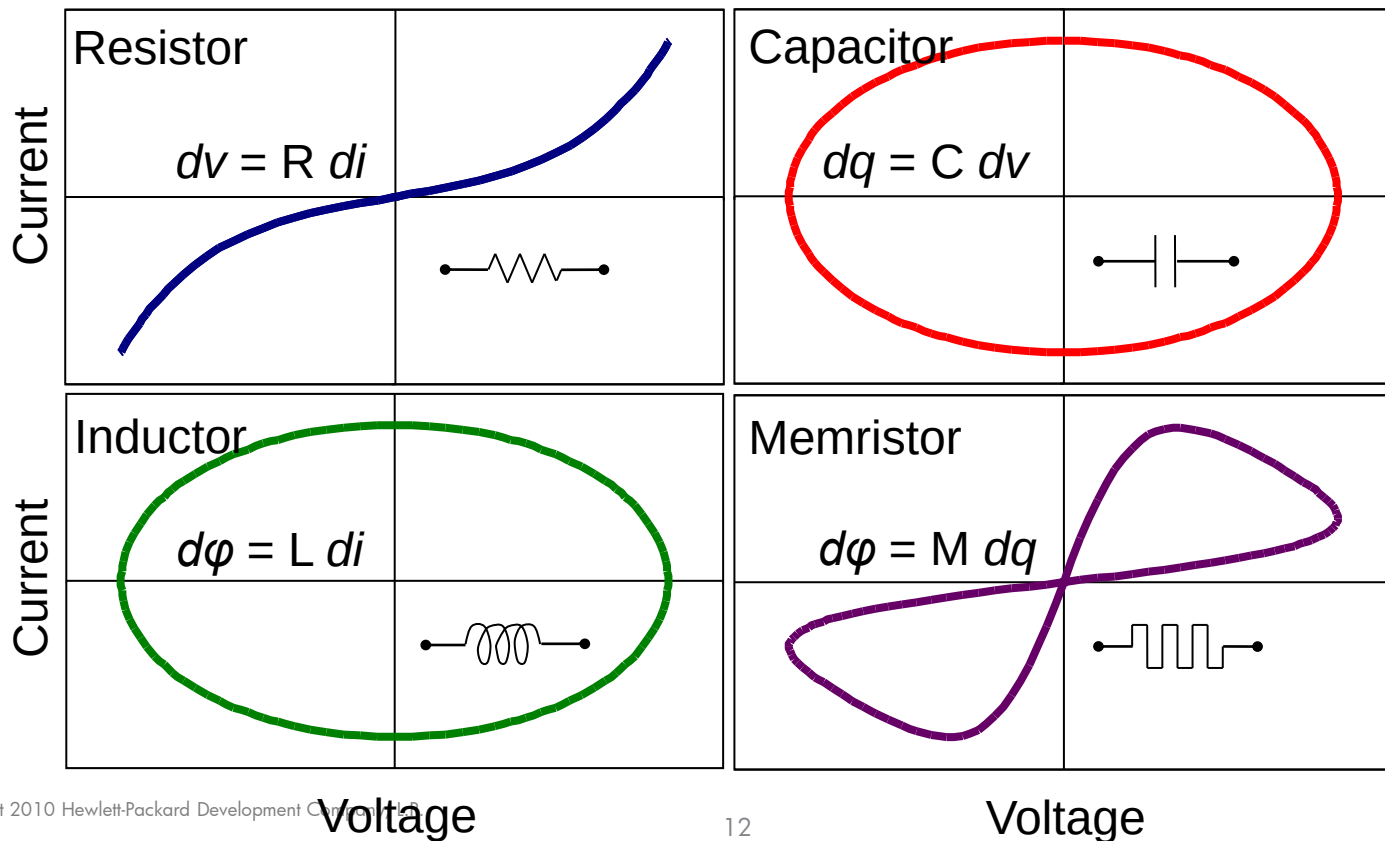
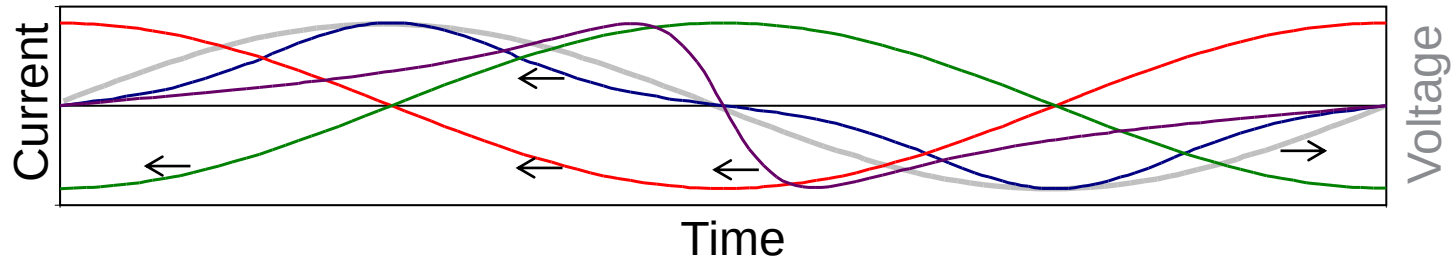
Rigorous mathematical definition

L. O. Chua, "Memristor - the missing circuit element," *IEEE Trans. Circuit Theory* 18, 507–519 (1971).

L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proc. IEEE*, 64 (2), 209-23 (1976).

What makes a memristor “fundamental”?

The inability to duplicate it's properties with the other passive circuit elements



RERAM IS A MEMRISTOR



Metal Oxide Resistive Switches: observation of pinched hysteresis

“Memory effects” in oxides
have been known for decades:

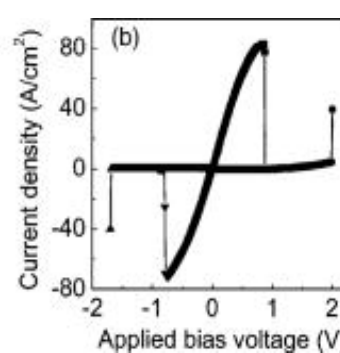
G. Dearnaley *et al.*, *Rev. Prog. Phys.* (1970)
a review with 150+ references

Just a few recent
references:

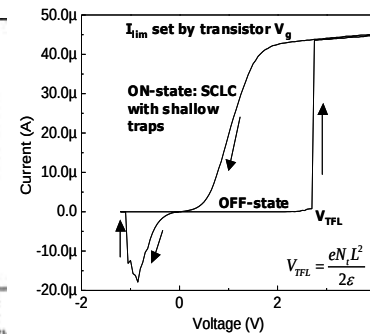
metal:

S. Seo <i>et al.</i> , <i>APL</i> (2003)	Ni
B. J. Choi <i>et al.</i> , <i>JAP</i> (2005)	Ti
H. Sim <i>et al.</i> , <i>Microel. Eng.</i> (2005)	Nb
D. Lee <i>et al.</i> , <i>EDL</i> (2005)	Zr
A. Chen <i>et al.</i> , <i>IEDM'05</i>	Cu
M. Kund <i>et al.</i> , <i>IEDM'05</i>	Ag
D. C. Kim <i>et al.</i> , <i>APL</i> (2006)	Nb
N. Banno <i>et al.</i> , <i>IEICE TE</i> (2006)	Cu(S)
T.-N. Fang <i>et al.</i> , <i>ICMTD'07</i>	Cu
L. Courtade <i>et al.</i> , <i>ICMTD'07</i>	Ni
W. Guan <i>et al.</i> , <i>APL</i> (2007)	Zr
S.-W. Kim & Y. Nishi, <i>NVMTS'07</i>	Cu(S)
D. Stewart, <i>NVMTS'07</i>	Ti
K.-C. Liu <i>et al.</i> , <i>NVMTS'07</i>	Hf
D. Lee <i>et al.</i> , <i>APL</i> (2007)	Mo

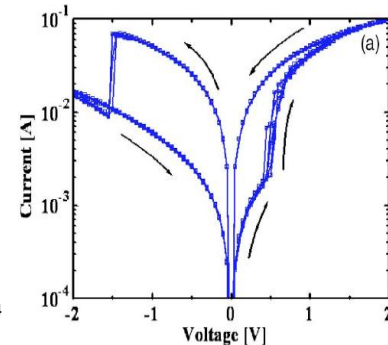
Just a few examples:



B. J. Choi *et al.* (2005)

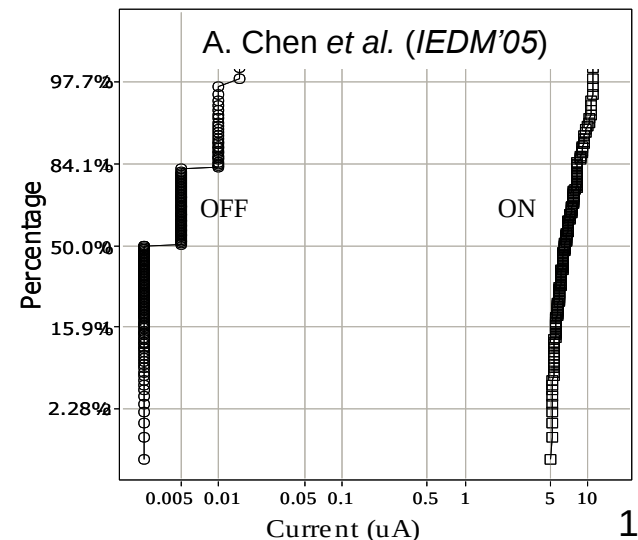
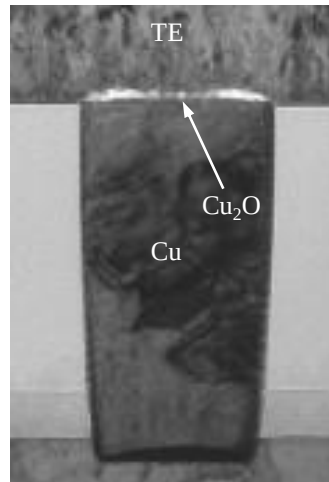


A. Chen *et al.* (2005)



D. Lee *et al.* (2007)

With time, data are becoming more reproducible:

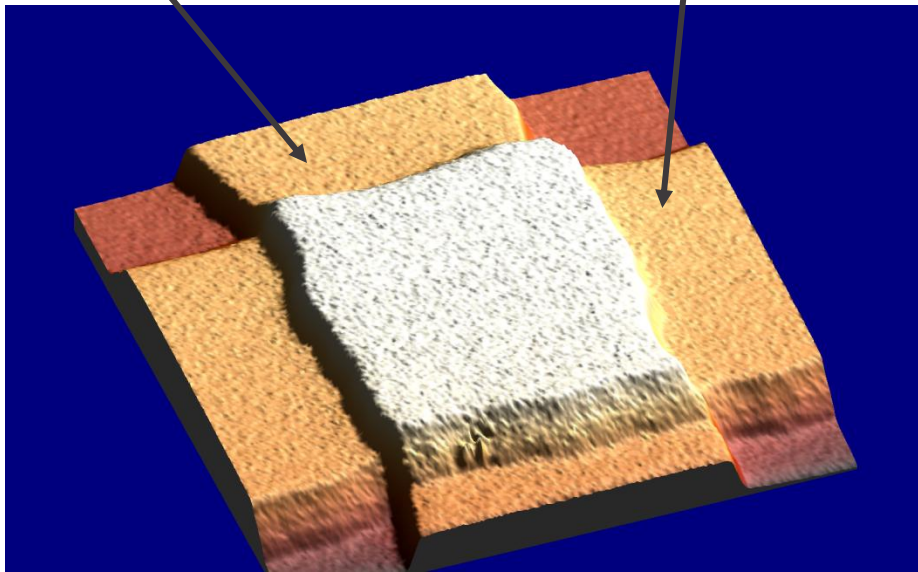


14

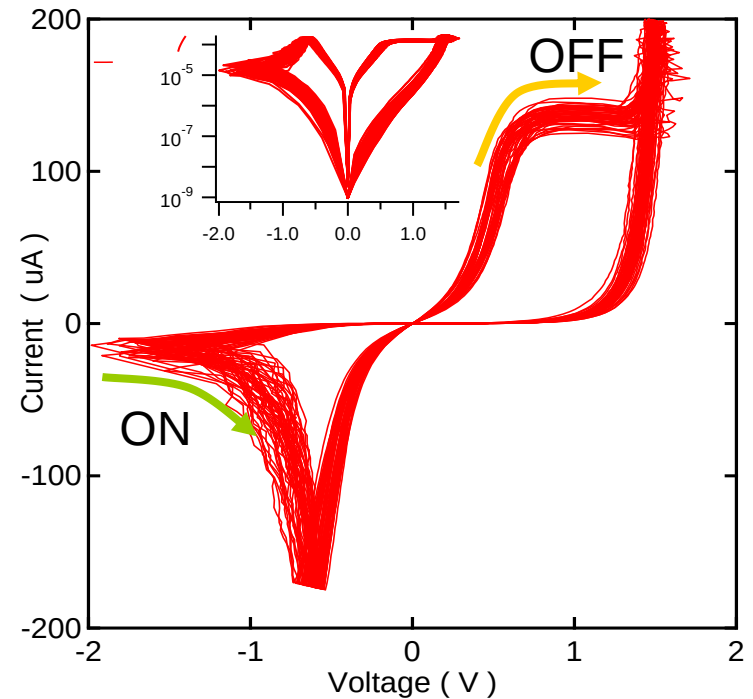
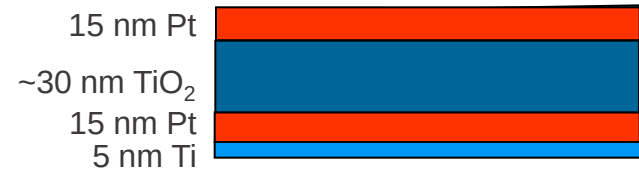
slide courtesy K. Likharev

OUR SWITCHING DEVICES: PT/TIO₂/PT

Top electrode Bottom electrode



- Dimensions: 30 nm – 16 μ m

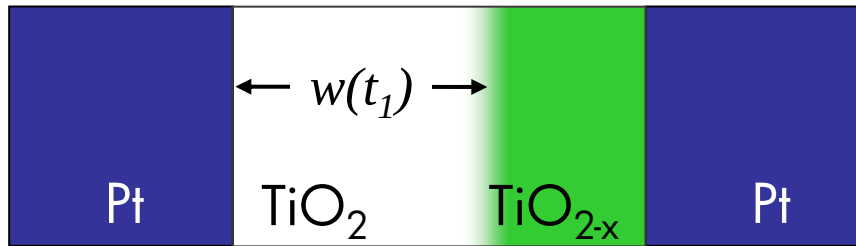


DRIFT, DIFFUSION AND THERMOPHORESIS



Vacancy Drift Model of Bipolar TiO₂ ReRAM

physical model has to be consistent with memristor equations!



$$v(t) = \left[R_{\text{OFF}} \frac{w(t)}{L} + R_{\text{ON}} \left(1 - \frac{w(t)}{L} \right) \right] i(t)$$

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{\text{ON}}}{L} i(t) \quad \text{Drift velocity}$$

$$w(t) = \mu_v \frac{R_{\text{ON}}}{L} q(t)$$

State variable w is the drift front

$$\mathcal{M}(q) = R_{\text{OFF}} \left(1 - \frac{\mu_v R_{\text{ON}}}{L^2} q(t) \right)$$

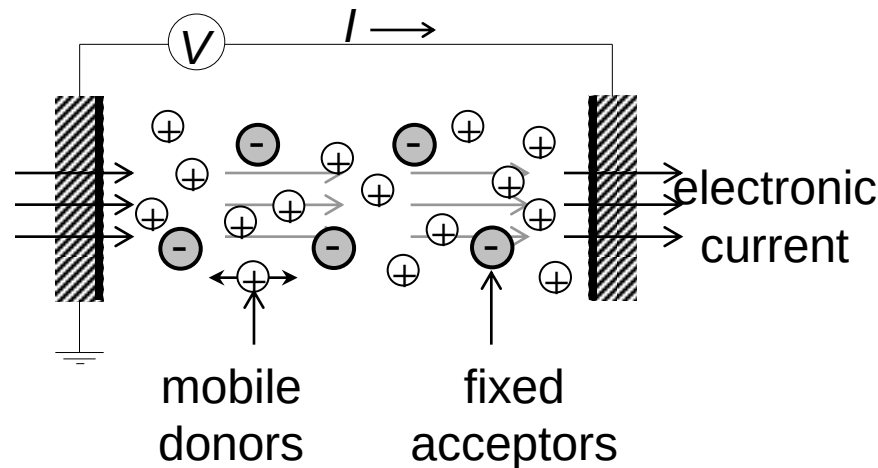
– Semiconducting TiO₂ Bipolar Switch

Previously: fixed semiconductor structure and only electronic motion.

Now: ionic motion dynamically modulates the semiconductor structure controlling the electronic current.

Coupled Ionic-Electronic Drift-Diffusion Model

Store information as the positions of atoms



Electrons: $\nabla \cdot (-en(x) \mu_n \nabla \phi_n(x)) = 0$

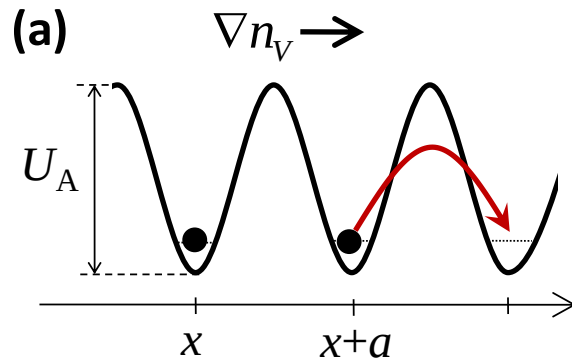
Holes: $\nabla \cdot (ep(x) \mu_p \nabla \phi_p(x)) = 0$

Ions: $-\nabla \cdot (-eD_i \nabla N_D(x) - eN_D(x) \mu_i E_0 \sinh[\nabla \phi(x)/E_0]) = e \frac{\partial N_D(x)}{\partial t}$

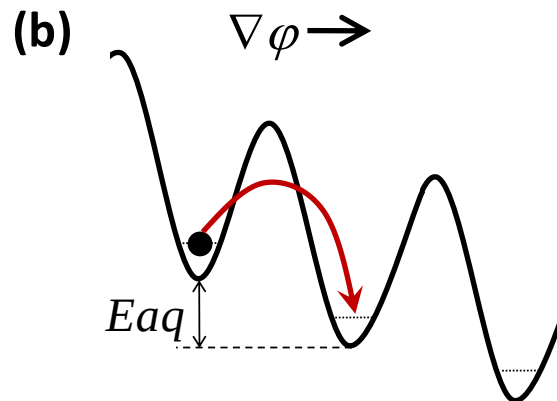
Poisson: $-\epsilon \epsilon_0 \Delta \phi(x) = e[p(x) - n(x) + f_D(x) N_D(x) - f_A(x) N_A]$

- Ohmic interfaces for electrons
- Blocking interfaces for ions
- Switch in a nanosecond, store for >10 years

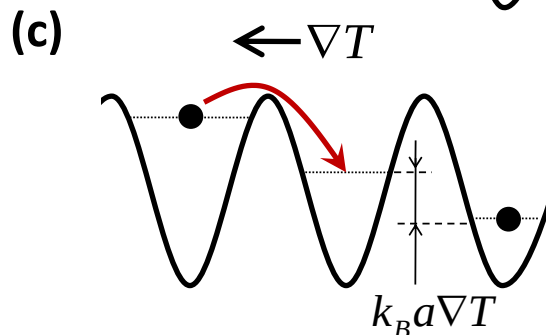
Factors affecting switching



Fick diffusion –
Concentration gradient
Limits state lifetime

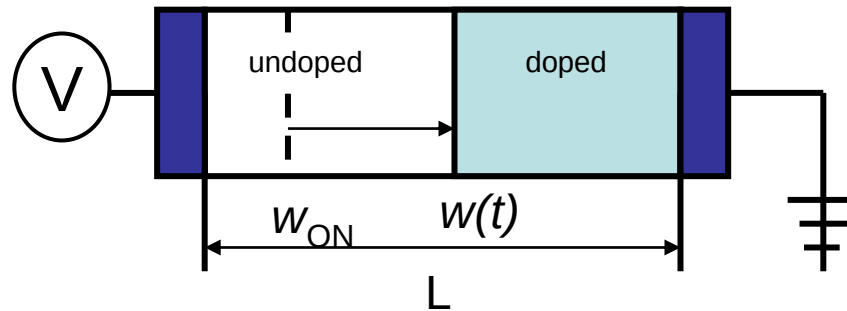


Drift –
Potential gradient
Bipolar switching speed

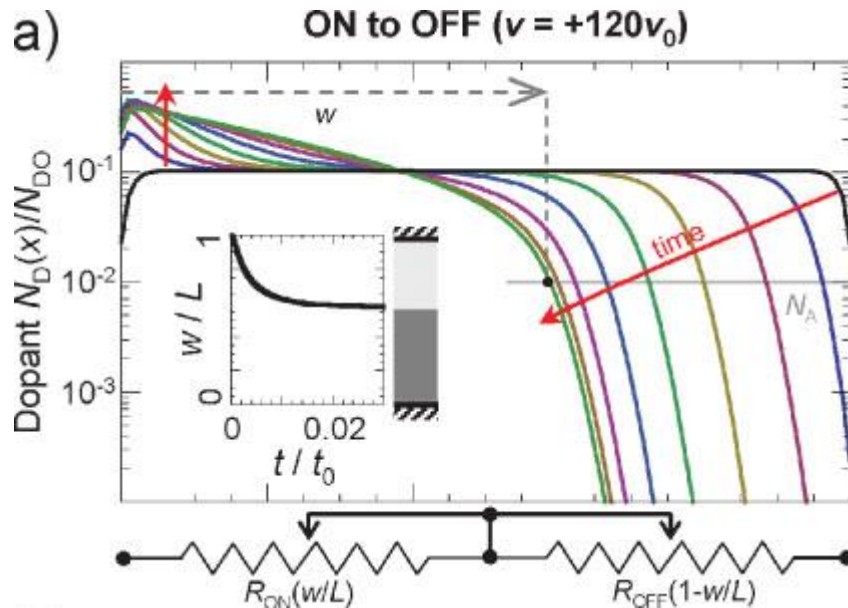


Thermophoresis –
Temperature gradient
Unipolar switching

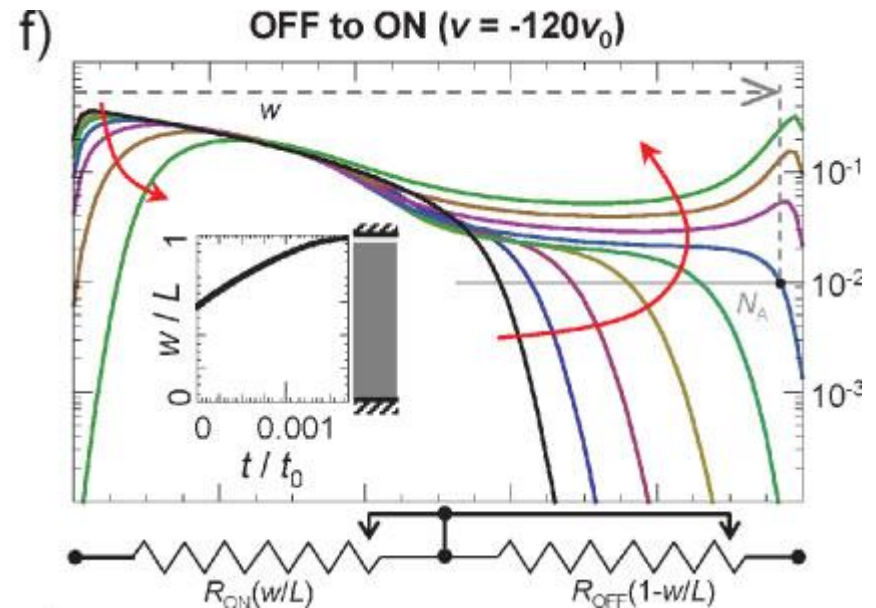
DRIFT – DIFFUSION MODEL OF BIPOLAR SWITCHING



Off switching:



Slow – diffusion opposes drift



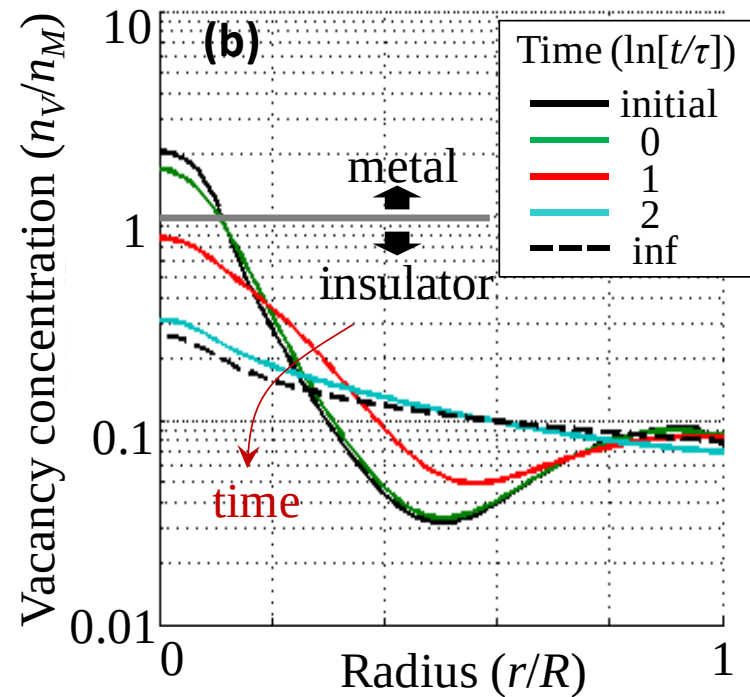
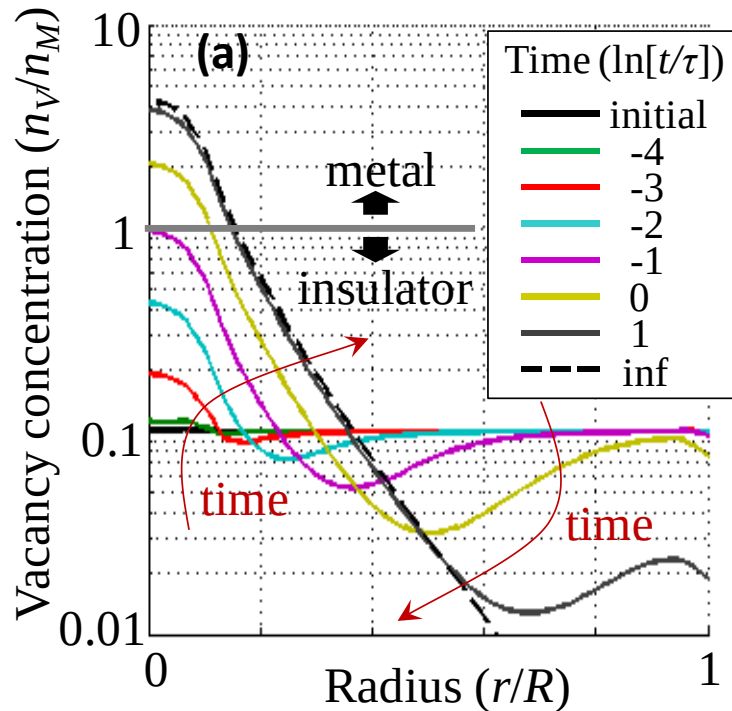
Fast – diffusion aids drift

D. Strukov *et. al*, Small 2009, 5, No. 9, 1058–1063

Thermophoresis-induced radial switching

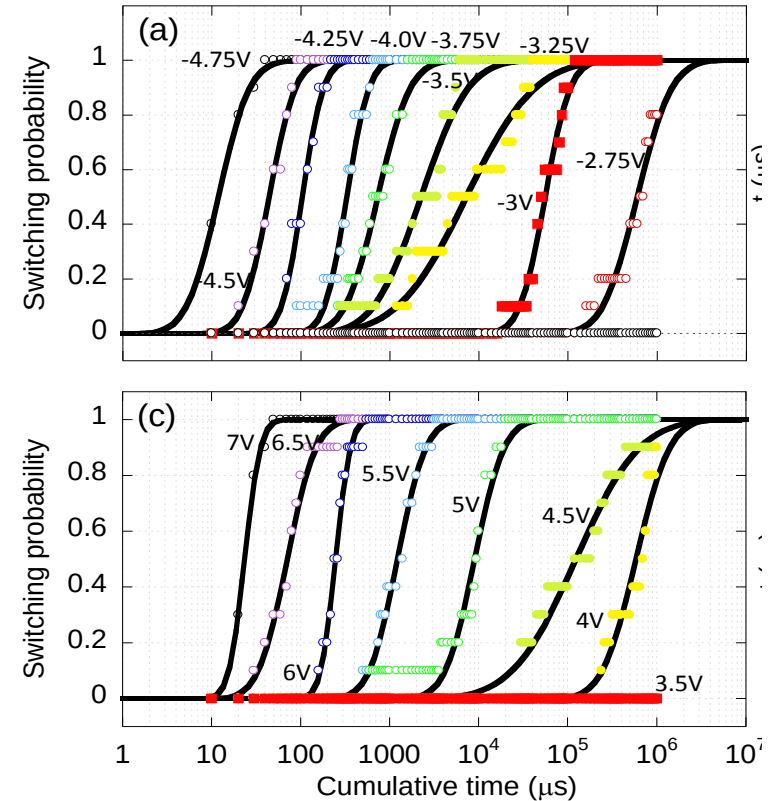
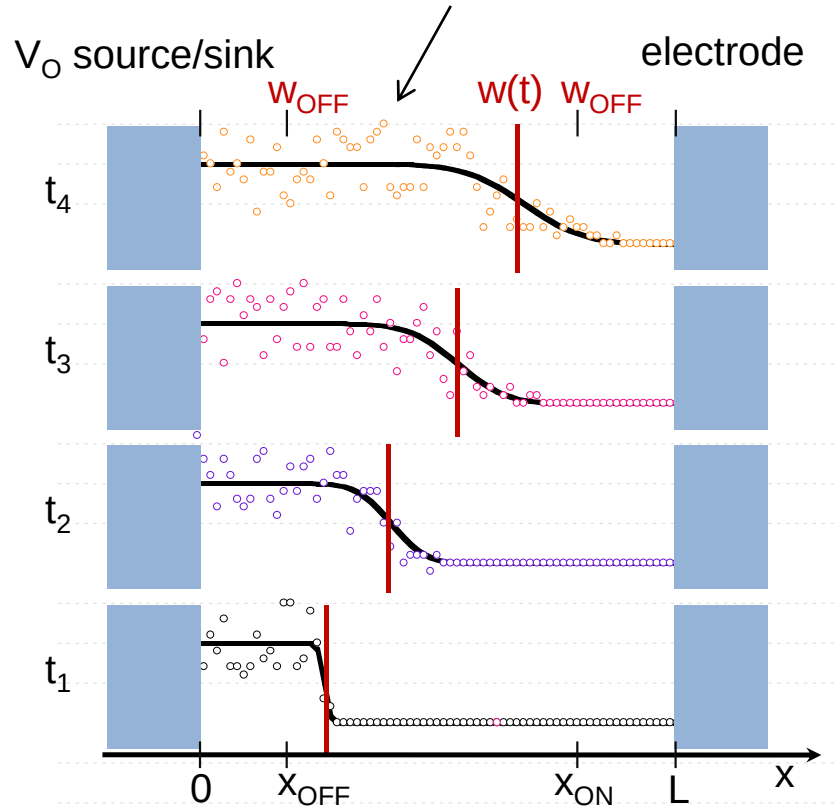
Vacancies 'breathe' in and out of a conducting channel

The origin of 'unipolar' switching



Analytical solution to drift-diffusion equation (solid lines)

$$N(x, t) = N_s \left(1 - \int_{-\infty}^x \frac{1}{(4\pi Dt)^{1/2}} \exp \left[-\frac{(x - \gamma t)^2}{4Dt} \right] dx \right) = N_s \left(1 - \frac{1}{2} \operatorname{erfc} \left[-\frac{(x - \gamma t)}{2\sqrt{Dt}} \right] \right)$$



$$P_{OFF}(t; V, \Delta w) = \frac{1}{2} \operatorname{erfc} \left[\frac{(\Delta w - k_v - b_v \ln[t])}{\sqrt{2\sigma_w^2 + 4Dt}} \right]$$

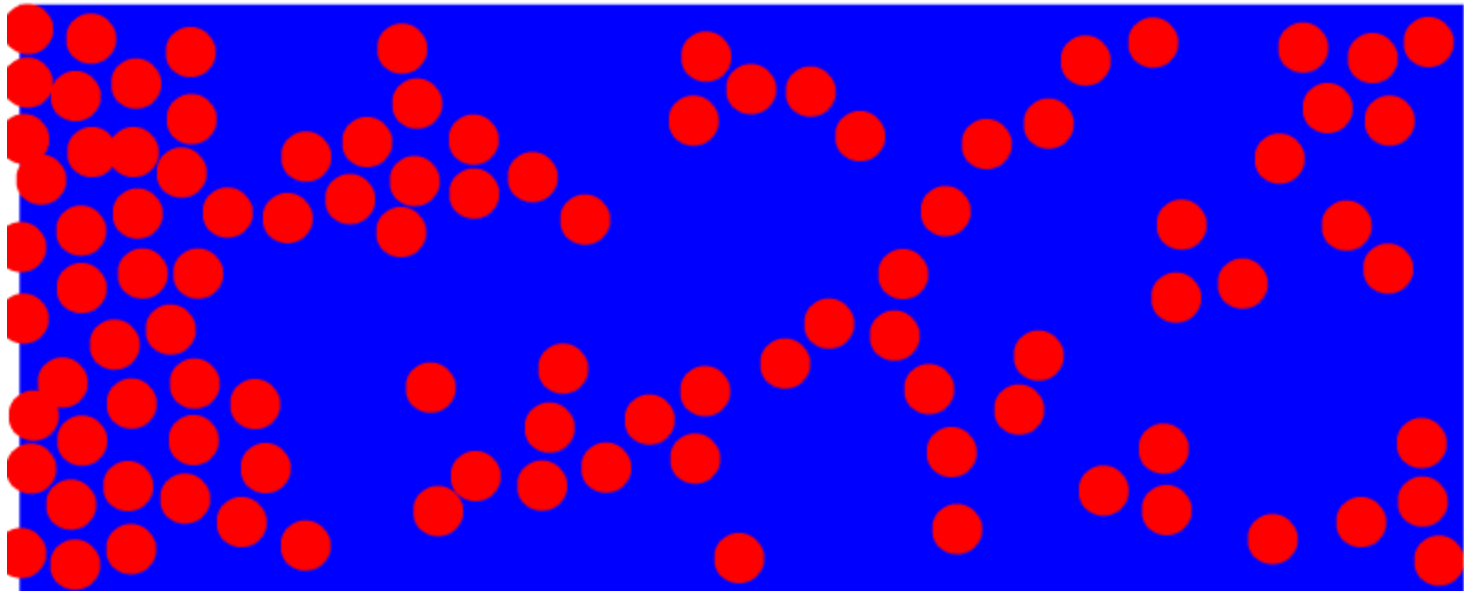
MOLECULAR DYNAMICS SIMULATION

Simple 2D model of O vacancies in TiO_2

Red Dots – O vacancies

Blue Background – TiO_2

Vacancy attractions cause 'filaments'



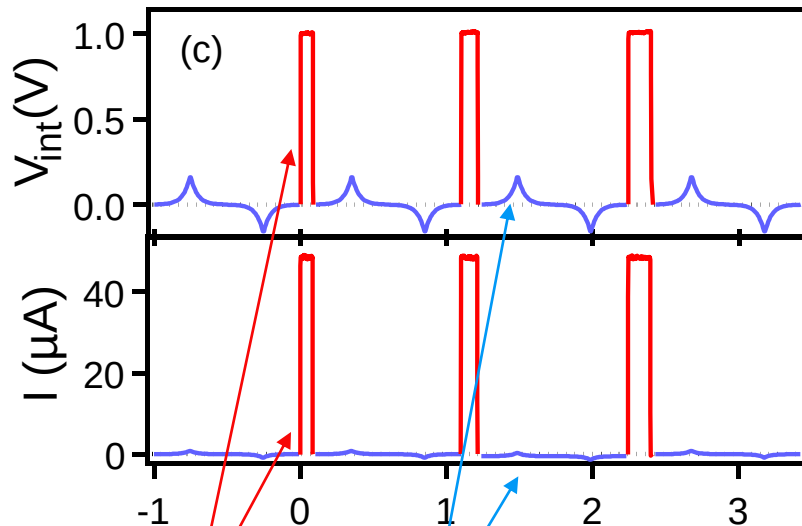
How to Measure and Model a Memristor



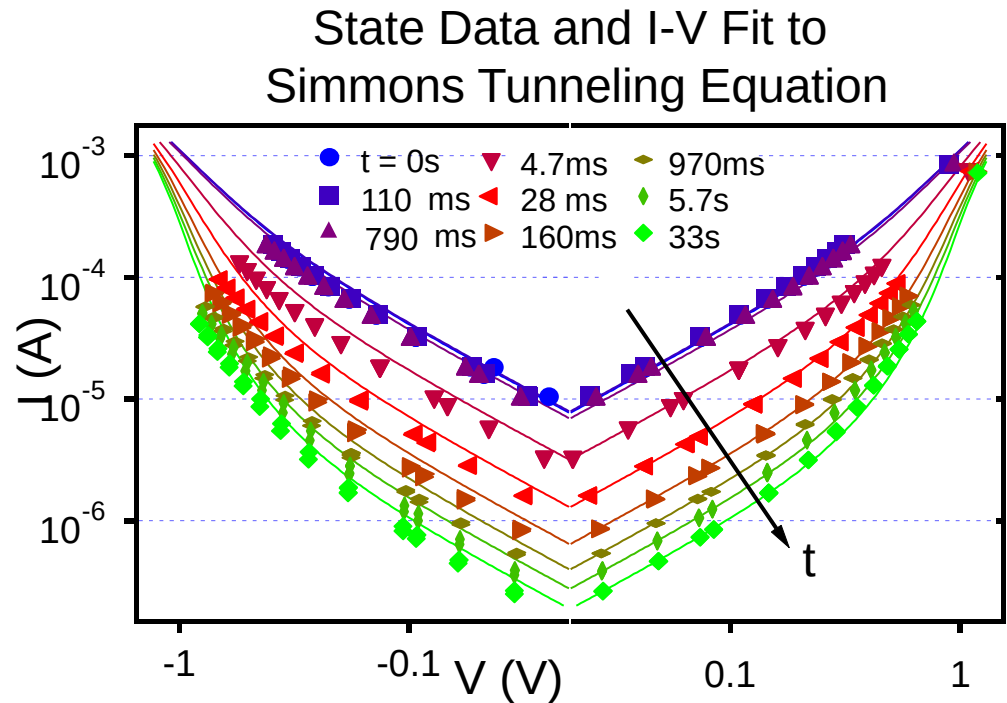
State-Test Protocol: must keep time stamp

Memristors are dynamical devices!

Example time series



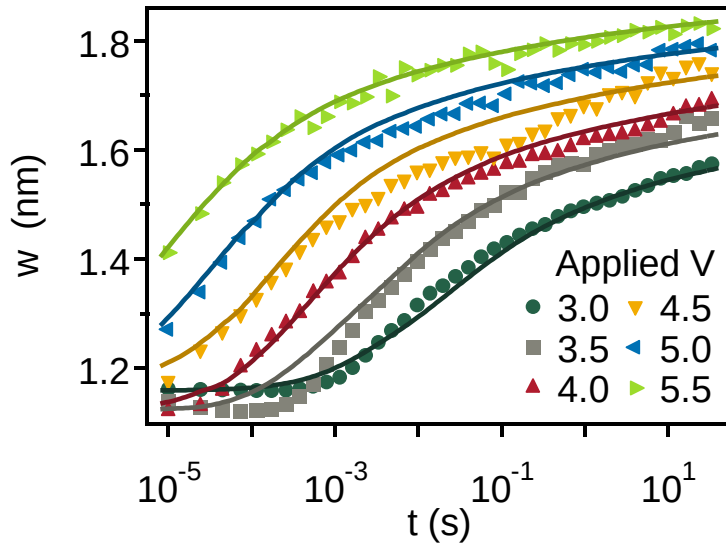
State Evolution State Test



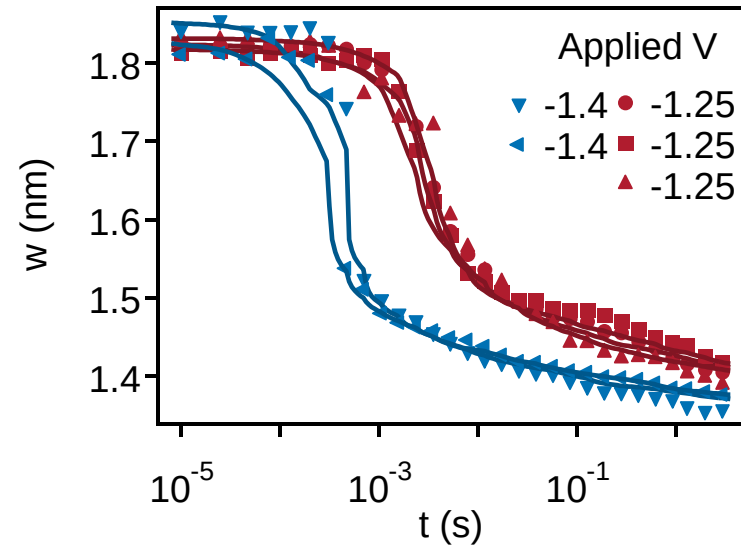
- Time series of I-V tests taken during the 4.5V OFF-switching state test
- Lines on state data are best fits to a series resistor R_s plus Simmons tunnel barrier
- Conduction model extrapolates well to high positive voltage

STATE VARIABLE TIME EVOLUTION

OFF switching:



ON switching:

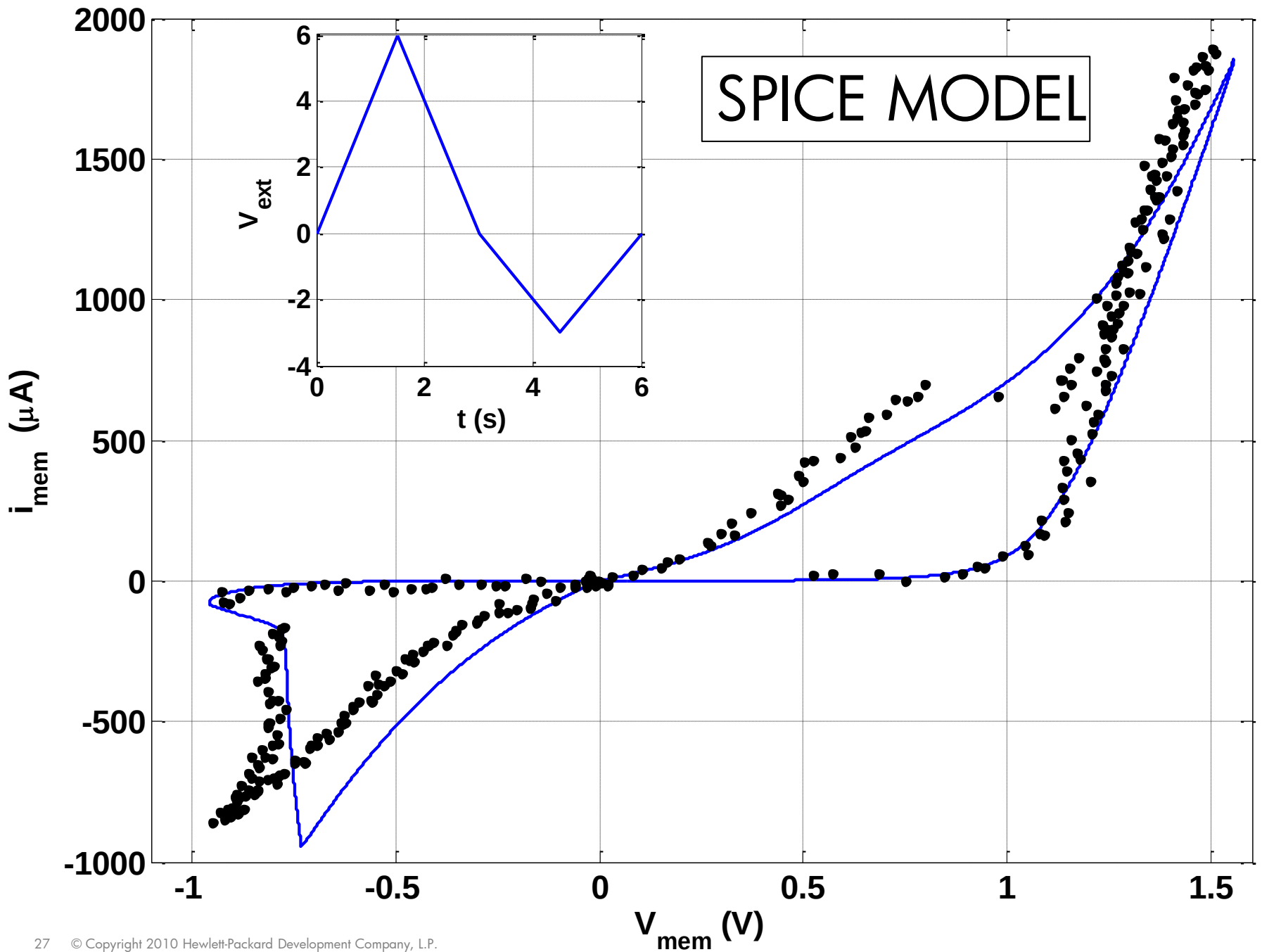


$$\dot{w} = f_{OFF} \sinh\left(\frac{i}{i_{OFF}}\right) \exp\left(-\exp\left(\frac{w - a_{OFF}}{w_c} - \frac{\text{abs}(i)}{b}\right) - \frac{w}{w_c}\right)$$

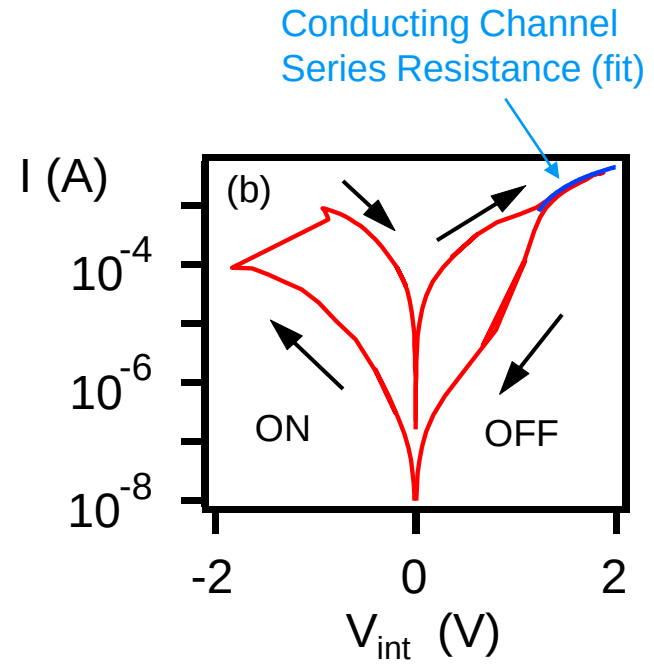
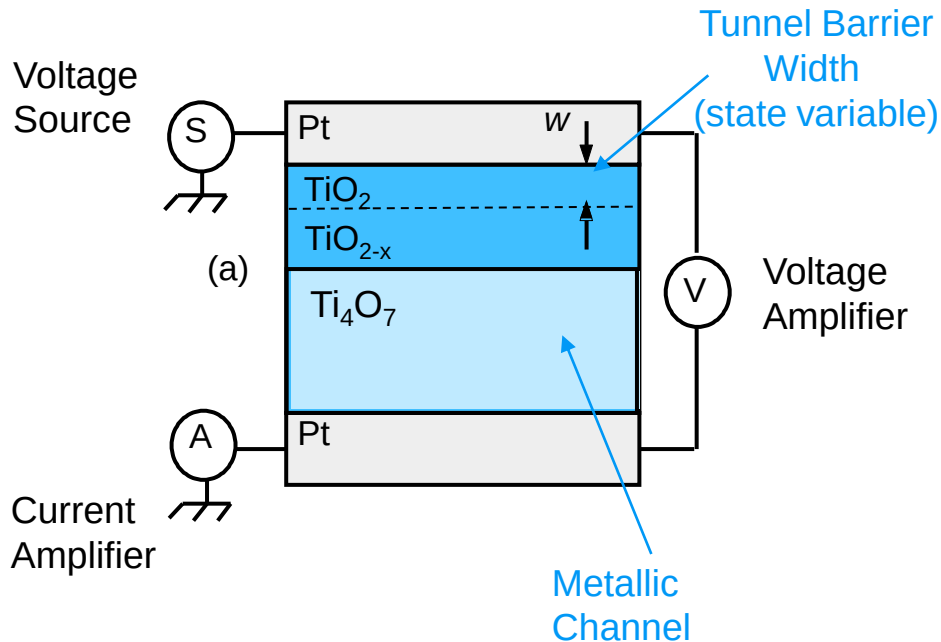
$$\dot{w} = f_{ON} \sinh\left(\frac{i}{i_{ON}}\right) \exp\left(-\exp\left(\frac{w - a_{ON}}{w_c} - \frac{\text{abs}(i)}{b}\right) - \frac{w}{w_c}\right)$$

Analytical approximations (lines) accurately represent device dynamical behavior (data points).

Extremely non-linear dynamics come from exponential I-V and drift



STRUCTURAL MODEL



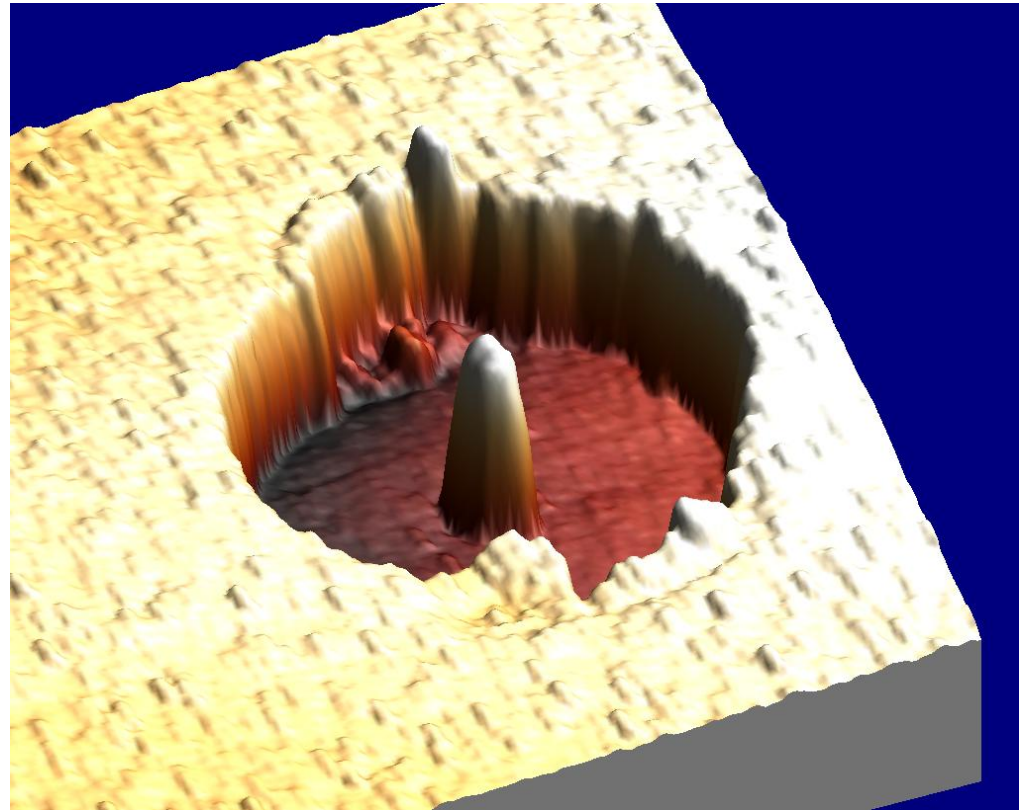
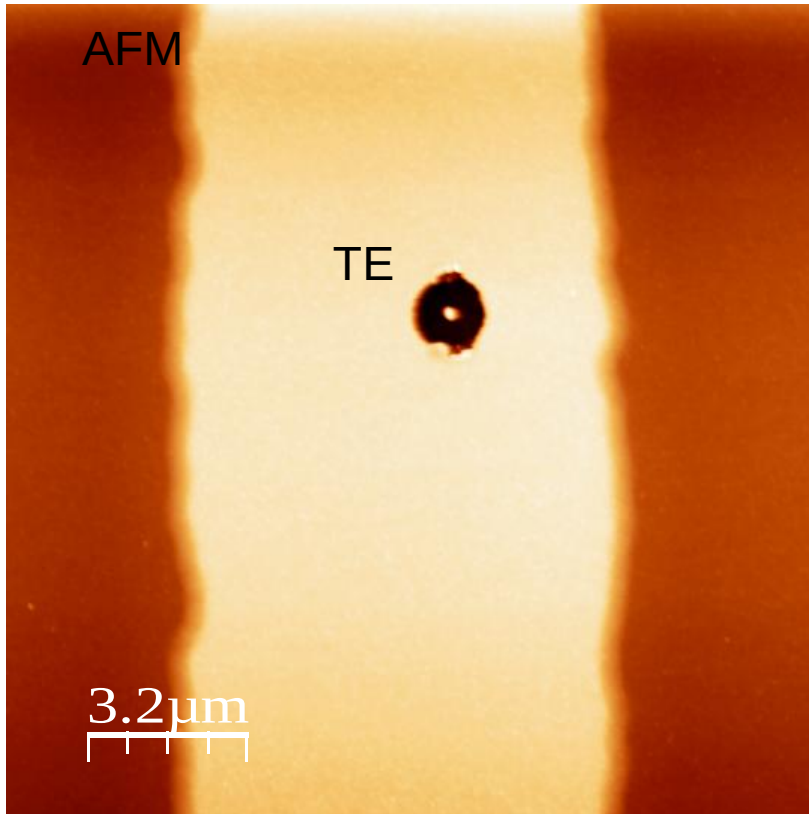
- Four Point measurement device schematic including
 - Metallic channel
 - tunnel barrier

- Typical device in study
 - negative polarity turns device ON
 - positive polarity turns device OFF

Materials Characterization



AFM Direct Observation of the Conducting Channel

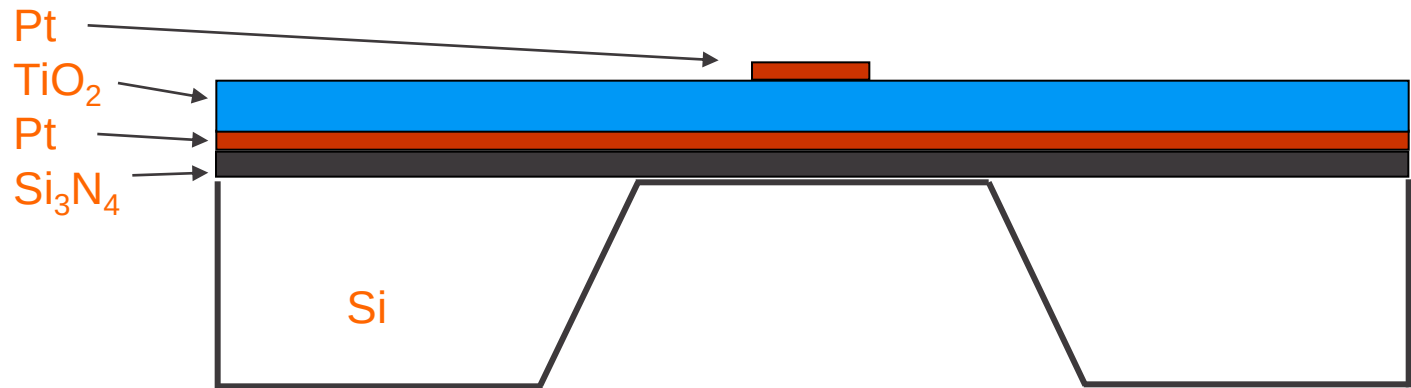


After forming a device, we can peel off the top electrode. With AFM, we see the conducting channel postulated from the electrical measurements. Can we determine the composition?

SCANNING TRANSMISSION X-RAY MICROSCOPY (STXM)

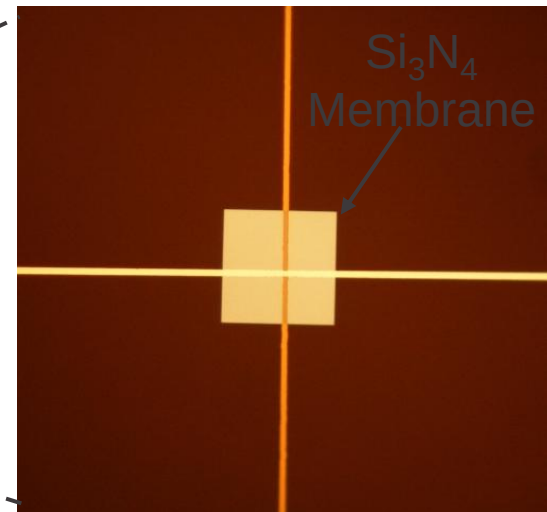
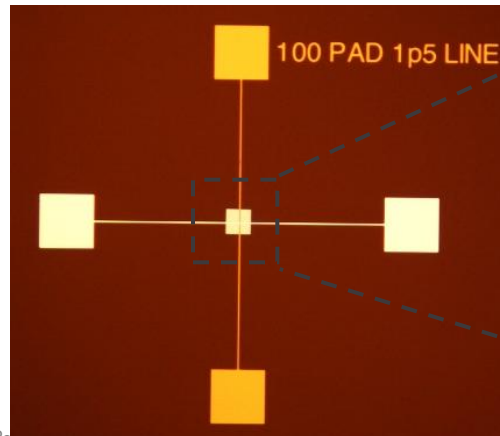
Devices need to be on membranes for transmission experiment

Side view

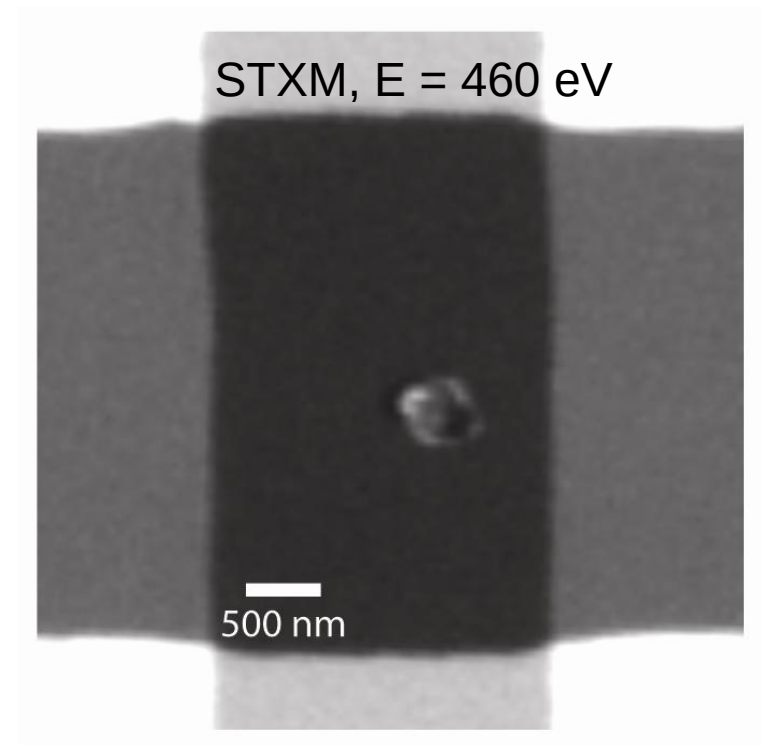
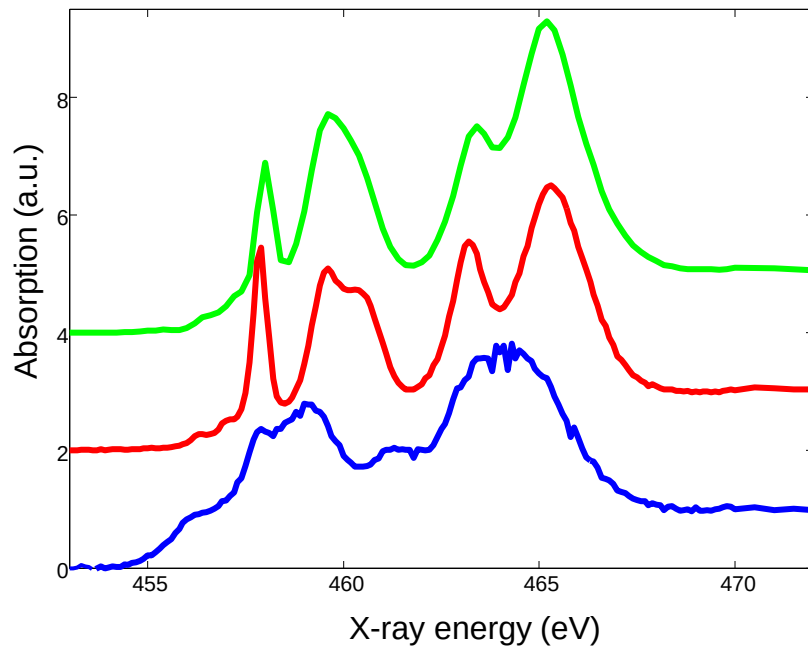
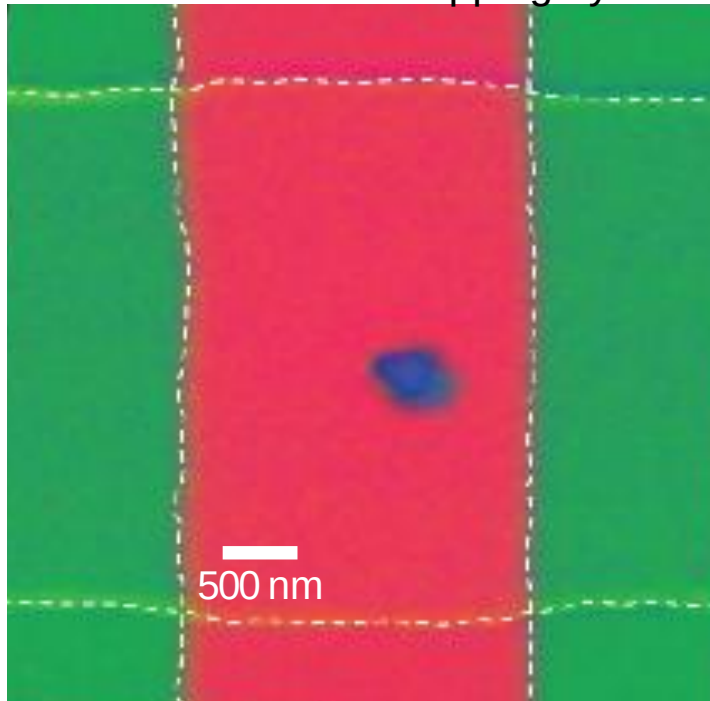


Top view

1.5 μ m x 1.5 μ m junction



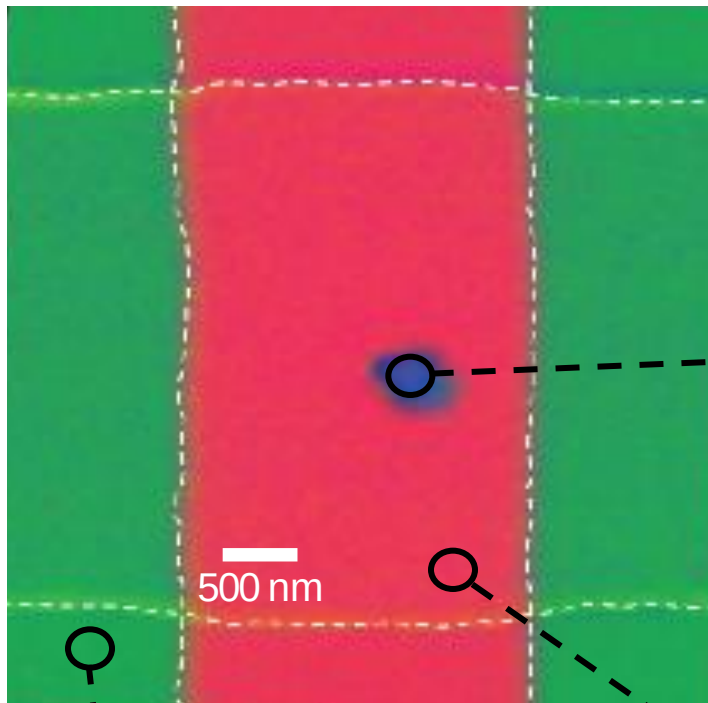
Chemical/Structural Mapping by XAS



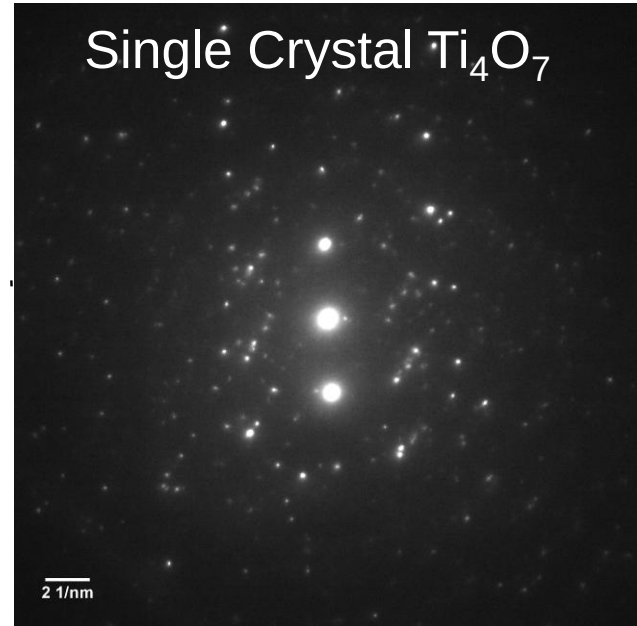
- TiO₂ Amorphous
- TiO₂ Anatase, heated > 330° C
- TiO_{2-x} Reduced

JP Strachan, MD Pickett, JJ Yang, S Aloni, ALD Kilcoyne, G Ribeiro, RS Williams, *Advanced Materials* 22, 3573 (2010)

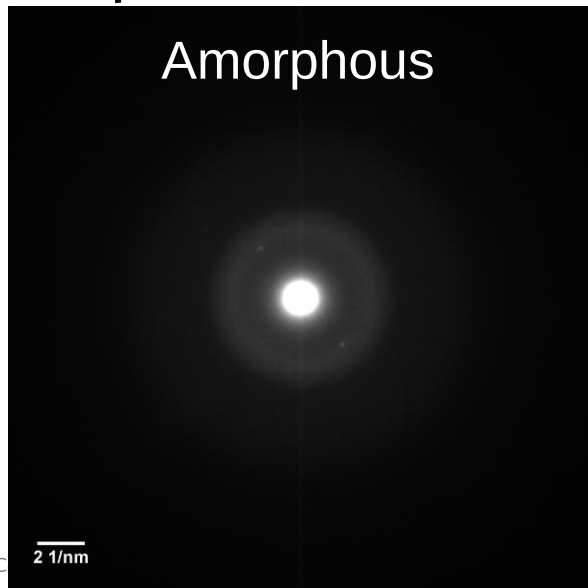
TEM - Electron diffraction



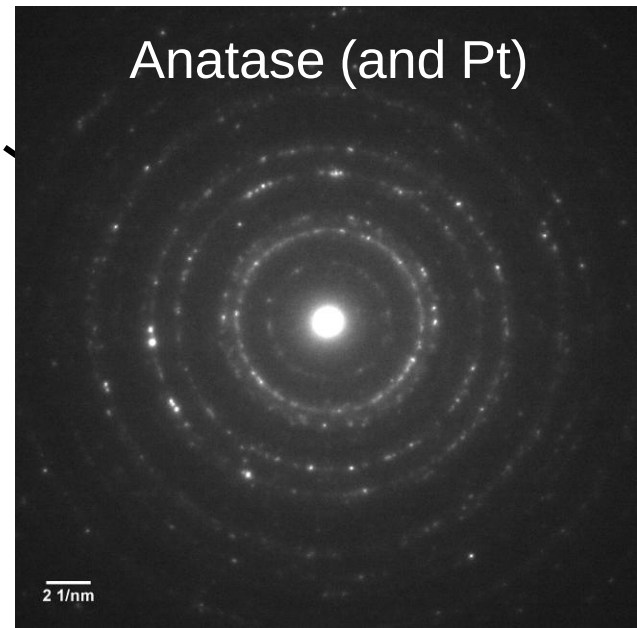
Single Crystal Ti_4O_7



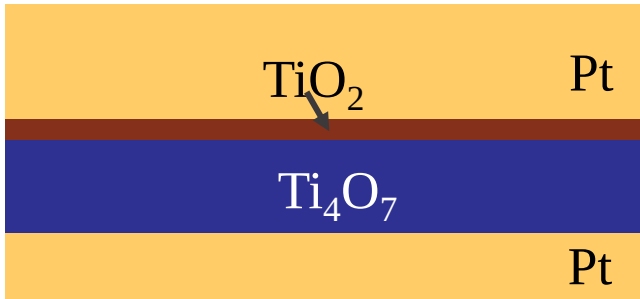
Amorphous



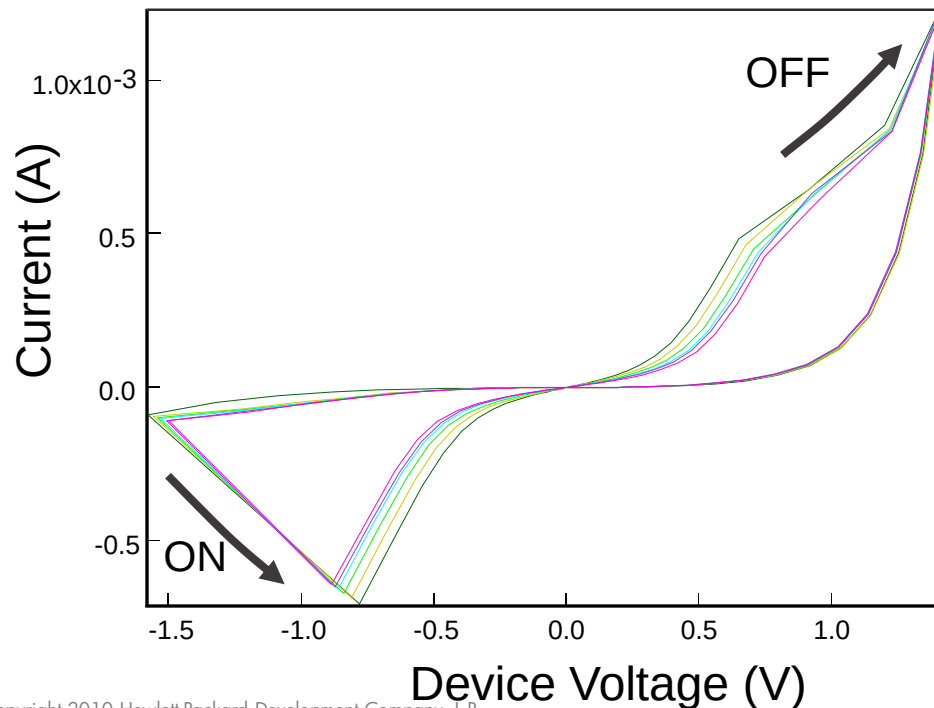
Anatase (and Pt)



ELIMINATE ELECTROFORMING!



Pt / 35nm " Ti_4O_7 " / 5nm TiO_2 / Pt



No electroforming step
OFF state = virgin state

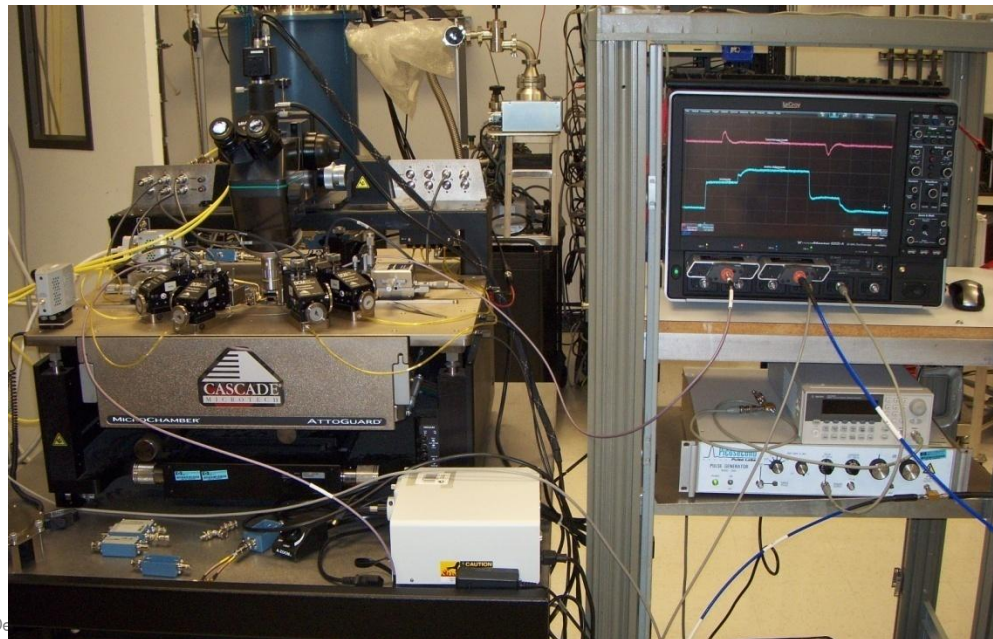
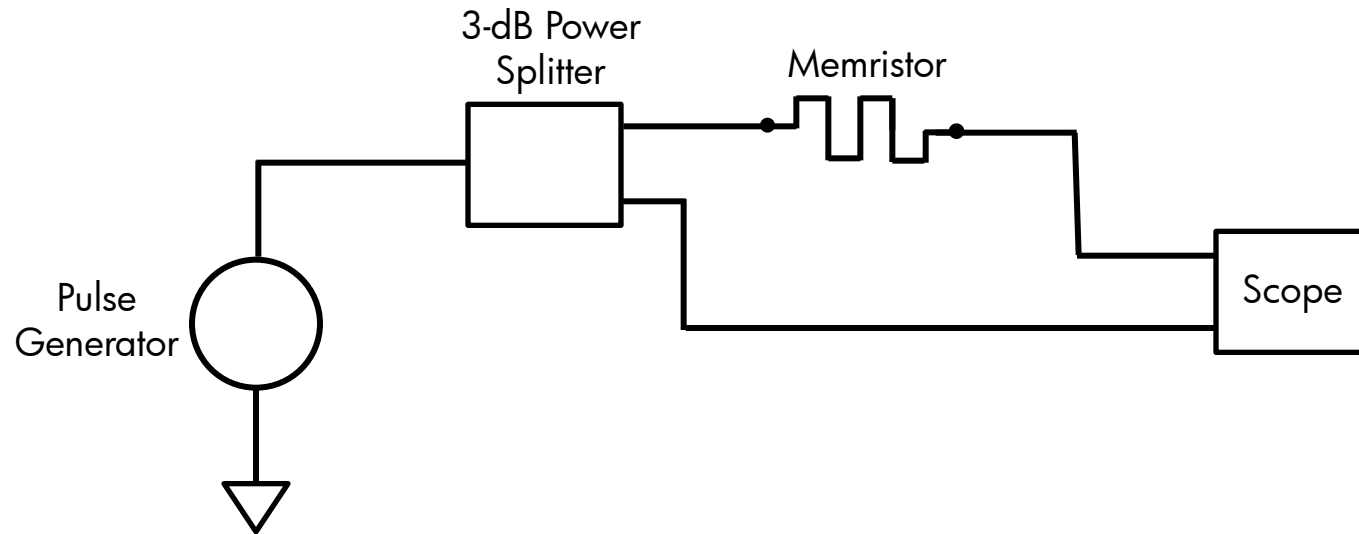
Switching Speed, Energy and Endurance



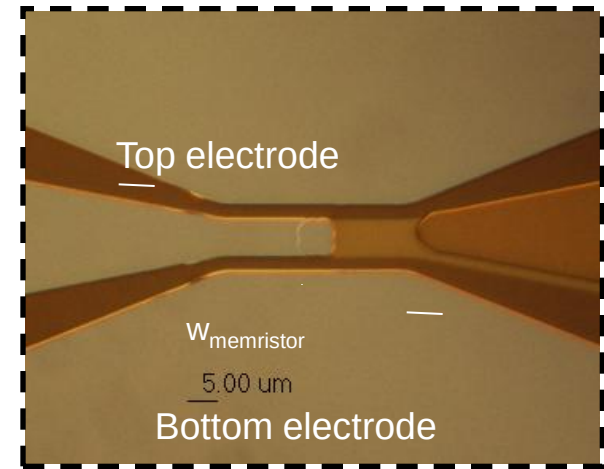
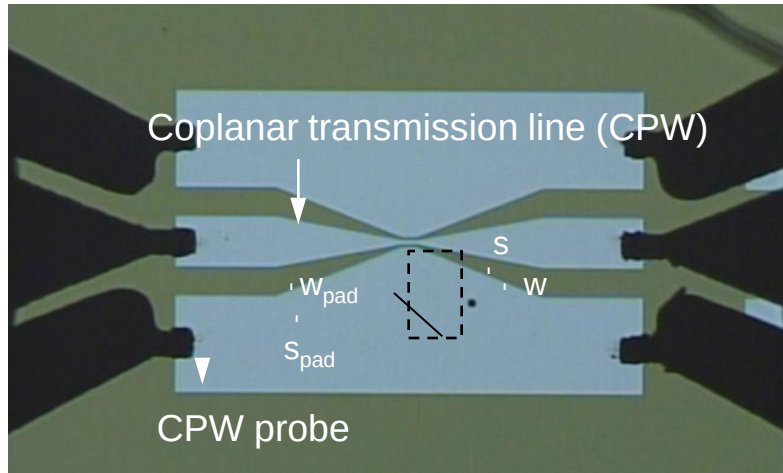
THE QUESTIONS PEOPLE ASK

- Switching voltages/currents (volts/nA - μ A)
- Write/Erase/Read speed and energy (<1 ns, ~ 1 pJ)
- ON/OFF ratio ($>1000:1$)
- Retention time ($>$ years)
- Endurance >10 billion and counting
- Scaling limits (10 nm pitch? ~ 1 terabit/sq cm/layer)
- Endurance and failure mechanisms (heating, electromigration)
- Nature of ON and OFF states (metal/insulator)
- Electroforming (can eliminate)
- Devices are evolving rapidly with understanding

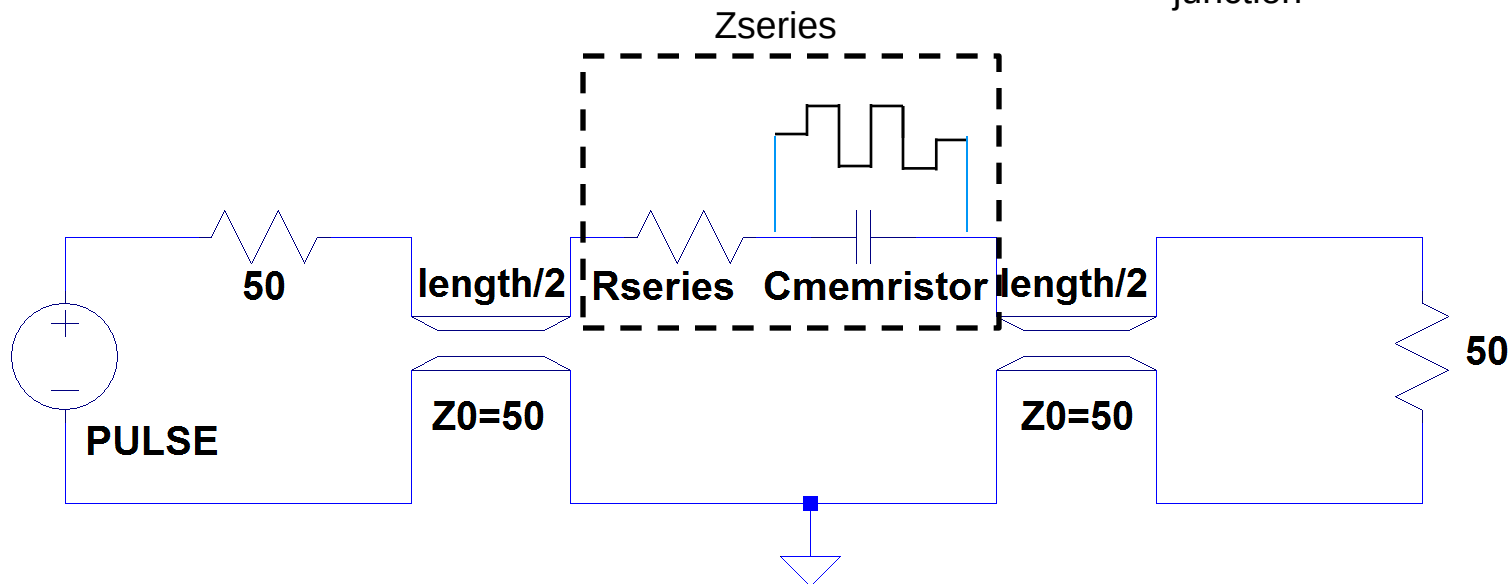
High-speed setup for memristor characterization



Microwave transmission line measurements: high speed switching time and energy

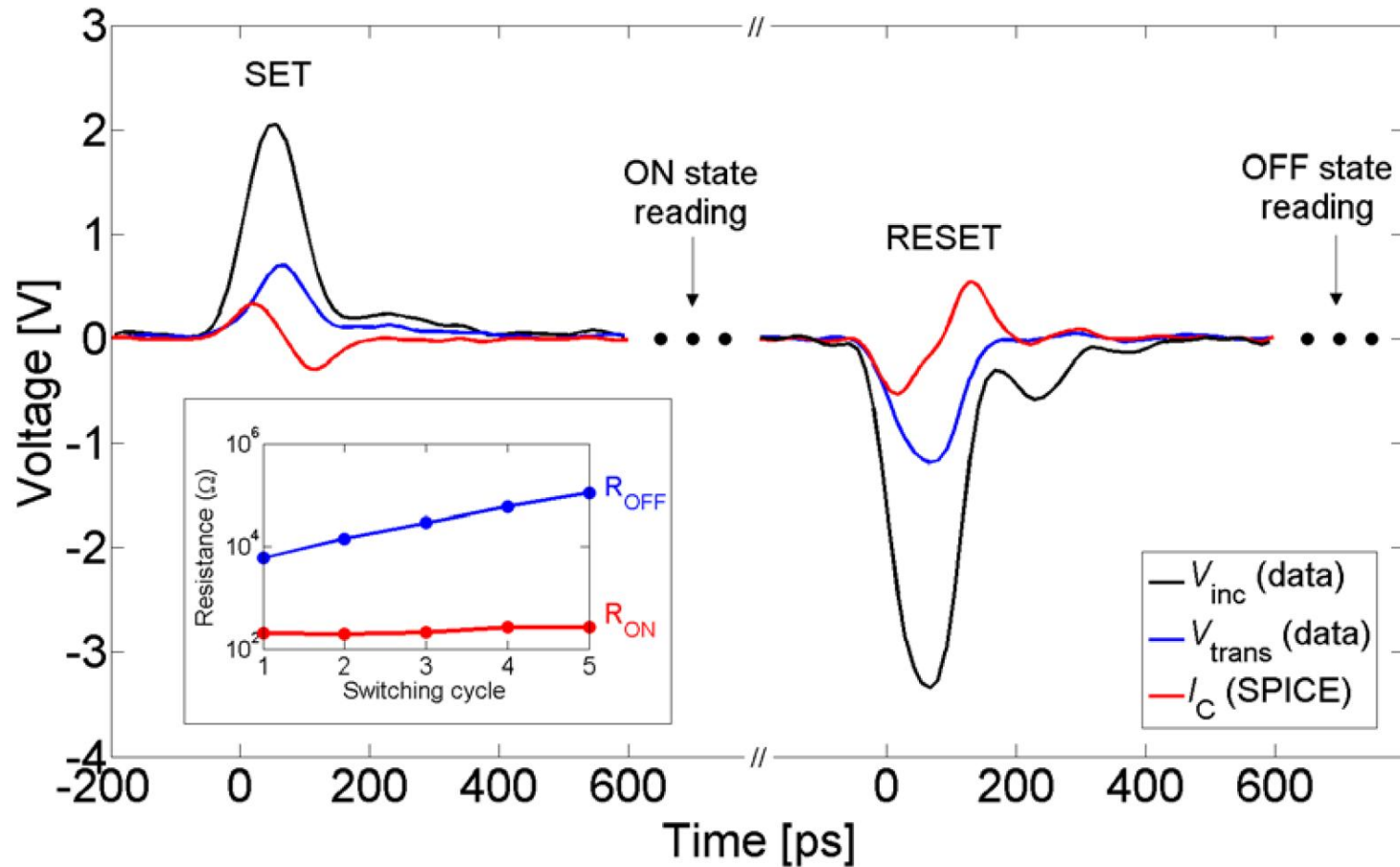


memristor
junction

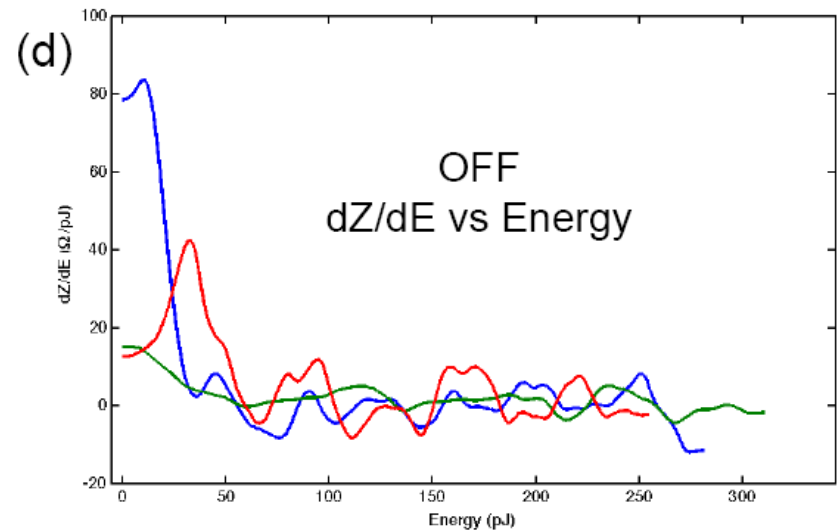
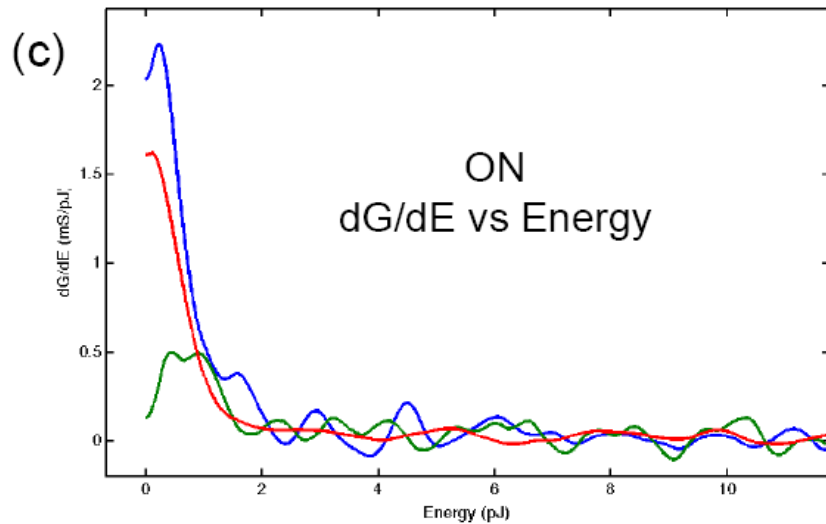
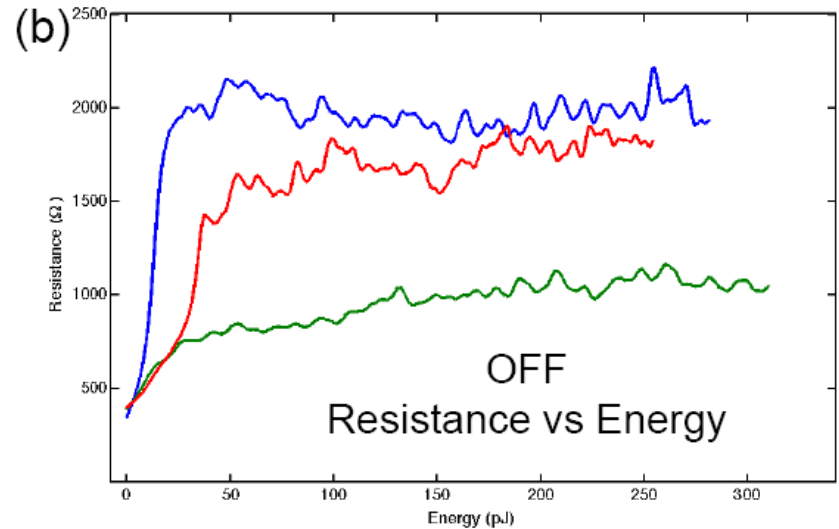
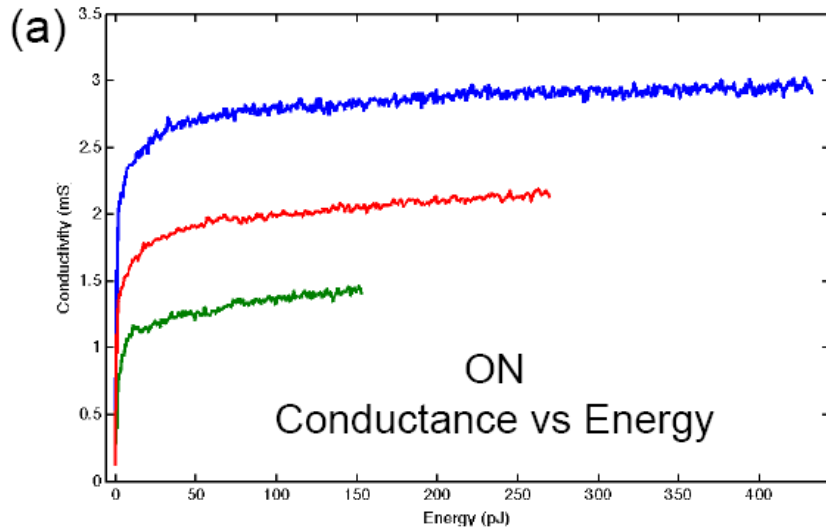


SWITCHING TIMES

SET and RESET in ~ 100 picoseconds @ $\sim 2V$



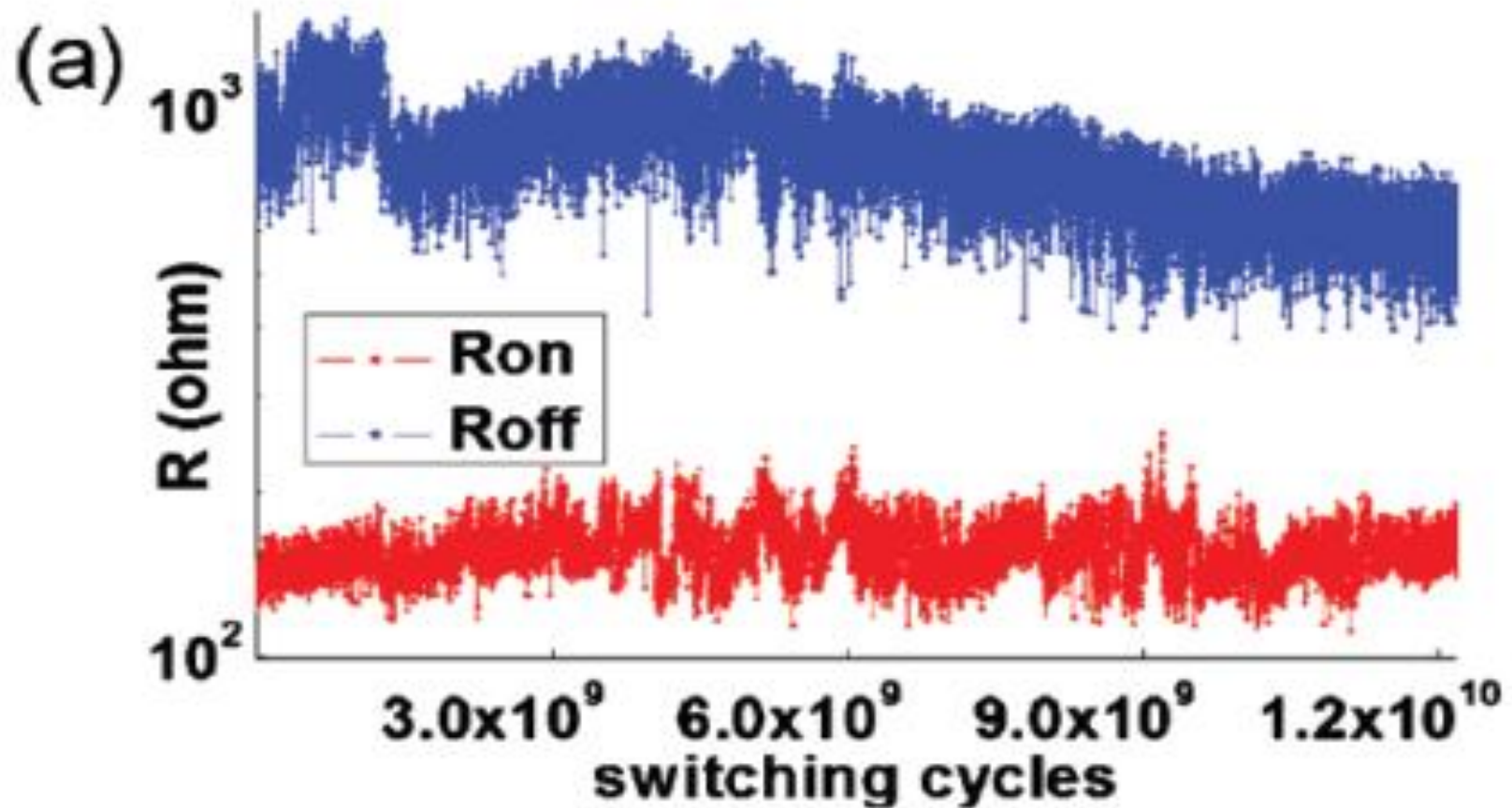
SWITCHING ENERGY @ ~0.5V



SOME RECENT RESULTS (TAOX):

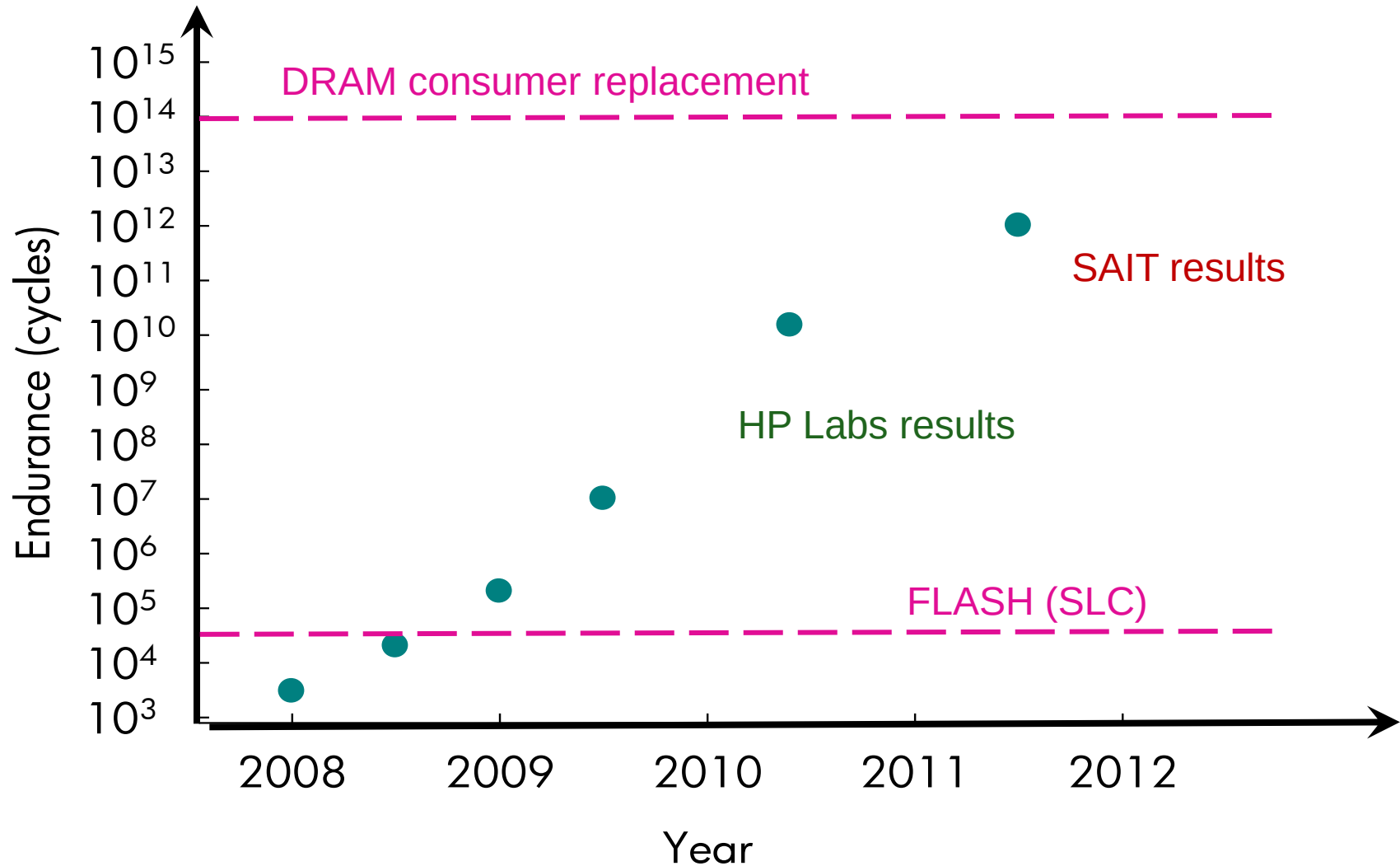
– Endurance: $>10^{10}$ cycles $\Rightarrow$

Yang *et al.*, APL **97**, 232102 (2010)



ENDURANCE

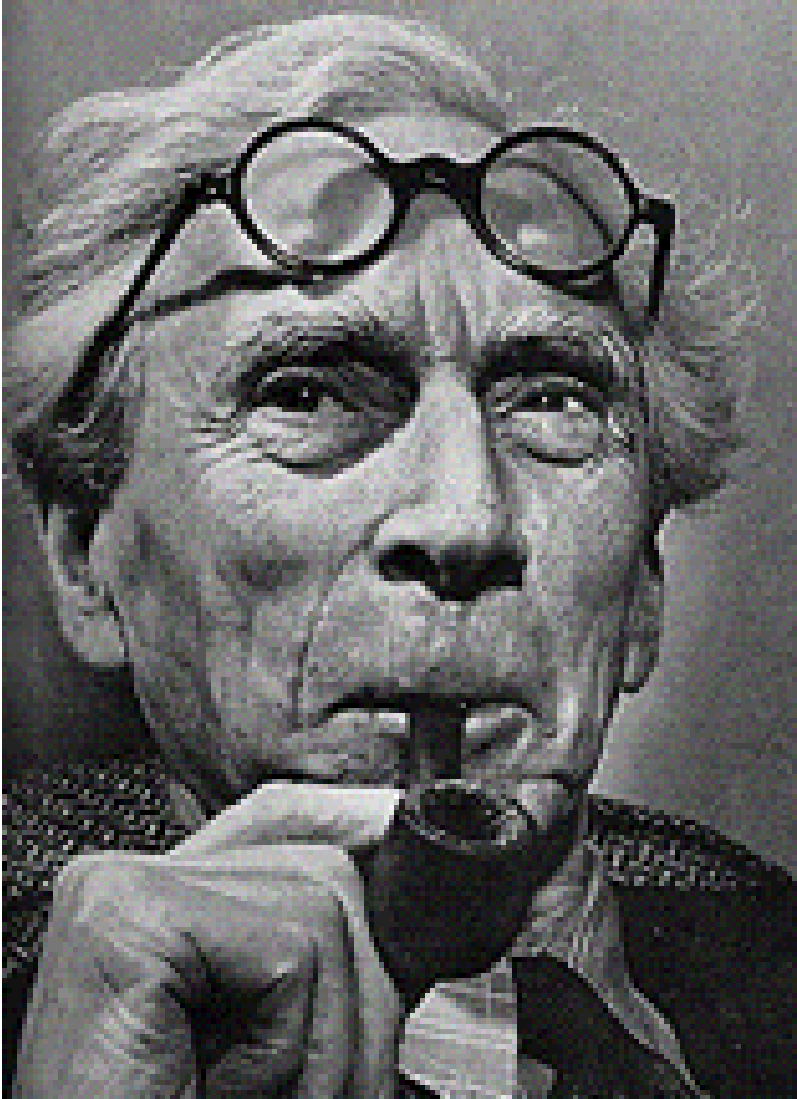
A Future



Memristor Logic

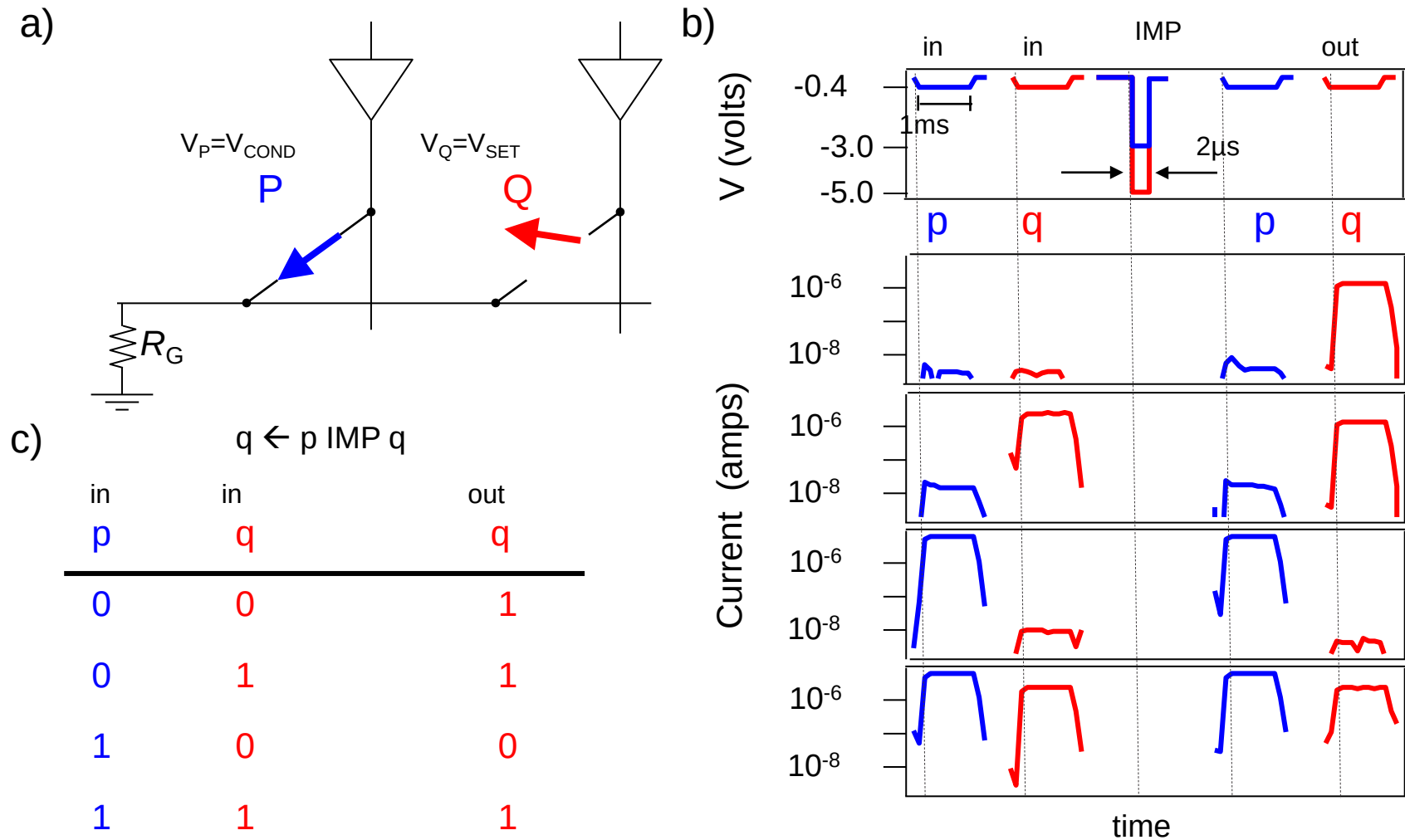


Bertrand Russell



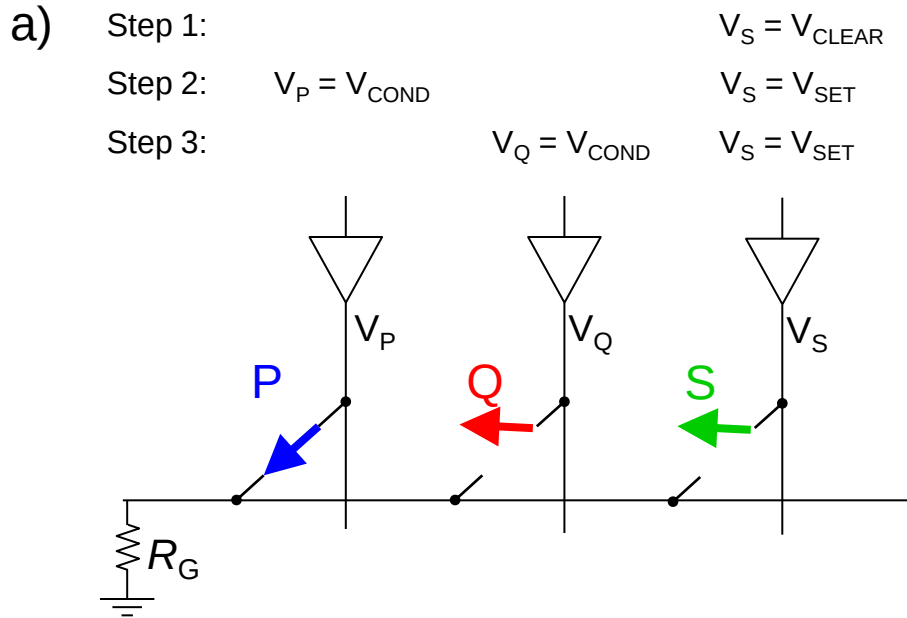
Bertrand Russell studied logic extensively in the early 1900's. He viewed the 'Material Implication' operation, which along with FALSE forms a complete basis for universal computing, as especially interesting.

Experimental Test of Memristor IMP operation



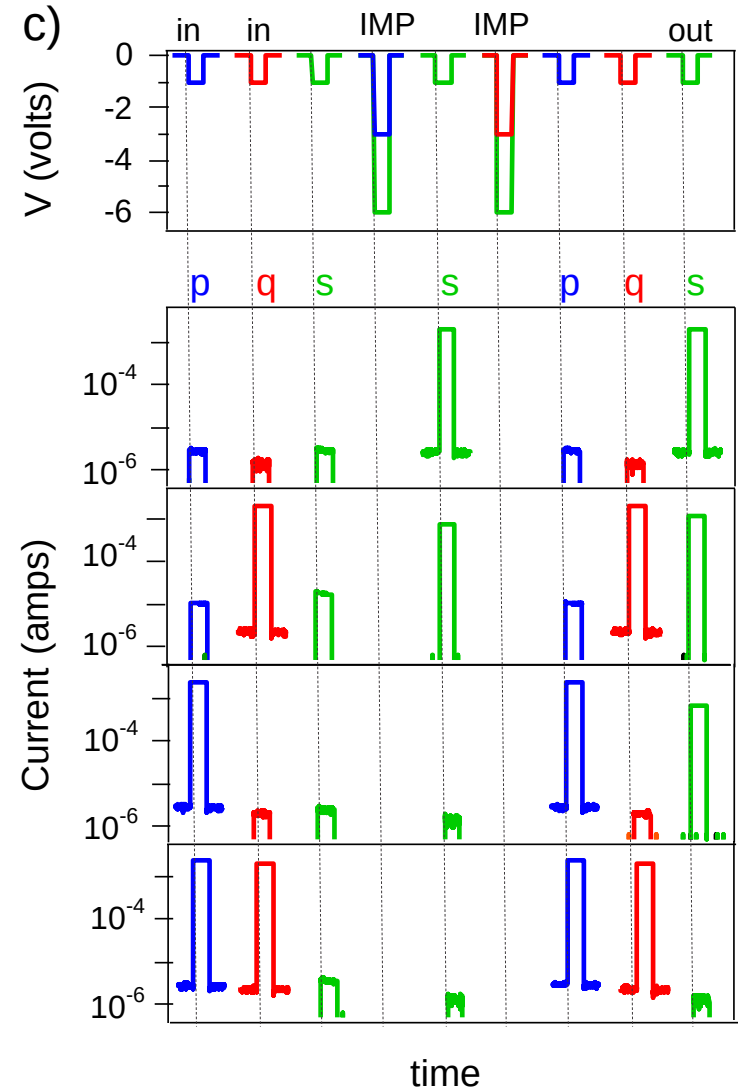
Borghetti et al., Nature (2010)

Experimental Demonstration of Memristor NAND



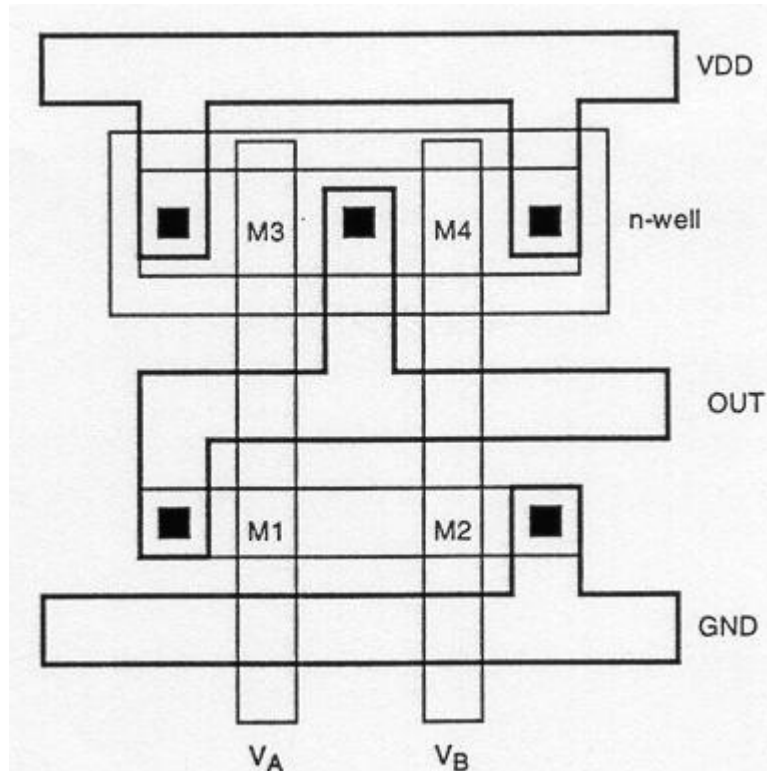
b)

Step 1	Step 2			Step 3			Steps 1-3		
s=0	s ← p IMP s			s ← q IMP s			s ← p NAND q		
s	p	s	s	q	s	s	p	q	s
0	0	0	1	0	1	1	0	0	1
0	0	0	1	1	1	1	0	1	1
0	1	0	0	0	0	1	1	0	1
0	1	0	0	1	0	0	1	1	0



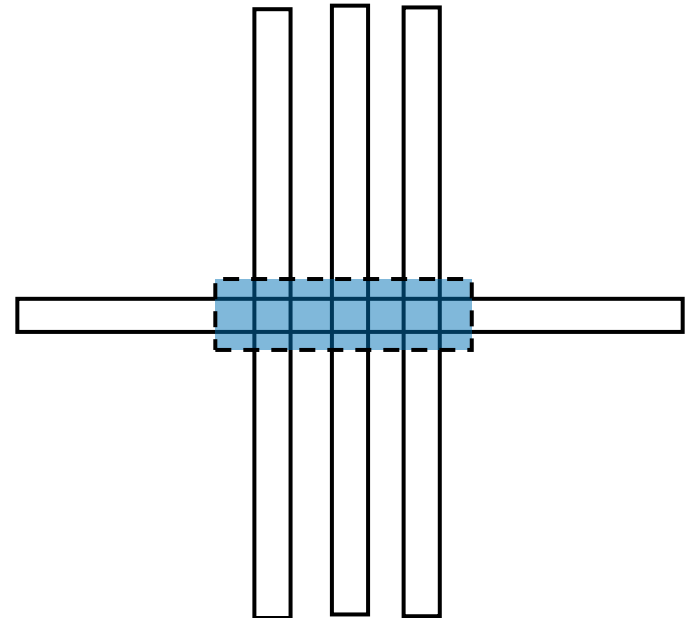
Area comparison of NAND gates

CMOS NAND gate



$$\begin{aligned}\text{Area} &= 36 \times (\text{FP})^2 \\ &= 0.12 \mu^2 @ 30 \text{ nm hp}\end{aligned}$$

SIMPL NAND gate



$$\begin{aligned}\text{Area} &= 3 \times (\text{FP})^2 \\ &= 0.01 \mu^2 @ 30 \text{ nm hp}\end{aligned}$$

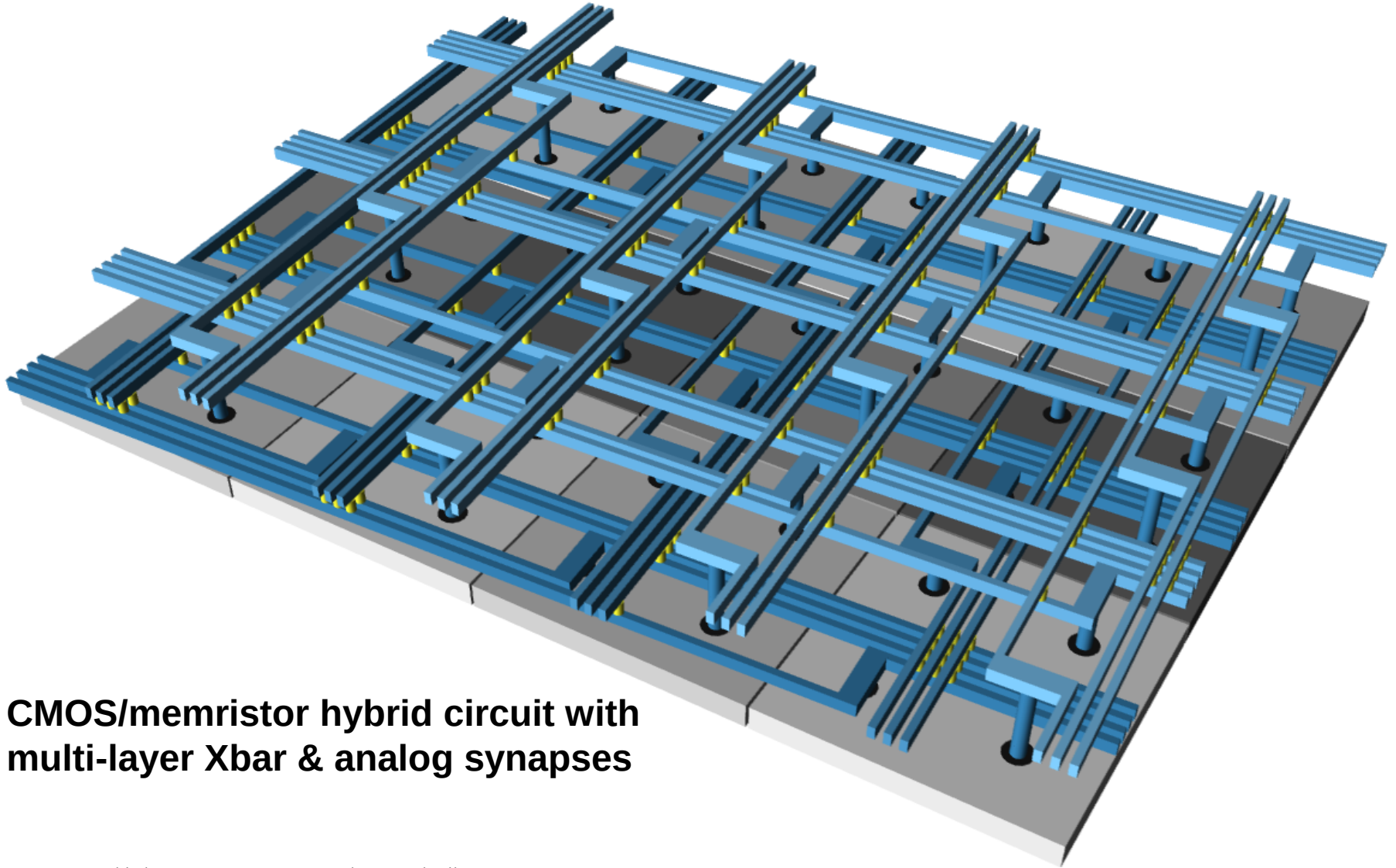
SUMMARY OF IMPLICATION LOGIC

- Memristors → *state machines*.
- Linear array + demux; simple and dense.
- State encoded with impedance, not voltage.
- No static power dissipation.
- Nonvolatile.
- Material Implication (IMP) and FALSE are complete
- Need to ask how the nanoscale world wants to compute, not impose our preconceptions!

SYNAPTIC COMPUTING

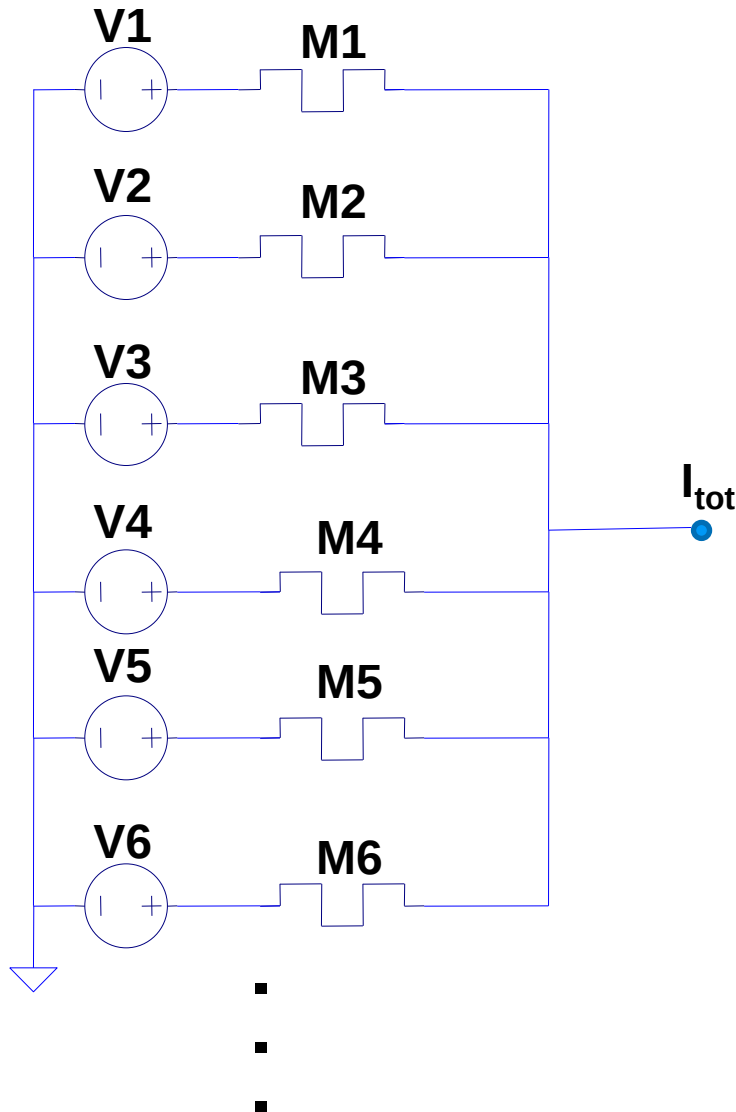


HYBRID XBAR SYNAPTIC CIRCUIT



**CMOS/memristor hybrid circuit with
multi-layer Xbar & analog synapses**

THE MEMRISTOR AS AN ANALOG SYNAPSE:



Calculate the dot product

$$I_{\text{tot}} = \mathbf{V} \cdot \mathbf{M}^{-1}$$

For a chip with 10^9 memristors
and a clock speed of 1 MHz,

The equivalent computation is

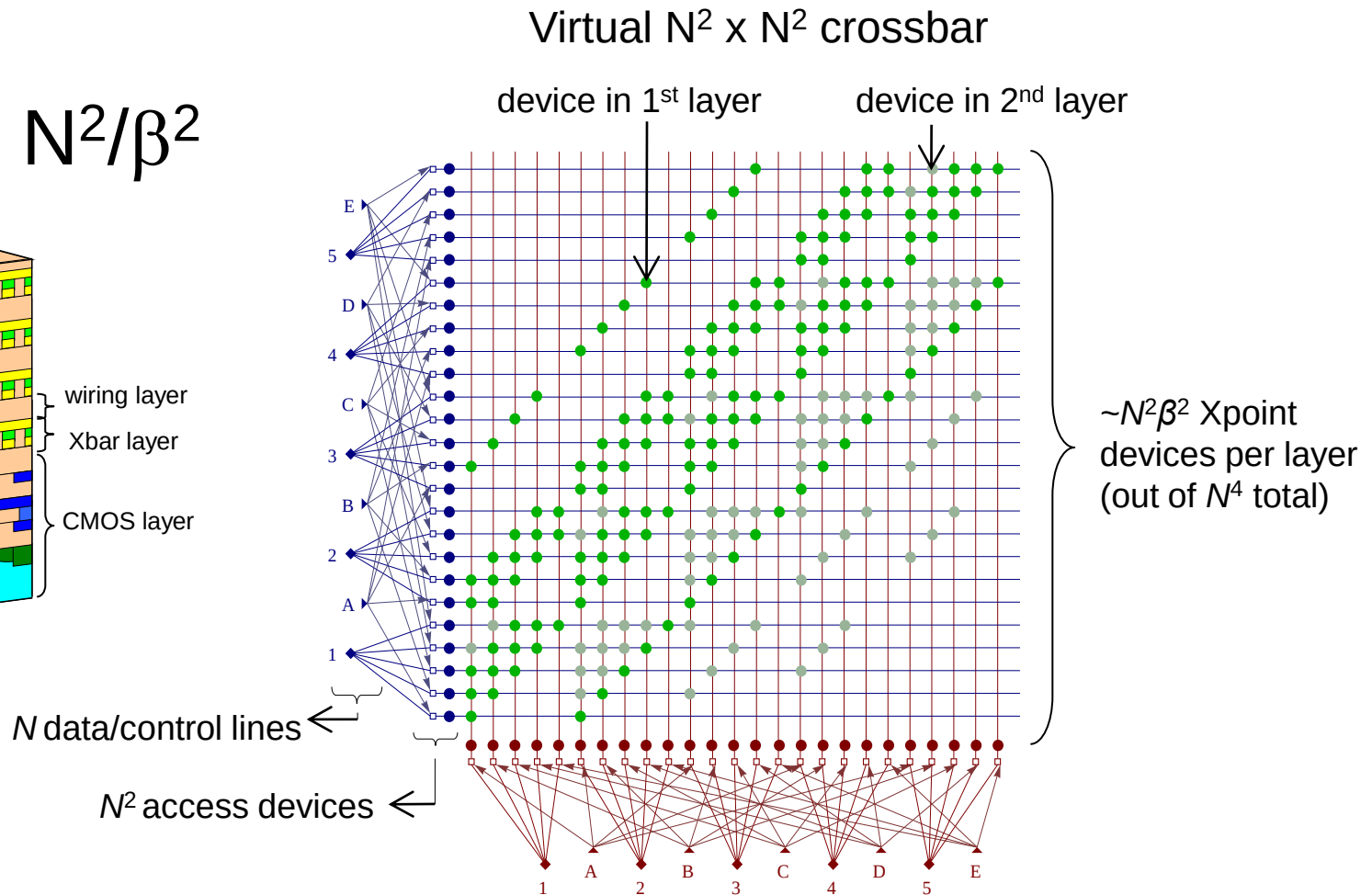
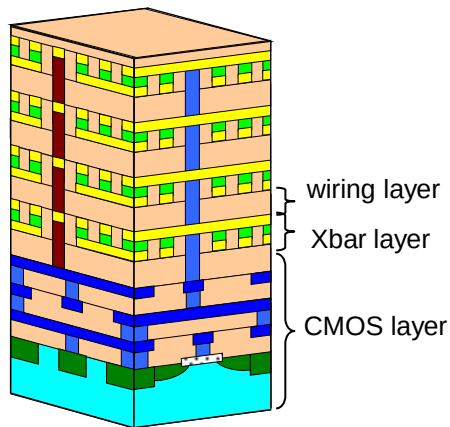
10^{15} FLOPS, i.e. a petaFLOP
(floating point operation per sec)

3D ARCHITECTURE



ARCHITECTURE: 4-D ADDRESS SPACE FOR M CROSSBARS!

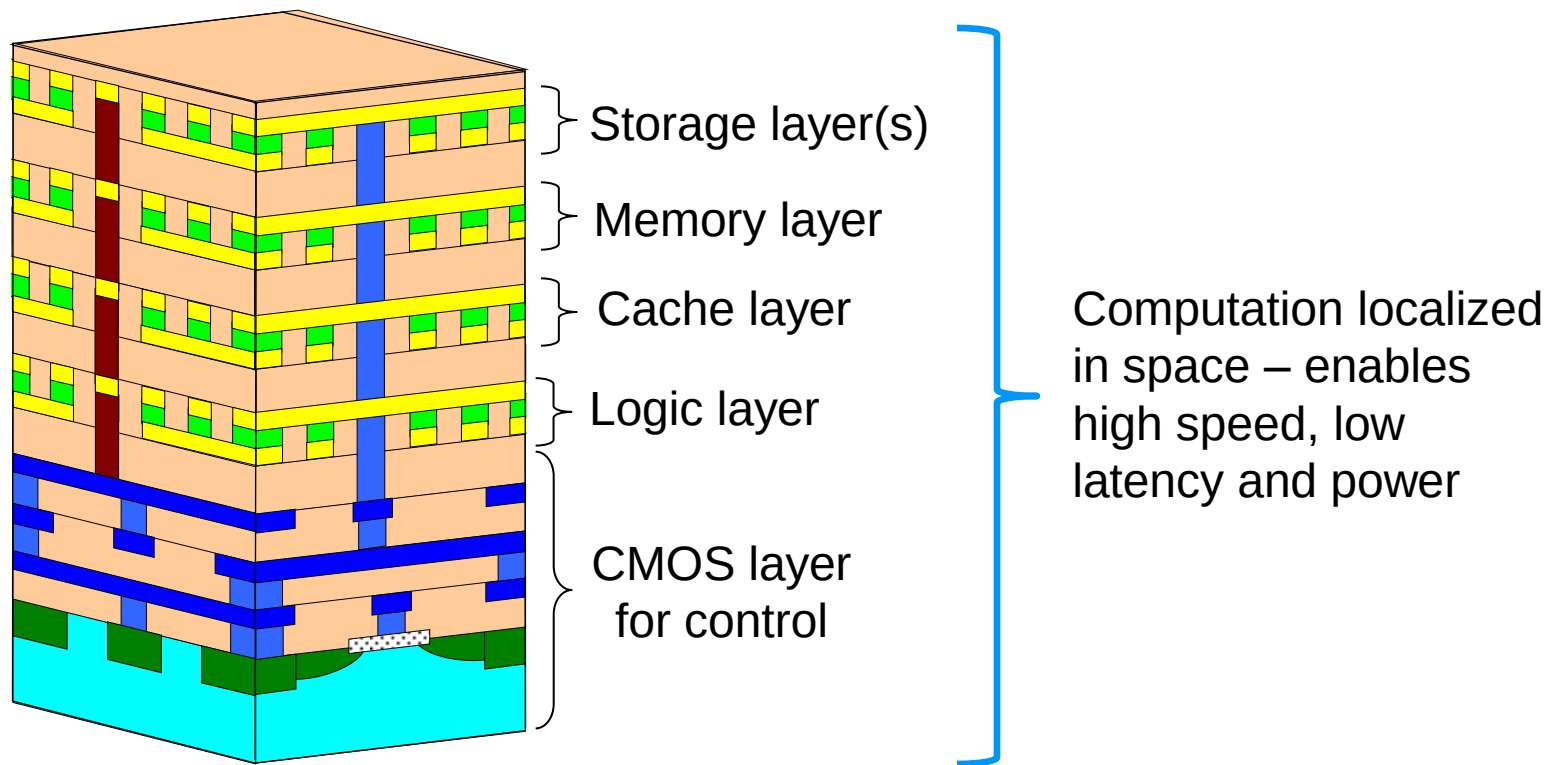
$$M = N^2/\beta^2$$



Can address any crosspoint in M crossbars with a single sparse set of vias!
The CMOS pitch can be much larger than the crossbar pitch

3D CROSSBAR ARCHITECTURE: LOGIC AND STORAGE

→ Longer range data transport done with photonics



Many layers per mask step needed –
Unlikely to be developed by industry

NEGATIVE DIFFERENTIAL RESISTANCE



THRESHOLD SWITCHING IN OXIDES

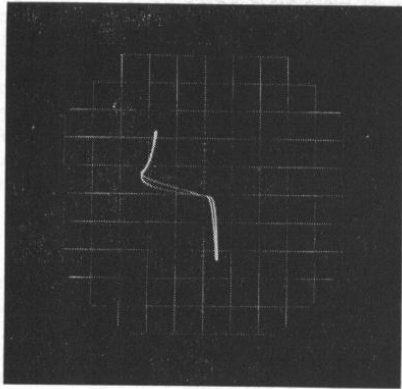


Fig. 1—Current-voltage trace of niobium oxide using mercury counter-electrode. Vertical scale 0.6 ma/division, horizontal scale 5 volts/division. The negative resistance region corresponds to the mercury being negative relative to the niobium.

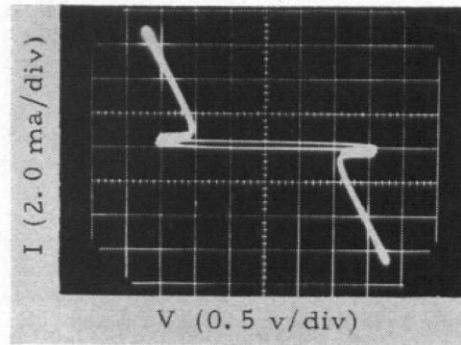


Fig. 1—I-V characteristics at 78°K with a negative resistance region.

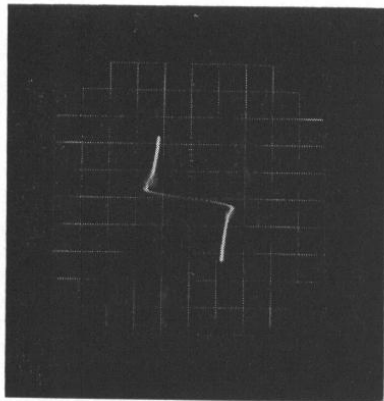


Fig. 2—Symmetrical current-voltage trace of niobium oxide using probe counter-electrode. Parasitic oscillations are visible in the negative-resistance regions. Vertical scale 0.1 ma/division, horizontal scale 5 volts/division.

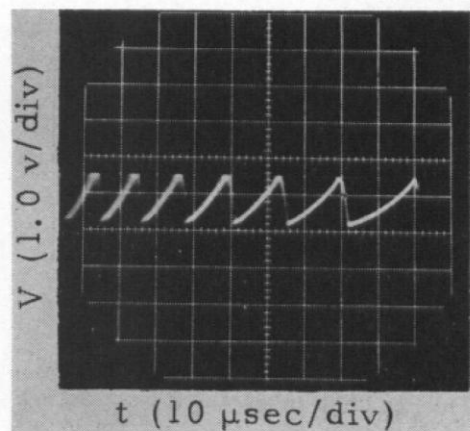
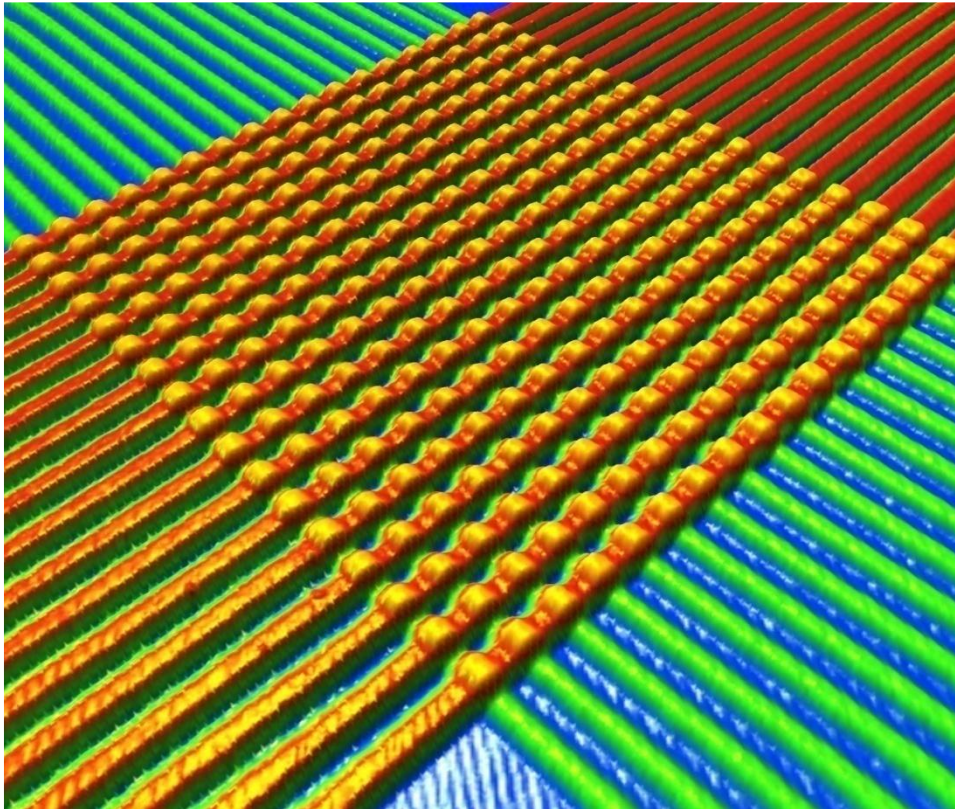


Fig. 3—Trace of sustained oscillations in the negative resistance region.

Threshold switching and resulting oscillations first observed in niobium oxide and later in related oxides. these are the same materials that display memristance.

Thus, we obtain two important and different properties from the same CMOS compatible material system.

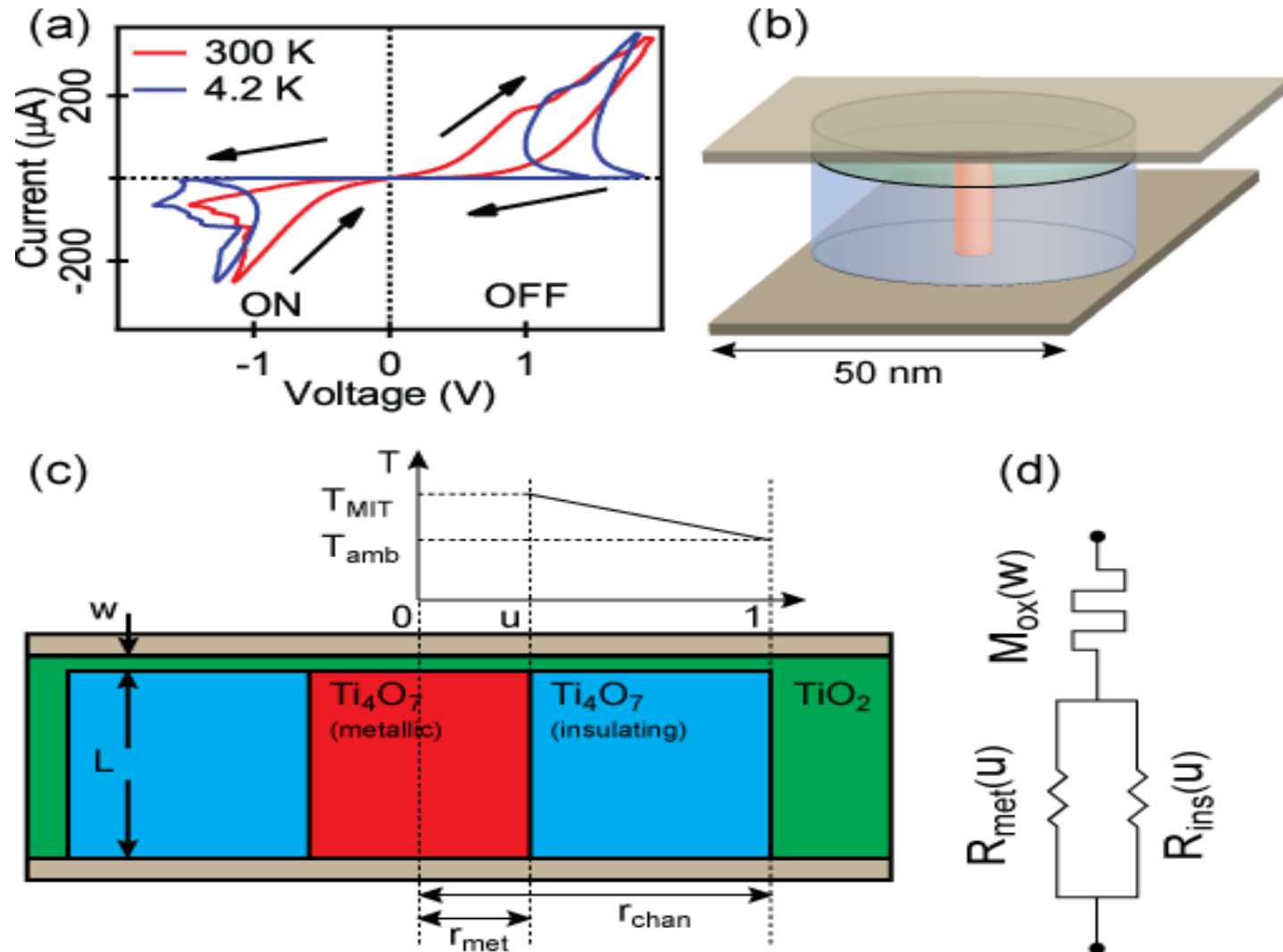
WHY IS THIS INTERESTING NOW?



Nanoscale crossbar circuits:

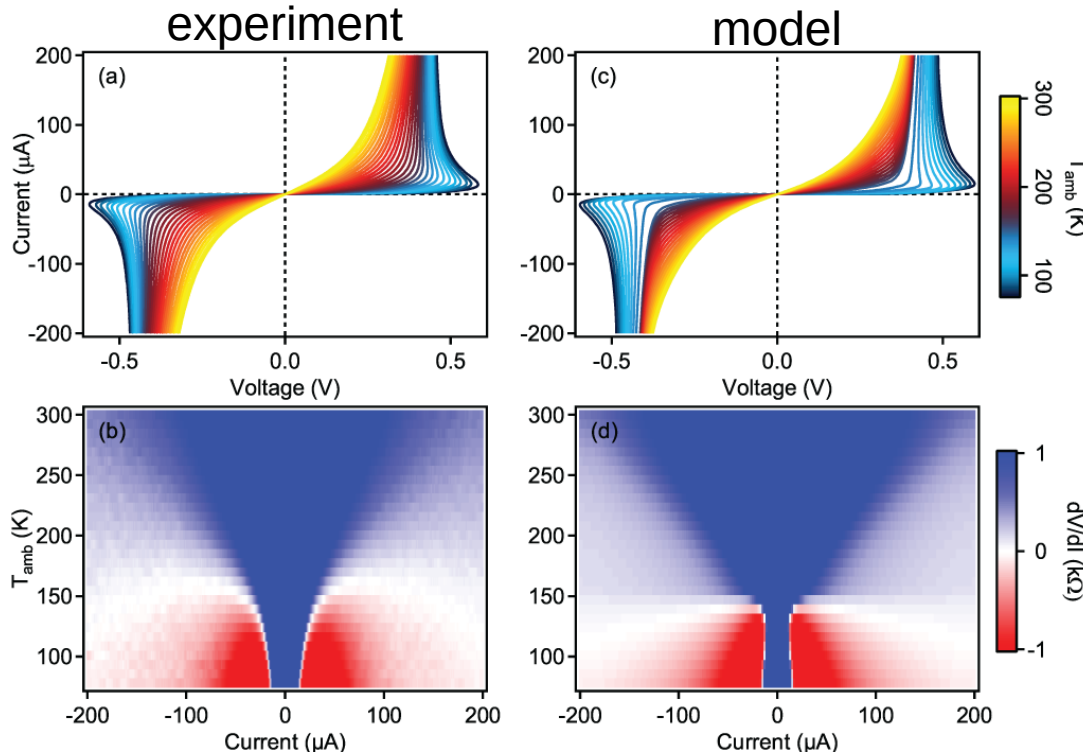
- $4F^2$ integration density
- Stackable/CMOS compatible
- 2 terminal devices
- Switching power scales with area
- Switching speed scales with area^{-1}
- Based on 'bulk properties' – no statistical issues with small volume doping

MEMRISTANCE AND NEGATIVE DIFFERENTIAL RESISTANCE



NEGATIVE DIFFERENTIAL RESISTANCE/ INSULATOR TO METAL TRANSITION

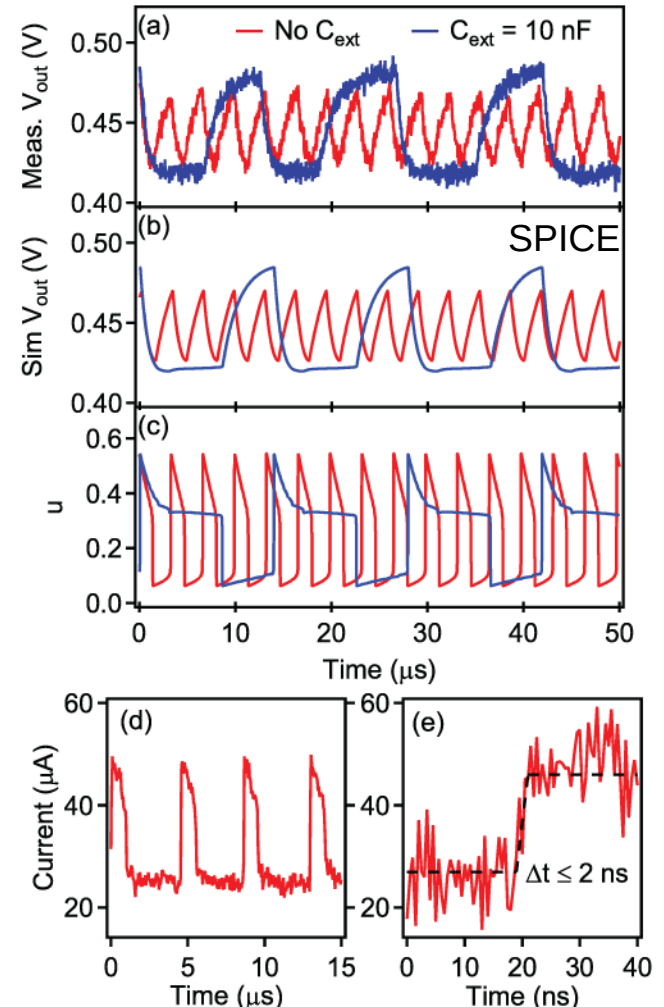
Ti₄O₇ I-V-T



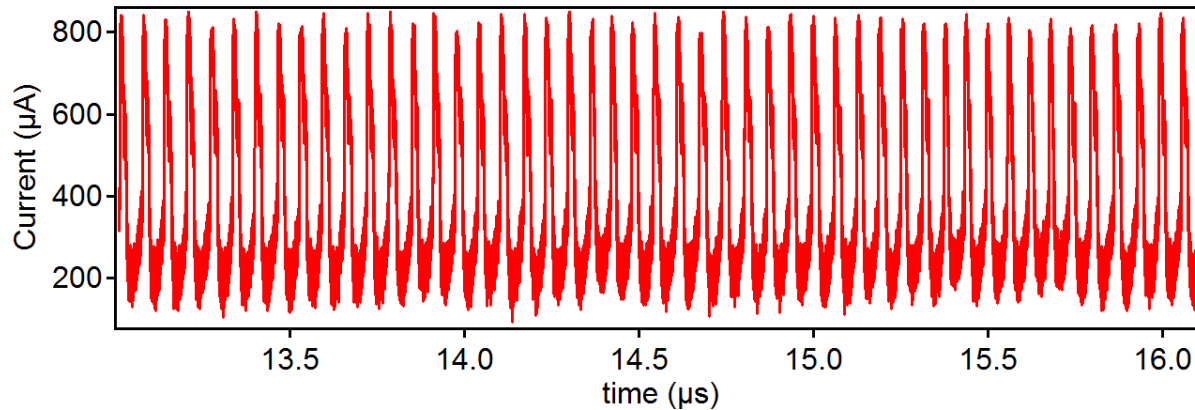
$$G_{\text{chan}}(i, T_{\text{amb}}) = \frac{\pi r_{\text{chan}}^2}{L} \left(\frac{u^2}{\rho_{\text{met}}} + \frac{(1-u)^2}{\rho_{\text{ins}}} \right)$$

$$u(i, T_{\text{amb}}) = \frac{r_{\text{met}}}{r_{\text{chan}}} = \exp \left[-\frac{1}{2} W_0 \left(\frac{4\pi^2 \kappa r_{\text{chan}}^2 (T_{\text{MIT}} - T_{\text{amb}})}{i^2 \rho_{\text{met}}} \right) \right]$$

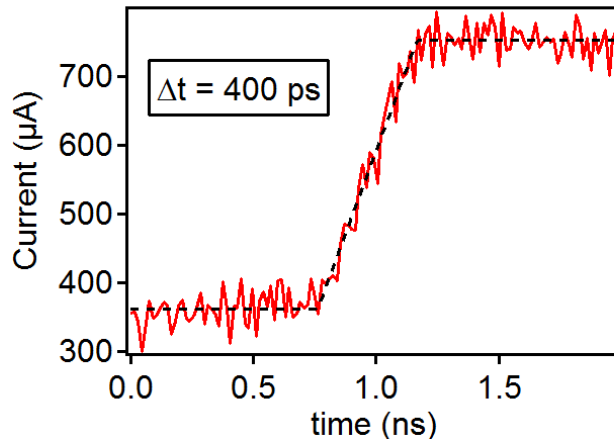
Free oscillations



FAST TRANSITION DYNAMICS



DC/AC conversion
'self-oscillations'



IM Phase transition time $\leq 400 \text{ ps}$

Primary limitation is capacitance of
oscilloscope

Potential for multi-GHz electronics

MEMRISTORS AND NDR COMPLEMENT CMOS

The materials used to make memristors and the newly discovered NDR devices are completely CMOS compatible – they can be inserted into the “interconnect” layers to provide a wide range of functionality.

For many applications, memristors and NDR devices can replace significant numbers of transistors in a circuit, and in the process dramatically increase the functionality per transistor and speed of operation while decreasing the power consumption of the circuit.

Q&A

