1. A competitor is selling a certain chip at $12.50 (net of test, packaging, etc.). Its die size is 65 mm$^2$ and is produced from a wafer diameter of 21 cm$^2$. We know that the wafer cost is $5,000. Assuming they are selling without a profit, what is the fab process defect density, $\rho_D$? $\ldots$

What is the minimum price they can sell this for, regardless of $\rho_D$? $\ldots$

We need to compete with this die. Our design also uses 65 mm$^2$, but we have access to a new fab with larger wafers (diameter 30cm). It has $\rho_D = 0.4$ defects/cm$^2$, and wafer cost of $7,000.

What will be the yield and cost per good die? $\ldots\%$, $\ldots$. 

2. An L2 on-chip cache has a minimum cycle time (and access time) of 4.9 nsec. We want to use it with a processor with cycle time of $\Delta t = 1.4$ nsec. Because of high L1 miss rates, we’d like to pipeline accesses to L2 at the processor cycle rate, but there is only one latched segment (the address to the data array) within the L2. Design data shows that

<table>
<thead>
<tr>
<th>Segment</th>
<th>max*</th>
<th>min</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2.4</td>
<td>1.8</td>
</tr>
<tr>
<td>2</td>
<td>2.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Total</td>
<td>4.9</td>
<td></td>
</tr>
</tbody>
</table>

* includes clock overhead

(a) It is proposed to use wave pipelining to run the L2 at the processor request rate, so the L2 is now accessed every __________ nsec, with clock skewed at $CS1 =$ __________ nsec, and segment 2 skewed at $CS2 =$ __________ nsec.

(b) If no clock skewing were allowed, but we could pad delays (max and min) in each segment of the L2, could we still match the processor request rate? _______

If so, we would pad segment 1 by _______ nsec and segment 2 by _______ nsec.

(c) Under the conditions of part (a), the processor would see an L2 access time of _______ processor cycles.
3. A network routing processor is latency tolerant and can process packets at 10K packet per second. Assume its service time is constant.

(a) On a certain day it is observed to be idle 30% of the time.
   What is the average number of packets awaiting service? _______

(b) What is the mean packet arrival rate? _______ packets/sec.

(c) What is the expected total time for a packet to be processed by this router? _______

(d) On other days when the total mean service time exceeds 300 \( \mu \text{sec}/\text{packet} \), the requesting node redirects packets to other nodes in the network.
   This corresponds to an occupancy of _______.
   The queue size at this point is _______.
4. A high speed processor uses an 8-way interleaved data cache \((T_c = 2\text{ cycle})\) to improve performance. The processor has 2 LD/ST units (one LD or ST can be issued by each unit each cycle). The processor architecture makes a 0.5 data refr (i.e., LD and ST combined) per instruction. The processor issues 4 instructions per cycle.

(a) The effect of cache contention is to lower the ideal IPC (instructions per cycle) from 4 to _______ IPC.

(b) By carefully scheduling the LD/ST instructions ahead of their use, it is proposed to buffer out conflicts and tolerate accessing delay. If we could achieve the ideal IPC, each request would have to tolerate a mean delay of _______ cycles. There would be a total of _______ requests waiting for service from the cache.
5. A video frame processor fetches frames from a network processor for decode and display. It decodes and displays at 30 frames per second. If it takes 200 ms latency to fetch a frame from the network (at 30 frames/sec), how many frames should be buffered to ensure that no frame processing disruptions occur? ______

To this number, we are told to add four additional frames for frame sorting. Why?

With ______ frames buffered (your answer above, plus four), what is the total processing time for a frame in the frame processor? ______ ms.

What is the probability that an overflow occurs in the frame buffer memory? ______

Note: Assume one frame is fetched at a time from the network processor, and that a fetch cannot begin unless there is a buffer available in the frame processor.