Chapter 7. Concurrent Processors

Problem 7.2

1. \( F37B90_{16} = 330313232100_4 \)

\[
 r = (0 - 0 + 1 - 2 + 3 - 2 + 3 - 1 + 3 - 0 + 3 - 3) \mod 5 = 5 \mod 5 = 0
\]

So, module address = 0

\[
\begin{align*}
330313232100_4 \\
- 000230211000_4 \\
\hline
030023021100_4 = 30B250_{16}
\end{align*}
\]

So, address in module = 30B250_{16}

2. \( AA3347_{16} = 222203031013_4 \)

\[
 r = (3 - 1 + 0 - 1 + 3 - 0 + 3 - 0 + 2 - 2 + 2 - 2) \mod 5 = 7 \mod 5 = 2
\]

So, module address = 0

\[
\begin{align*}
222203031013_4 \\
- 202002210012_4 \\
\hline
020200221001_4 = 220A41_{16}
\end{align*}
\]

So, address in module = 220A41_{16}

1
Problem 7.3

\[
\begin{array}{cccccccc}
m_3 & m_2 & m_1 & m_0 & m'_3 & m'_2 & m'_1 & m'_0 \\
0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 \\
0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 1 & 1 & 1 & 1 & 0 & 1 \\
0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 \\
0 & 1 & 0 & 1 & 0 & 0 & 1 & 1 \\
0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 \\
1 & 0 & 1 & 1 & 1 & 1 & 0 & 0 \\
1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \\
1 & 0 & 0 & 1 & 1 & 1 & 1 & 1 \\
1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 1 & 1 & 0 & 1 & 0 & 1 \\
1 & 1 & 0 & 0 & 1 & 1 & 1 & 0 \\
1 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \\
1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\
1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 \\
\end{array}
\]

Since each original address maps to a unique hashed address, the scheme works.

2. \(F37B90_{16}\)

The 4 least significant bits are 0000\(_2\) which map to 0010\(_2\), thus the module address is 2.

\(AA3347_{16}\)

The 4 least significant bits are 0111\(_2\) which map to 1001\(_2\), thus the module address is 9.

Problem 7.4

\(\Delta T = 8\) ns

Memory cycle time \((T_c) = 64\) ns

Two requests per \(\Delta T\)

1. Offered memory bandwidth

\[n = 2 \times \frac{64}{8} = 16\]

\[\lambda = \frac{n}{T_c} = \frac{16}{64 \times 16} = 250\text{ MAPS}\]

Assume 64 bit word size
\[ \lambda = 250 \text{ MAPS} \times 8 \text{ bytes} = 1907 \text{ MBps} \]

2. Achieved bandwidth

Use \( M_B/D/1 \)

\[
B(m,n) = 8 + 16 \cdot \frac{1}{2} \sqrt{(8 + 16 - .5)^2 - 2 \times 8 \times 16} = 6,288
\]

\[
\lambda_{ach} = \frac{B}{n \times \lambda_{offered}} = \frac{6,288}{16} \times 1907 \text{ MBps} = 750 \text{ MBps}
\]

3. Mean queue size

\[
q_{\text{mean}} = n - B = 16 - 6,288 = 9,712
\]

**Problem 7.8**

\[ \gamma = .5, m = 17 \]

\( n = 16 \) and \( T_c = 64 \text{ ns, from problem 7.4} \)

Assume 64 bit word size.

\[
B(m,n,\gamma) = 17 + 16(1+.5)\cdot.5 - \sqrt{(17 + 16(1+.5)\cdot.5)^2 - 2 \times 16 \times 17(1.5)} = 11.79
\]

\[
\lambda_{ach} = \frac{B}{T_c} = \frac{11.79}{64 \times 10^{-9}} \approx 184 \text{ MAPS} = 1405 \text{ MBps}
\]

**Problem 7.10**

4 memory requests/\( \Delta T \)

\( \Delta T = 8 \text{ ns} \)

\( T_c = 42 \text{ ns} \)

1. Minimum number of interleaving for no contention

\( m > n \)

\( m > 4 \times \frac{42}{8} = 21 \), or \( m = 32 \) if only powers of 2 are allowed.

2. \( m = 64 \)

\[
\gamma_{\text{opt}} = \frac{n-1}{2m-2n} = \frac{21-1}{2 \times 64 - 2 \times 21} = .233
\]

Mean TBF = \( n \times \gamma_{\text{opt}} = 21 \times .233 = 4.893 \)

\[
B(m,n,\gamma) = B(64,21,.233) = 20.567
\]

Relative perf = \( \frac{20.567}{21} = .979 \)
Problem 7.11

Assume that both the vector processor and the uniprocessor have the same cycle time. Assume that the uniprocessor can execute one instruction every cycle. Assume that the vector processor can do chaining.

The vector processor can load 3 operands concurrently in advance of using them since there are 3 read ports to memory. It can also store a result concurrently since there is a write port to memory. With chaining, the vector processor can perform 2 arithmetic operations concurrently if there are enough functional units.

Thus, the vector processor can perform 6 operations per cycle and the maximum speedup over a uniprocessor is 6.