Proposal for EE384y (Final Draft)
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Date: April 16, 2003

Throughput of Internally Buffered Crossbar Switch

1 Motivation and Objective

Crossbar switching system has been heavily investigated in last decade, and became a dominant switching fabric tecnology in current use. However, in order to achieve desirable performance (high throughput, low packet delay, and fairness, etc.), a complicated and computationally expensive scheduling algorithm is often needed. We want to analytically evaluate a new variation of crossbar - Internally Buffered Crossbar Architecture. Preliminary study will only consider i.i.d. Bernoulli traffic and IQ (input queue) crossbar. The second step will include non-uniform traffic and VOQ (Virtual Output Queue). The result we hope to obtain is to proof that even under simple scheduling algorithm, this new crossbar architecture can still deliver high performance at a reasonable cost to include extra hardware cost of internal buffer. The following is the diagram:

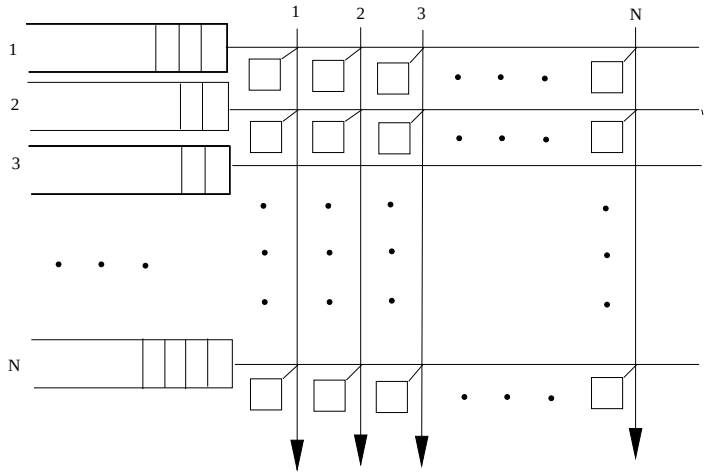

Diagram of a Internally-Buffered Crossbar Switch

2 Planned Research Schedule

- Week 1 Week3 - Literature review and simulations;
  - The first step will be to do extensive simulation to verify my conjecture. Totally three cases will be considered, (1) Write code to simulate the classic IQ crossbar without internal buffer, we want to observe the classic conclusion of 58 % of throughput, the purpose of

doing this is to get a sense of what the behavior of input queue will be when the maximal load is used. (2) Simulate the CIOQ(no VOQ) situation, we want to observe the impact of the size of output queue has on the throughput. (3) Finally, we want to do simulation of the behavior of the internally buffered crossbar. Especially, what will be the throughput.

- Week 4 Week7 - Modeling analysis and simulation;
  - There are 2 directions we want to investigate analytically: (1) It seems that directly analyze the internally buffered crossbar will be difficult, because of the expenential size of the state space, however, if we consider to move the internal buffer to output, what we have is one type of CIOQ, which is much easier to analyze. We want to tackle this problem first. Actully, this case should perform better than the internally buffered crossbar architecture.

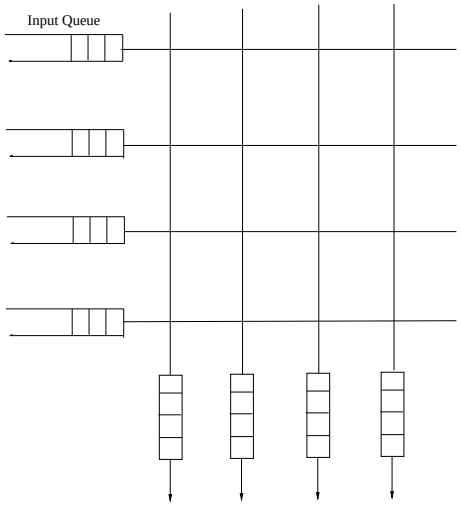

Fig3. Diagram of the CIOQ Crossbar without VOQ.

(2) We also want to find a way to accurately appoximate the internally buffered crossbar. We propose a queueing model to serve this model, which essentially a one input queue, multiple server, and with variable size of waiting room. The problem itself is also interesting, we hope to use this model to to analyze the internally buffered crossbar at certain accuracy.

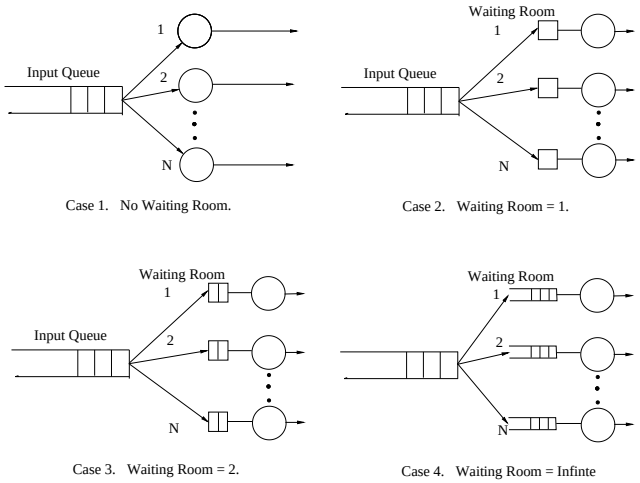

Fig2. Diagram of the Queueing Model of Different Cases.

- Week 8 end - Wrap up and writing report.
  - In the end, we want use some kind of mathmatical model to model the internally buffered crossbar, we are interested to find out what is the impact of having internal buffer at crosspoint on throughput, delay, and expected queue size. What we want to find out is where is the best place to place the buffer.