Cost of a Chip

- 300mm wafer will give 700 ~1cm² chips
- Material Costs (wafer, copper etc) ~5%
- Fab amortization cost ($3B/fab) plus Fab operational cost ~25%
- Personnel cost ~20%
- Package Cost ~10%
- Testing Cost ~40% !!!

Cost of Testing Semiconductor Chips

- Three main variable components
  - Test Application Time
    - When amortizing the cost of a tester over all chips, higher test time results in to higher actual cost
    - Rule of thumb: 1 second per chip!
  - Test Data Volume
    - Low and medium cost testers have limited storage
  - Tester Pins
    - Cost of a tester is directly proportional to the number of pins it supports

Example: An IBM chip

- 7million gates (logic only, RAM not included)
- 250k Flip-Flops
- Full Scan design, all FFs connected as shift register
- 7000 Test Vectors
- Test Application Time: $7000 \times 250k = 1.75G$ cycles
  - at 100MHz scan speed it takes 17.5 Seconds!
  - at 500MHz scan speed it takes 3.5 Seconds
- Tester memory required: $7000 \times 250k = 1.75G$ bits

Parallel Scan

- 1000 Parallel Scan Chains by 250 FFs
- Scan-in
- Scan-out
- 1000 scan-in pins!
- 1000 scan-out pins!
- Reduces Test Vector Load time by a factor of 1000!

Parallel Scan Output Compaction

- 100 Parallel Scan Chains by 2500 FFs
- Scan-in
- Scan-out
- output compactor
- A Combinational Compactor is a tree of XOR gates
- A Sequential Compactor is a Linear Feedback Shift Register with multiple parallel inputs XORed. Also called a Multiple Input Signature Analyzer (MISR)
Parallel Scan - Summary

- Scan loading time can be reduced by dividing the single scan chain into parallel scan chains
- Some Observations
  - Output compaction is well established
  - Number of scan chains is limited by the availability of pins on a chip and tester scan channels
  - Additional "pins" on an embedded core require more routing in the SOC
- Parallel Scan has no impact on test data volume

Some Observations

Output compaction is well established.
Number of scan chains is limited by the availability of pins on a chip and tester scan channels.
Additional "pins" on an embedded core require more routing in the SOC.

Parallel Scan has no impact on test data volume.

Test Vector Compaction

- For example, all 40 ISCAS 85 and ISCAS89 (full scan) circuits, sizes of the test sets generated by MinTest (Hamzaoglu and Patel, ICCAD 1998, pp. 283-289) meet lower bounds for 31 out of 40 ISCAS circuits.
- This shows that compaction has already reached theoretical lower bounds in many instances.
- So we must look for other solutions beyond vector compaction.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Lower Bound</th>
<th>Min Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>C432</td>
<td>27</td>
<td>27</td>
</tr>
<tr>
<td>C5315</td>
<td>37</td>
<td>37</td>
</tr>
<tr>
<td>C7552</td>
<td>65</td>
<td>73</td>
</tr>
<tr>
<td>S1196</td>
<td>113</td>
<td>113</td>
</tr>
<tr>
<td>S1423</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>S5378</td>
<td>97</td>
<td>97</td>
</tr>
<tr>
<td>S38714</td>
<td>62</td>
<td>68</td>
</tr>
</tbody>
</table>

Test Vector Compaction

- For example, all 40 ISCAS 85 and ISCAS89 (full scan) circuits, sizes of the test sets generated by MinTest (Hamzaoglu and Patel, ICCAD 1998, pp. 283-289) meet lower bounds for 31 out of 40 ISCAS circuits.
- This shows that compaction has already reached theoretical lower bounds in many instances.
- So we must look for other solutions beyond vector compaction.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Lower Bound</th>
<th>Min Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>C432</td>
<td>27</td>
<td>27</td>
</tr>
<tr>
<td>C5315</td>
<td>37</td>
<td>37</td>
</tr>
<tr>
<td>C7552</td>
<td>65</td>
<td>73</td>
</tr>
<tr>
<td>S1196</td>
<td>113</td>
<td>113</td>
</tr>
<tr>
<td>S1423</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>S5378</td>
<td>97</td>
<td>97</td>
</tr>
<tr>
<td>S38714</td>
<td>62</td>
<td>68</td>
</tr>
</tbody>
</table>

BIST: STUMPS Architecture


This has the same limitations as any other BIST based scheme.

Limitations of Logic BIST

- BIST is excellent for Data Volume Reduction, But
  - Lower Fault Coverage. Test Point insertion and/or additional logic in test generator is required to cover Random Resistant Faults.
  - Design Modification needed to permit any arbitrary test pattern.
    - Tri-State logic must be fully decoded
    - No floating bus is permitted, since unknown values can corrupt the signature
    - Switching activities of various modules, and hence the power, cannot be easily controlled
- Will almost always increase the tester time!
- Failure Diagnosis becomes extremely difficult.

Proposed New Method

- Illinois Scan Architecture
  - Applicable to full-scan embedded cores and full-scan stand-alone chips.
  - Addresses all issues raised earlier -
    - Low test application time, low pin overhead, and low test data volume.
  - Does not have any of the limitations of the BIST.
  - No test point insertions and No design modifications!
  - Undesirable test vectors can be filtered, e.g., Vectors that produce Tri-State Conflicts, Unknown value generation, or High switching activity.

Illinois Scan Architecture

1. Divide it up into several chains keeping the same Scan-in pin.
2. Add a MISR to compact the outputs.

Scan in → MISR → Scan out

Scan in → Multiple Input Signature Register → Scan out

Illinois Scan Architecture

1. Divide it up into several chains keeping the same Scan-in pin.
2. Add a MISR to compact the outputs.

Scan in → MISR → Scan out

Illinois Scan Architecture

1. Divide it up into several chains keeping the same Scan-in pin.
2. Add a MISR to compact the outputs.

Scan in → MISR → Scan out

Illinois Scan Architecture

1. Divide it up into several chains keeping the same Scan-in pin.
2. Add a MISR to compact the outputs.

Scan in → MISR → Scan out
In the figure shown on left, all three scan chains will have identical test vectors. Therefore, only applicable test vectors are 000 and 111 for the AND gate. Test vectors 100, 010 and 001 cannot be applied due to Broadcast constraint. This makes three faults on the AND gate untestable.

In practice, how serious is this problem? How many faults become untestable?

Additional Untestable Faults

- Illinois Scan puts constraints on inputs
  - Cannot generate tests for some of the faults that are testable under normal scan test
  - The number of such “Additional Untestable Faults” is surprisingly small even for arbitrary partition!
  - Experimental Data for Scan Chain divided into 16 chains (arbitrary partition), with a single scan input

Two Test Modes of Illinois Scan

1. Broadcast Test Mode
   - Reduces Scan Time by a factor of n
   - Reduces Scan Data by a factor of n
   - But may require many more vectors and may reduce fault-coverage!

2. Serial Test Mode
   - Used for covering the loss of fault-coverage in the Broadcast Mode
   - Generates “top-off vectors”.

Number of Test Vectors

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Vectors</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_s13207$</td>
<td>400</td>
</tr>
<tr>
<td>$f_s15850$</td>
<td>350</td>
</tr>
<tr>
<td>$f_s35932$</td>
<td>300</td>
</tr>
<tr>
<td>$f_s38417$</td>
<td>250</td>
</tr>
<tr>
<td>$f_s38584$</td>
<td>200</td>
</tr>
</tbody>
</table>

Number of Test Cycles

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_s13207$</td>
<td>200,000</td>
</tr>
<tr>
<td>$f_s15850$</td>
<td>175,000</td>
</tr>
<tr>
<td>$f_s35932$</td>
<td>150,000</td>
</tr>
<tr>
<td>$f_s38417$</td>
<td>125,000</td>
</tr>
<tr>
<td>$f_s38584$</td>
<td>100,000</td>
</tr>
</tbody>
</table>
Illinois Scan Data Volume

Circuit Versions: fs = full scan, and ILS = Illinois Scan, DIV16

Illinois Scan

internal scan chains

scan-in pin

output compactor

Illinois Scan with multiple pins

internal scan chains

external scan-in pins

output compactor

Case Study at Texas Instruments

Original Circuit: 150K logic gates, 9300 scan flip-flops
910 Scan Vectors, 94.25% stuck-at fault coverage

Divison Blocks

Serial Scan Fault Coverage

Serial Scan Vectors needed

Broadcast Fault Coverage

Broadcast Vectors needed

Data Volume Reduction Factor

<table>
<thead>
<tr>
<th>Illinois Scan Version</th>
<th>Broadcast Vectors</th>
<th>Broadcast Fault Coverage</th>
<th>Additional Untestable Faults</th>
<th>Serial Scan Vectors needed</th>
<th>Serial Scan Fault Coverage</th>
<th>Broadcast Vectors needed</th>
<th>Data Volume Reduction Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIV16</td>
<td>15,000</td>
<td>94.08%</td>
<td>733</td>
<td>53</td>
<td>70%</td>
<td>9700</td>
<td>1.4</td>
</tr>
<tr>
<td>DIV24</td>
<td>14,000</td>
<td>94.09%</td>
<td>692</td>
<td>38</td>
<td>67%</td>
<td>9500</td>
<td>2</td>
</tr>
<tr>
<td>DIV32</td>
<td>12,000</td>
<td>93.87%</td>
<td>1565</td>
<td>59</td>
<td>73%</td>
<td>8000</td>
<td>3</td>
</tr>
</tbody>
</table>

Similar reduction was also found in Transition Fault Data


IBM Data using Illinois Scan (OPMISR+)

<table>
<thead>
<tr>
<th>Design</th>
<th>Gate Count</th>
<th>Scan flip-flops</th>
<th>Test Time Reduction</th>
<th>Test Volume Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip1</td>
<td>1.7M</td>
<td>230k</td>
<td>130x</td>
<td>200x</td>
</tr>
<tr>
<td>Chip2</td>
<td>2.1M</td>
<td>31k</td>
<td>38x</td>
<td>54x</td>
</tr>
<tr>
<td>Chip3*</td>
<td>715k</td>
<td>41k</td>
<td>7x</td>
<td>21x</td>
</tr>
<tr>
<td>Chip4*</td>
<td>1.2M</td>
<td>65k</td>
<td>8x</td>
<td>12x</td>
</tr>
</tbody>
</table>

* These chips already had their scan divided by customer

"...scan fan-out, which is sometimes informally referred to as Illinois Scan [ix]. In the Cadence ATPG tools we refer to this as OPMISR+.”


Intel Data on Illinois Scan

From a Paper by D. Wu et. al. of Intel, published in 2003 Int. Test Conf.

“The first test chip has 81 scan-in and 81 scan-out channels, we use Illinois Scan with 4 scan-in and 81 scan-out. The results are quite surprising: both methods got the same test coverage.”

“We have implemented Illinois scan into one of the microprocessors, but the silicon results will not be ready for the timing of this year’s ITC.”
More Data on Illinois Scan

- 7M Gates, 250k flip-flops, 7000 test vectors


Illinois Scan in CAD Tools

- Cadence (formerly IBM)
  - Illinois Scan on their patented “OPMISR” is called OPMISR+
- Synopsys
  - Illinois Scan is called “Virtual Scan”
- Mentor Graphics
  - ATPG Tools understand and support Illinois Scan

Illinois Scan with multiple pins

- Large Industrial Circuits have used Illinois Scan with multiple pins
  - IBM ASIC-4 chip (Design and Test, Sept. 2002, pp. 65-72)
    - 1.14 million gates, 46 pins, 269 internal chains
  - Intel chips (Int. Test Conf., Sept. 2003, pp. 1229-1238)
    - ASIC-1, 4 pins, 81 internal chains
    - ASIC-2, 4 pins, 96 internal chains
    - Next generation microprocessor (no data given)
- All of the above scan-chain groupings are ad-hoc!

Illinois Scan with multiple pins

- Large Industrial Circuits have used Illinois Scan with multiple pins
  - IBM ASIC-4 chip (Design and Test, Sept. 2002, pp. 65-72)
    - 1.14 million gates, 46 pins, 269 internal chains
  - Intel chips (Int. Test Conf., Sept. 2003, pp. 1229-1238)
    - ASIC-1, 4 pins, 81 internal chains
    - ASIC-2, 4 pins, 96 internal chains
    - Next generation microprocessor (no data given)
- All of the above scan-chain groupings are ad-hoc!

Optimal Grouping of Chains

Objective:
Minimize number of Scan-In Pins without loss in fault coverage.

Compatibility among Chains

- Compatibility between two scan cells
  - Two inputs (scan cells) are compatible if and only if no fault becomes untestable as a result of tying the two cells to a single input (Chen&Gupta, ITC 1995)
- Compatibility between two scan chains
  - Two chains are compatible if and only if every pair of scan-cells that receive the same broadcast value are compatible (Hamzaoglu&Patel, FTCS 1999)
  - Determination of all pair wise compatibilities is computationally very expensive
  - Resort to an inexpensive algorithm which gives a subset of all compatible pairs

Incompatibilities from a Test Set

A Partially Specified Test Vector, 20-bits long folded on to 5 chains

001x 0xx1 x01x 0011 xx11

No conflicting values found

001x 0xx1 x11x 0011 xx11

Chains a and c are incompatible, so are chains c and d
Example of Chain Grouping

Given Incompatible Pairs:
AB, AD, AG, BD, BE, BF, CE, CF, EF, EG, EH, FH
Construct a Graph with Nodes=Chains and Edges=Incompatibility

Perform Graph Coloring Algorithm
Conflict-free Chain Grouping

Dual-mode Illinois Scan

Single Pin Broadcast Mode
Group Mode

Some Results on Pin Reduction

<table>
<thead>
<tr>
<th>Circuit</th>
<th>no. of Chains</th>
<th>no. of Pins</th>
<th>Reduction Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>s13207.1</td>
<td>64</td>
<td>8</td>
<td>8.0</td>
</tr>
<tr>
<td></td>
<td>107</td>
<td>9</td>
<td>11.8</td>
</tr>
<tr>
<td>s15850.1</td>
<td>54</td>
<td>7</td>
<td>7.7</td>
</tr>
<tr>
<td></td>
<td>89</td>
<td>11</td>
<td>8.0</td>
</tr>
<tr>
<td>s38417</td>
<td>52</td>
<td>7</td>
<td>10.4</td>
</tr>
<tr>
<td></td>
<td>82</td>
<td>7</td>
<td>11.7</td>
</tr>
<tr>
<td>s38584.1</td>
<td>90</td>
<td>7</td>
<td>12.8</td>
</tr>
<tr>
<td></td>
<td>119</td>
<td>8</td>
<td>14.8</td>
</tr>
</tbody>
</table>

Illinois Scan: Summary

- A simple DFT technique, ideal for reducing test costs for large chips
- Significant reduction in test application time, test data and test pins without loss in fault coverage
- Even a "dumb" partition is very effective!
- For very large chips, 200 fold reduction is likely!

"Things should be made as simple as possible, but not any simpler" Albert Einstein

More information on Illinois Scan