EE410 vs. Advanced CMOS Structures

Prof. Krishna Saraswat
Department of Electrical Engineering
Stanford University

EE410 CMOS Structure

- P+ poly-Si
- N+ poly-Si
- Al/Si alloy
- LPCVD PSG
- LOCOS Field oxide
- PMOS
- NMOS
- N-substrate
- P-well

General Features of the EE410 Process
- 7 mask levels
- 0.45µm minimum dimensions
- 540nm field oxide LOCOS isolation
- 10nm gate oxide
- p+ poly-Si gate for PMOS transistors and n+ poly-Si for NMOS transistors
- single mask n+ and p+ source/drain definition (no LDD)
- single level of aluminum/silicon metallization
- phosphosilicate glass (PSG) passivation
- non-silicided contacts (high metal contact resistance to poly and active regions)
Dual Well CMOS Technology

- Global Interconnect
- Semi-global Interconnect
- Local Interconnects

- N-well
- P-well
- PMOS
- NMOS
- Vias
- Intermetal Dielectric
- First Level Dielectric
- LOCOS Isolation
- P-Well
- N-Well
- P+
- N+
- LDD
- LOCOS

Feature Size Trend & Moore’s Law

- Reduction in transistor area has resulted in higher packing density and hence more complex chips

- Transistors Per Die
- Generation
- L_GATE
- Micron
Scaling of MOS Gate Dielectric

Gate SiO$_2$ thickness is approaching $< 10$ Å to improve device performance

- How far can we push MOS gate dielectric thickness?
- How will we grow such a thin layer uniformly?
- How long will such a thin dielectric live under electrical stress?
- How can we improve the endurance of the dielectric?

\[
 I_D \propto g_m \propto \frac{K}{\text{thickness}}
\]

(Ref: S. Asai, Microelectronics Engg., Sept. 1996)

MOS Technology in 2010

Gate oxide thickness $\sim$ 1 nm
Channel Length $\sim$ 20 nm
Junction depth $\sim$ 1-2 nm
Size of an atom $\sim$ 5Å

Technological Issues
- Gate dielectrics/electrode
- Shallow junctions
- Isolation
- Contacts
- Interconnections

In integrated system
- 10 billion components
- 10 interconnect layers
Problems in Scaling of Gate Oxide

- Below 20 Å problems with SiO$_2$
  - Gate leakage => circuit instability, power dissipation
  - Degradation and breakdown
  - Dopant penetration through gate oxide
  - Defects

MOSFET Scaling Limit: Leakage

- Ability to control $I_{on}$ will limit gate-length scaling
  - Thermionic emission over barrier
  - QM tunneling through barrier
  - Band-to-band tunneling from body to drain

- To suppress D/S leakage, need to use:
  - Higher body doping to reduce DIBL
    - lower mobility, higher junction capacitance, increased junction leakage
  - Thinner gate dielectric to improve gate control
    - higher gate leakage
  - Ultra-shallow S/D junctions to reduce DIBL
    - higher $R_{series}$
**High-k Dielectric Technology Evolution**

Physical thickness can be increased for MOS gate dielectric operation by using a higher K dielectric

\[ I_D \propto 8m \propto \frac{K}{\text{thickness}} \]

- **Today**
  - 20 Å SiO₂ \(K \approx 4\)
  - Si

- **Near future**
  - 40 Å
  - \(\text{Si}_3\text{N}_4\) \(K \approx 8\)

**Higher thickness \(\rightarrow\) reduced gate leakage**

---

**Parasitic S/D Resistance**

\[ I_{DS}^{\text{SAT}} = K \left( (V_{GS} - V_T) - I_{DS} R_{SD} \right)^\alpha \]

- **Problem in junction scaling:**
  - With scaling parasitic S/D resistance \(R_{SD}\) increases compared to channel resistance
  - Contact resistance \(R_{sd}\) is one of the dominant components for future technology
  - Problem more serious for PMOS

**Source:** Jason Woo, UCLA

---

**Stanford University**

EE410 Winter 2009
Solutions to Shallow Junction Resistance Problem

Extension implants

Elevated source/ drain

Silicidation

Device Isolation pitch as a function of minimum dimension

With decreasing feature size the requirement on allowed isolation area becomes stringent.
Scaling of Device Isolation

LOCOS based isolation technologies have serious problems in loss of area due to bird’s beak.

Trench isolation can minimize area loss

Physical Limits in Scaling Si MOSFET

Source/Drain
- Contact resistance
- Band-to-band tunneling
- Doping level, abruptness

Gate stack
- Tunneling current
- Gate depletion, resistance

Channel
- Surface scattering - the “universal mobility” tyranny
- Subthreshold slope limited to 60mV/decade (kT/q)
- $V_G - V_T$ decrease
- DIBL $\Rightarrow$ leakage

Net result: Bulk-Si CMOS device performance increase commensurate with scaling is unlikely beyond the 65 nm generation
New Structures and Materials for Nanoscale MOSFETs

1. Electrostatics - Double Gate
   - Retain gate control over channel
   - Minimize OFF-state drain-source leakage
2. Transport - High Mobility Channel
   - High mobility/injection velocity
   - High drive current for low intrinsic delay
3. Parasitics - Schottky S/D
   - Reduced extrinsic resistance
4. Gate leakage - High-K dielectrics
   - Reduced power consumption
5. Gate depletion - Metal gate

Non Planar MOSFETs

Vertical FET
Double Gate FinFET
Tri Gate FET
Seemingly Useful Devices

- **Single Electron Transistors (SET)**
  - Limited Current Drive
  - Cryogenic operation

- **Quantum Dot**
  - Limited Fan-Out
  - Critical dimension control

- **Resonant Tunneling Diode**
  - Challenging fabrication and process integration

- **Spintronics**
  - Need high spin injection and long spin coherence time

- **Molecular Device**
  - Limited thermal stability
  - New architectures needed

- **Carbon Nanotubes**
  - Controlled growth
**Limits of Interconnect**

Scaled wire with lower $A$ and longer $l$ has higher $R,C$ and $L$ and thus reduced bandwidth, higher delay and higher power dissipation.

**Current Interconnect Technologies**

Reduced resistivity and dielectric constant results in improvement in performance.
**Carbon Nanotubes**

1-D conductors:
- Quantum Wires:
  - Very limited phase space for scattering.
  - Mean free paths as large as 1.6 µm.
  - Lower resistivity

3-D conductors:
- Conventional metal wires:
  - Backscattering through a series of small angle scatterings.
  - Mean free paths ~ 30nm.
  - Higher resistivity

Potential Candidates for GSI Interconnects.

**Can Optical Interconnects help?**

On-Chip Optical Interconnects
- For Clock Distribution
  - Signal wires
    - Reduce delay
    - Increase bandwidth
  - Clock distribution
    - Reduce jitter and skew
  - I/O with very high bandwidth
  - Reduce power

Chip-to-chip Optical Interconnects
- incoming short laser pulse
- modulator chip
- grating
- fiber
- receiver chip
Summary: Technology Progression

Bulk CMOS

- Cu interconnect
- Low-k ILD

Double-Gate CMOS

- Metal gate
- High k gate dielectric

Strained Si Ge channel

FD SOI CMOS

- Wafer bonding
- Crystallization

3D, heterogeneous integration

- Optical interconnect
- Detectors, lasers, QWM, waveguides

Self-assembly

- Interconnects and contacts for nanodevices

Nanotechnology

- Nanotube
- Molecular devices

Feature Size

- 100 nm

- 2 nm