EE 410: Integrated Circuit Fabrication Laboratory

Web Site:  [http://www.stanford.edu/class/ee410](http://www.stanford.edu/class/ee410)

[https://ccnet.stanford.edu/ee410/](https://ccnet.stanford.edu/ee410/) (on CCNET)

Instructor: Prof. Krishna Saraswat; CISX 326; 725-3710; saraswat@stanford
Office Hours: Monday 4-5 pm. Friday, 2 3 PM; or by appointment

Secretary: Gail Chun-Creech; CISX 329; 723-0983; CREECH@snow.stanford.edu

TAs: TBD

Lecture: ~ 6 meetings, dates and times to be announced on the web

Lab: 4 hours of laboratory work per week by arrangement

Text: None. Extensive notes will be provided.

References: Books related to EE212 and 216 (see the web page)
Course Outline:

• Specifically the course is divided in three parts:
  • Silicon gate CMOS fabrication (Group activity)
  • Process simulation using TSUPREM (Individual activity)
  • Device testing and characterization (Group activity)

• Emphasis is on the practical aspects of IC fabrication, including silicon wafer cleaning, photolithography, etching, oxidation, diffusion, ion implantation, chemical vapor deposition, physical sputtering and electrical device testing.

• Prerequisite: EE212 and EE216 or equivalent required. Course has limited enrollment capacity. Preference will be given to the students who are planning to use the IC Lab facility for their PhD research.

• Credit: 4 units for CMOS (3 units option possible if you have limits on units). Letter grade only.

CMOS Fabrication

• For group activity the course is divided into 4 groups
• Each group is led by a TA
• TA will give you demonstration of the fabrication equipment and process
• You will participate in processing under the supervision of the TA
• On your own you won’t be able to enter the fab and do anything
### EE 410 - Winter 2010-11

**PLEASE PRINT IN BLOCK LETTERS**

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<th>NAME (LAST, FIRST)</th>
<th>Prerequisites or equivalent</th>
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Earliest time I can take class in: ____________________________

Is safety class done?

Lab Performance judged by the TA  25%
Process and Device Modeling Paper  25%
Group Report  50%
What's on the EE410 chip?

The CMOS-LOCOS wafer contains 80 dice, each die measuring 8.3mm x 8.3mm.
1. Fabrication Test Structures — checked during processing
2. Device Test Structures — MOSFET's, parasitic MOS & BJTs, capacitors, diodes
3. Process Test Structures — sheet resistance, contacts, continuity, isolation
4. Circuit Test Structures — CMOS inverters
5. Research Test Structures (Not used in EE410)
General Features of the EE410 Process

- 7 mask levels
- 0.45µm minimum dimensions
- 540nm field oxide LOCOS isolation
- 10nm gate oxide
- p+ poly-Si gate for PMOS transistors and n+ poly-Si for NMOS transistors
- single mask n+ and p+ source/drain definition (no LDD)
- single level of aluminum/silicon metallization
- phosphosilicate glass (PSG) passivation
- non-silicided contacts (high metal contact resistance to poly and active regions)

Process and Device Modeling Paper
(Submitted by each student: Individual effort)

Simulations (by TSUPREM, etc.) and calculations of the structures (e.g. thickness, doping profile, ..........) and electrical parameters (e.g. sheet resistance, threshold voltage, ..........) that should result from the process flow you are following in the Lab.

Contents: Less than 10 pages of main body. It should be written similar to a paper published in a Journal. Any supporting material should go in an appendix.

Schedule 1 copy of the paper will be due on 2/7/2010

Grading Completeness of information 10%
Quality of presentation 10%
Innovations and others 5%

Check details on the report format etc. on the web page
Process and Device Modeling Paper Format

I) Introduction
Include a short overview of the process including major steps, the structure and the scope of the study.

II) Analytical calculations (by hand)
   a) Field and gate oxide thicknesses
   b) Ion implant profiles
   c) Junction depths
   d) Sheet resistance of junctions and poly-Si gate
   e) Threshold voltages

III) SUPREM Simulations on the same topics as in II)

IV) Comparison and Discussion
A table showing SUPREM values and hand calculated values and a discussion on discrepancies.

V) Conclusion

VI) References

Electrical Testing

- Testing will be a group activity
- TA will give you demonstration of the testing equipment and procedures
- You will be on your own for remainder of the testing activity
Group Lab Report

- Written as a group report. It may be divided up into chapters and each chapter written by a designated member of the group.
- Please indicate on the report specific contributions of the individuals.
- Contents: The style of the report should be similar to a PhD thesis (but not as long). It should include at least the following chapters:
  1. A discussion of the process flow used, including the reasons for each step, problems encountered and solutions adopted.
  2. Simulations (by SUPREM, PISCES, etc.) and calculations of the structures (e.g. thickness, doping profile ...........) and electrical parameters (e.g. sheet resistance, threshold voltage ...........) that should result from the process flow (Similar to the Process and Device Modeling Paper).
  3. Methodology and results of measurements taken on test structures, devices and circuits
  4. Comparison of (2) and (3) and explanations of all discrepancies.
  5. Conclusions and comments.
  6. References

Schedule: One copy of the final report will be due on 3/14/2010. (The report will be kept for record)

Grading:
- Completeness of information 25%
- Quality of presentation 20%
- Innovations and others 5%

Pledge: If needed you will be available to TA the course in future
EE 410 - Lectures

6 meetings will take place through the quarter.

1. "Course organization meeting" – 1/6/2009, 12:00 - 1:00 PM, CISX 101
2. "Safety tour" Friday, January 8, 12:00 noon, meet outside CISX 101
3. "Cleaning and clean Processing Techniques"
4. "Process simulation using TSUPREM"
5. "Description of the test structures in EE410 mask sets"
6. "Comparison of EE410 and industry standard CMOS processes"

Place, Date and time to be announced on the web for the remaining lectures

Safety Training

- Please sign the information sheet.
- To gain access to the lab, you must be a current lab member (if so, provide your Coral login on the sheet), or complete the SNF Intro & Safety course.
- If you need to complete the Intro & Safety course, you must do the following:
  - Check all the times that you are available for lab tours on Friday. There is a limit of 8 people per tour session and we would like to have at least 4 people in a session.
  - Lab Orientation & Safety, Part I or http://spf.stanford.edu/training/safetyone.wmv
  - Lab Orientation & Safety, Part II or http://spf.stanford.edu/training/safetytwo.wmv
  - Gowning or http://spf.stanford.edu/training/gowning.wmv
Safety Training

- Read both lab manuals, available at [http://snf.stanford.edu/labmembers](http://snf.stanford.edu/labmembers). The manuals are:

- Take the SNF lab safety test. You are encouraged to work together and discuss how to best answer the questions.

- Take the [SNF Ethics Survey](http://www.surveymonkey.com/s/WLMZ7LQ). This is requirement of the NSF NNIN program at SNF.

- Sign the Safety Acknowledgement Form.

**Without safety training you won't be allowed to work in the SNF fab and thus won't be able to take this course**

*Good luck and have fun!!*