Fabrication of samples for scanning probe experiments on quantum spin Hall effect in HgTe quantum wells

M. Baenninger, M. König, A. G. F. Garcia, M. Mühlbauer, C. Ames et al.

Citation: J. Appl. Phys. 112, 103713 (2012); doi: 10.1063/1.4767362
View online: http://dx.doi.org/10.1063/1.4767362
View Table of Contents: http://jap.aip.org/resource/1/JAPIAU/v112/i10
Published by the American Institute of Physics.

Related Articles
Light emission from InGaAs:Bi/GaAs quantum wells at 1.3 μm
AIP Advances 2, 042158 (2012)

Polarization spectroscopy of N-polar AlGaN/GaN multi quantum wells grown on vicinal (000) GaN

Temperature dependent band offsets in PbSe/PbEuSe quantum well heterostructures

Universal behavior of photoluminescence in GaN-based quantum wells under hydrostatic pressure governed by built-in electric field

Effects of scattering on two-dimensional electron gases in InGaAs/InAlAs quantum wells

Additional information on J. Appl. Phys.
Journal Homepage: http://jap.aip.org/
Journal Information: http://jap.aip.org/about/about_the_journal
Top downloads: http://jap.aip.org/features/most_downloaded
Information for Authors: http://jap.aip.org/authors
Fabrication of samples for scanning probe experiments on quantum spin Hall effect in HgTe quantum wells

M. Baenninger,1 M. König,1 A. G. F. Garcia,1 M. Mühlbauer,2 C. Ames,2 P. Leubner,2 C. Brüne,3 H. Buhmann,2 L. W. Molenkamp,3 and D. Goldhaber-Gordon1
1Department of Physics, Stanford University, Stanford, California 94305, USA
2Physikalisches Institut (EP3) and Röntgen Center for Complex Material Systems, Universität Würzburg, Am Hubland, 97074 Würzburg, Germany

(Received 8 September 2012; accepted 26 October 2012; published online 28 November 2012)

We present a fabrication process for devices on HgTe quantum wells through which the quantum spin Hall regime can be reached without the use of a top-gate electrode. We demonstrate that a nominally undoped HgTe quantum well can be tuned from p-type to n-type, crossing through the quantum spin Hall regime, using only a back-gate hundreds of microns away. Such structures will enable scanning probe investigations of the quantum spin Hall effect that would not be possible in the presence of a gate electrode on the surface of the wafer. All processes are kept below 80 °C to avoid degradation of the heat-sensitive HgTe quantum wells. © 2012 American Institute of Physics. [http://dx.doi.org/10.1063/1.4767362]

INTRODUCTION

The quantum spin Hall (QSH) effect has attracted a lot of attention in the condensed matter community since its theoretical prediction1–3 and experimental demonstration4 soon after. One of the most intriguing predictions for the QSH effect is that ballistic transport should occur in edge states even at zero magnetic field. While there has been convincing indirect evidence that this is, indeed, the case,4,5 there has been no direct imaging of the current flow along the edges. Scanning probe microscopy (SPM) experiments such as scanning gate microscopy,6 scanning SQUID microscopy,7 or microwave impedance microscopy8 could not only provide direct evidence of the quantum spin Hall edge states but also probe various aspects of the helical edge states on a local scale. However, all QSH experiments to date have been carried out in n-doped wafers, where the QSH regime was only reached by depleting the bulk carriers in the quantum well with a top-gate electrode. This approach is not practical for most scanning probe experiments since the metal on the surface would screen the interactions between the probe and the quantum well. In this communication, we describe a method for fabricating devices suitable to study the QSH effect with scanning probes.

FABRICATION

Fabricating microstructures on HgTe/HgCdTe quantum wells pose substantial challenges: The heterostructures are very sensitive to heat and need to be kept at T ≤ 80 °C at all times during processing to avoid interdiffusion of well and barrier materials.9 This makes it impossible to use many standard processes for optical and electron beam lithography, where the resist usually has to be baked at T > 80 °C. Other challenges include the softness of the material, which makes wirebonding and general handling difficult, and the reactivity of HgTe/HgCdTe with other materials.10 In the following paragraphs, we describe a low-temperature fabrication process for microstructures on HgTe quantum wells using optical lithography.

We start with heterostructures grown by molecular beam epitaxy on a (100) Cd0.96Zn0.04Te (below referred to as CdZnTe) or CdTe substrate.11,12 The layer structure bottom up consists of a CdTe buffer, a Hg0.3Cd0.7Te (below referred to as HgCdTe) layer followed by a thin HgTe layer (the quantum well), and finally a HgCdTe cap of 15–100 nm. The band structure is normal for quantum well widths dQW < 6.3 nm but inverted for dQW > 6.3 nm and, therefore, appropriate for the quantum spin Hall effect.4 Iodine doping can be introduced on either side of the quantum well, but this paper focuses on undoped wafers. The first step in fabrication of a HgTe quantum well device from a wafer is to define a mesa. There are few wet etchants for HgTe/HgCdTe, and the commonly used Br2 in ethylene glycol is problematic due to its toxicity and its isotropic etch behavior that tends to undercut the etch mask and make a reproducible process difficult.9 Therefore, we used Ar ion milling. While undercut does not generally occur in ion mill patterning, one commonly encountered problem is side wall re-deposition along the edge of a mesa. In scanning probe experiments, the resulting “fences” which protrude above the mesa edge (see Figs. 1(c) and 1(d)) can affect the coupling of the scanning probe to the quantum well, leading to measurement artifacts, and can also cause the probe to crash. This may require a larger separation of the probe from the device, limiting sensitivity and resolution. We developed an ion milling process that avoids this problem by etching at an optimized angle on a rotating stage as described below. The patterning is done with optical lithography, using the photore sist as an etch mask. We spin Shipley 3612 at 5500 rpm, bake it for 2 min on an 80°C hotplate, then expose it for 5 s at a UV intensity of 10 mW/cm2 and develop in Microposit CD-30 developer for 30 s. The ion milling is done at a beam voltage Vb = 150 V and intensity Jb = 0.1 mA/cm2 at an angle θ = 20° off the normal on a stage rotating at 30 rpm. The samples are mounted with a thermally conductive silver paste to the stage that is cooled to Tstage = 5°C to avoid overheating. After etching, the photore sist is removed in hot acetone (50°C) and ultrasonic bath.
The ion mill settings were optimized to get a highly reproducible etch rate of 7–8 nm/min and minimal fencing, as shown in Figs. 1(a) and 1(b) in atomic force microscope (AFM) and scanning electron microscope (SEM) images, respectively. In contrast, Figs. 1(c) and 1(d) show the strong buildup along the mesa edge typical for non-optimum settings.

The next step is the fabrication of ohmic contacts to the quantum well layer. The optical lithography is done in the same way as described above. For shallow quantum wells (≤30 nm below the surface), a sequence of 50 nm AuGe eutectic (88:12 wt. %), 5 nm Ti, and 50 nm Au is evaporated directly after the photolithography, in an electron beam evaporator (base pressure <5 × 10⁻⁷ Torr) with liquid nitrogen cooled stage (−30°C ≤ Tstage ≤ −10°C) followed by a lift-off in hot acetone and a short time in the ultrasonic bath. For deeper quantum wells, an ion milling step is added after the lithography to locally reduce the cap layer thickness to <30 nm. After that, the same metallization and lift-off are carried out. No annealing step is required in this process to achieve a good ohmic contact (RContact ≤ 500 Ω) to the quantum well. An alternative way of fabricating patterned ohmic contacts is to thermally evaporate 50 nm of indium followed by 50 nm of gold. In this process, quantum wells as deep as 40 nm have been contacted without etching or annealing, but it is difficult to wirebond to the contacts as described below.

Although the main focus of this article is on devices without top-gate electrode, we also include the description of a process for fabricating top-gates. Top-gated devices can be used for a wide range of experiments without scanning probe but also for certain scanning probes that do not couple electrically such as scanning SQUID microscopy. HgCdTe does not generally build a good Schottky barrier with metals, therefore, a gate insulator is required between the wafer surface and the metal. We use low temperature atomic layer deposition (ALD) of Al₂O₃ as gate dielectric, where we reduce the chamber temperature to 60°C from the usual 110–120°C but increase the exposure times from 0 to 5 s and pump times from 5 s to 30–50 s. An Al₂O₃ layer of ≈40 nm was found to withstand several volts on the topgate. This gate dielectric is only about one third of the thickness used in previously reported Si-O-N insulator layers. Optical lithography for the topgate is done with the same process as described above. It is important to use a passivated developer such as Microposit CD-30 that does not strongly etch the Al₂O₃ (CD-26 is in fact a convenient etchant for Al₂O₃). As an extra precaution, care is taken not to overdevelop the resist and the devices are rinsed extensively in DI water after developing, in order to avoid extended exposure of the Al₂O₃ to the developer. Metallization of 20 nm/100 nm Ti/Au is done in an e-beam evaporator with liquid nitrogen cooled stage (−30°C ≤ Tstage ≤ −10°C) followed by a lift-off in hot acetone.

The devices are mounted onto a chip carrier with GE-varnish or silver paint. Wirebonding to the contacts can be difficult on HgTe/HgCdTe heterostructures. While AuGe/Ti/Au ohmics can be bonded to with a wedge bonder, although with reduced power, this does not work for In/Au ohmics or Ti/Au gate contacts, due to the softness of the HgCdTe and poor adhesion of the metal. For those contacts, a different method is used, where a wire is bonded on the chip carrier with the wedge bonder, but the second bond is placed on the chip with zero ultrasound power, which cuts the wire without damaging the surface of the device. A 200 μm diameter indium dot is then placed on the contact with a tweezers tip and the wire end is squeezed manually into the indium. This technique leads to a mechanically robust and electrically reliable contact that survives multiple thermal cycles to 4K. The spacing between contacts needs to be larger than with normal wirebonding, but contacts at a 500 μm pitch can be bonded quite comfortably after some practice.

RESULTS

We now present experimental results that demonstrate that nominally undoped HgTe quantum wells can be tuned from p-type to n-type with only a backgate, thereby crossing the quantum spin Hall regime in the case of inverted
band structure. Devices used in these experiments were 50 μm × 30 μm HgTe Hall bars as shown in an optical microscope image in Fig. 2(a), fabricated with the process described above but without a topgate electrode. The device used here was made from a wafer with a 7 nm HgTe quantum well below a 50 nm HgCdTe cap. It was glued with a thin layer of GE-varnish onto the metallic surface of a chip carrier, which acted as a backgate electrode, separated from the quantum well by about 800 μm of CdTe substrate. Transport measurements were carried out with the sample immersed in liquid helium at 4.2 K with standard lock-in techniques. Fig. 2(b) shows the 4-probe longitudinal resistance as a function of backgate voltage. There is a clear maximum with resistance of 100–120 kΩ at V_{bg} = 0–50 V, which indicates that the device can be tuned from p-type at large negative V_{bg} through the QSH regime to n-type at large positive V_{bg}. Our gate sweeps show a quite strong hysteresis but after a slight shift between the first and second loops, subsequent hysteresis loops were very reproducible in their overall shape. However, there are fluctuations of about 10% of the resistance, which are not reproducible. These fluctuations can be reduced by sweeping very slowly, and they completely disappear when the backgate is kept at a fixed voltage. We attribute the fluctuations to charging events at one of the layer interfaces between the backgate and the quantum well. Interface charging can also explain the hysteresis and the weakening of the backgate effect observed in several devices when applying |V_{bg}| > 200 V (not shown). While the appearance of a resistance maximum as a function of backgate voltage indicates tuning from p- to n-type, Hall measurements give unequivocal evidence of a change in the sign of the charge carriers. Figs. 2(c) and 2(d) show the low field longitudinal and transverse magnetoresistance at V_{bg} = ±210 V, respectively. The negative slope in the Hall resistance at V_{bg} = −210 V shows that the charge carriers are positive, i.e., holes, whereas the positive slope at V_{bg} = 210 V shows that the carriers are electrons. The extracted densities of p ≈ 6 × 10^{10} cm^{-2} at V_{bg} = −210 V and n ≈ 5 × 10^{10} cm^{-2} at V_{bg} = 210 V are consistent with the location of the resistance maximum at slightly positive backgate voltage although the total change in density is almost a factor of 4 larger than expected from the capacitor model discussed below. We believe that the extracted densities are substantially higher than the real density. A systematic overestimate of the density determined from the slope of

FIG. 2. Demonstration of QSH effect with backgate: (a) Optical micrograph of a typical Hall bar device with ohmic contacts. (b) Longitudinal resistance as a function of backgate voltage measured at 4 K in a 4-probe measurement configuration. A maximum with finite resistance R_{max} = 100–120 kΩ indicates that the device can be tuned through the QSH regime. (c) and (d) Longitudinal and transverse low field magnetoresistance at V_{bg} = ±210 V. The change in sign of the Hall slope demonstrates a change from p-type to n-type and, therefore, tuning through the gap. (e) and (f) The clear non-local resistance for two different configurations provides very strong evidence of edge state transport at V_{bg} ≈ 0 and therefore the QSH regime.
the Hall resistance can be explained by the onset of localization effects in the low-density regime. The non-linear feature in $R_{xy}$ at $-0.1 \text{ T} < B < 0.1 \text{ T}$ for $V_{bg} = -210 \text{ V}$ can be explained by the coexistence of two types of holes with different masses and mobilities, which can occur near the transition from a direct to indirect bandgap material. Indeed, with a nominal quantum well thickness of 7 nm our device is very close to the transition from direct to indirect bandgap, which is expected to occur at a thickness of 7.2–7.3 nm. The finite resistivity in the bulk gap when sweeping from p- to n-type is a unique feature of the QSH effect, and the resistance of the order of 100 kΩ is consistent with the previously reported experimental observation that a roughly quantized resistance of $\hbar/2e^2 = 12.9 \text{ kΩ} \pm 10\%$ in the QSH regime is only observed for devices with dimensions up to a few microns, while the resistance is higher in devices with larger dimensions. We observed a similar resistance maximum for several backgated as well as top-gated devices with an inverted band structure ($d_{QW} > 6.3$ nm). Conversely, devices with the same dimensions but a regular band structure ($d_{QW} < 6.3$ nm) showed at least two orders of magnitude higher resistance. Apart from the finite longitudinal resistance in the gap, we investigated another unique feature of the quantum spin Hall regime: the presence of edge states necessarily leads to non-local transport that can be detected in a 4-probe measurement setup. For example, in a setup where a current $I_{16}$ is applied between contacts 1 and 6 as indicated in Fig. 2(a), that current not only flows in the most direct way between those contacts but also along the long path defined by edge states across contacts 2–5. This leads to a measurable voltage drop $V_{ij}$ between any pair of these contacts, which can be calculated using the Landauer-Büttiker formalism. If we define $R_{pqij} = V_{ij}/I_{pq}$, the prediction in the perfectly ballistic case is $R_{16,23} = R_{16,34} = R_{16,45} = h/6e^2 \approx 4.3 \text{ kΩ}$. In Figs. 2(c) and 2(f), we show $R_{16,45}$ and $R_{16,23}$ as a function of backgate voltage. At the extremes of backgate voltage $V_{bg} = \pm 210 \text{ V}$, far away from the QSH regime, the measured resistances are low, but around $V_{bg} = 0$ there is a very clear non-local signal that indicates the presence of edge states. It is not surprising that the measured resistances deviate from the predicted values since the device is clearly not in the ballistic regime as demonstrated by the large longitudinal resistance. The reduced resistance $R_{16,45} \approx 3.5 \text{ kΩ}$ can be explained if the current along the long path is smaller than predicted. On the other hand, if one segment is much more resistive than the other one, the measured voltage could be higher than predicted even if the current is lower. This might explain the high value of $R_{16,23} \approx 25 \text{ kΩ}$. Even with the relatively strong deviation from the theoretical value, the clear non-local resistance observed is a very strong indication of edge state transport. Overall, our presented results clearly demonstrate that the QSH regime can be reached in this device without a topgate.

**OUTLOOK: SUBSTRATE THINNING**

We found experimentally that a backgate voltage change from $-200 \text{ V}$ to $+200 \text{ V}$ across an $800 \mu\text{m}$ thick CdTe substrate only changes the density by $\Delta n \leq 5 \times 10^{10} \text{ cm}^{-2}$. The substrate breaks down under a voltage of $\approx 450 \text{ V}$, but the density saturates at lower voltages so that for $|V_{bg}| > 200 \text{ V},$ the achieved density change is substantially reduced. This means that as-grown density of the wafer needs to be $\leq 2.5 \times 10^{10} \text{ cm}^{-2}$ for the QSH regime to be reachable with the backgate. Unfortunately, nominally undoped HgTe quantum wells tend to be p-type, sometimes substantially ($p > 10^{11} \text{ cm}^{-2}$) depending on growth conditions, most likely due to Hg vacancies in the HgCdTe. This limits the wafers that are suitable for scanning probe investigations of the QSH effect. In order to increase the density range that can be accessed with a backgate, we investigated thinning of the substrate to bring the backgate closer to the quantum well. The fabrication process for thinned-substrate devices is as follows: First, a regular device is fabricated with the process described above. The device is glued face down onto a glass slide with superglue and then mechanically lapped from the back to a thickness of about 100 µm. After thinning, the glue is dissolved in hot acetone and the device is flipped over and transferred to a new substrate: a silicon chip slightly larger than the HgTe device, on which Ti/Au was evaporated followed by deposition of 2000 cycles of ALD Al2O3 ($\approx 200$ nm). The Ti/Au serves as a backgate electrode and the thick Al2O3 layer is required as a strong insulator that allows application of $>200 \text{ V}$ to the backgate even though the $100 \mu\text{m}$ CdTe substrate would break down at much lower voltages. The thinned device is glued onto the prepared substrate with a thin layer ($\lesssim 1 \mu\text{m}$) of PMMA and then both are mounted on a chip carrier. A schematic diagram of a thinned device mounted on a backgate/substrate is shown in Fig. 3(a), and an optical micrograph of a thinned, mounted Hall bar device is shown in Fig. 3(b).

Fig. 3(c) compares the density dependence on backgate voltage for a normal and a thinned device, where the densities were obtained from the low field Hall resistance. The two devices discussed here were made from two different, nominally undoped wafers, with a $25 \text{ nm}$ HgCdTe cap layer and QW thickness of $8 \text{ nm}$ (thinned device) and $7 \text{ nm}$ (unthinned device), respectively. The blue data in Fig. 3(c) show a typical gating behavior of an unthinned device with a relatively high as-grown p-type density. A simple plate capacitor model predicts the relation between $V_{bg}$ and charge density to be $p = C_0(V_{bg} - V_0)$ with $C_0 = \varepsilon_0\varepsilon/\text{ed}$, where $\varepsilon_0\varepsilon$ are the dielectric constants, $\varepsilon$ is the electron charge, and $d$ is the separation between the backgate and the quantum well. With $\varepsilon(\text{CdTe}) \approx 10.2$ (Ref. 16) and $d \approx 800 \mu\text{m}$, the predicted $C_0 \approx 7 \times 10^4 \text{ V}^{-1}\text{cm}^{-2}$ is smaller than the slope $C \approx 1.1 \times 10^8 \text{ V}^{-1}\text{cm}^{-2}$ obtained from a linear fit to the data. We consistently found that the experimental $C$ was larger than the theoretical $C_0$ with the deviation varying from 30% to 70%. A systematic error in the measured density as discussed above can be ruled out since the data were taken in the higher density regime, where the Hall slope gives reliable density values. We do not have a good explanation for this deviation from the theoretical model at this point. The red data in Fig. 3(c) show the backgate characteristics for a device that was thinned to about $100 \mu\text{m}$. Here, the slope is $C \approx 5.4 \times 10^8 \text{ V}^{-1}\text{cm}^{-2}$, almost a factor of 5 higher than for the typical unthinned device. The total measured change in density $\Delta p \approx 1.98 \times 10^{11} \text{ cm}^{-2}$ is about 4.5 times more than $\Delta p \approx 4.43 \times 10^{10} \text{ cm}^{-2}$ in the unthinned device.
effective $\Delta p$ in the thinned device might even be a bit larger, since the density point at $V_{bg} = 210$ V is not reliable due to the systematic error near the localization transition and this point was excluded from the linear fit. Indeed, the Hall resistance shows a zero field offset that is not expected for the Hall effect in the metallic regime (not shown) and the longitudinal resistivity shown in Fig. 3(d) is larger than $h/e^2$ indicating the transition to the localized regime. Further support that the density does not really saturate comes from the dependence of resistance on gate voltage shown in Fig. 3(d), which continues to increase up to $V_{bg} = 210$ V without any sign of saturation. The resistance trace is stable and only shows a weak hysteresis, confirming the good quality of the backgate. The CdZnTe substrates are very brittle and prone to breaking apart during thinning. For a successful thinning, the device needs to be attached to the glass slide very well beforegate. The CdZnTe substrates are very brittle and prone to breaking apart during thinning. More work is required to improve the yield substantially with these steps but a risk remained that the device could be damaged during thinning as can be seen for the chip in Fig. 3(b), where parts of the device broke off starting from cracks at the edge. We found that it is very important that the thinned chips have very clean edges, otherwise the device starts to break off starting from cracks at the edge. We managed to improve the yield substantially with these steps but a risk remained that the device could be damaged during thinning as can be seen for the chip in Fig. 3(b), where parts of the device broke off during thinning. More work is required to improve the yield but our results demonstrate the potential that substrate thinning has to improve the backgate efficiency.

CONCLUSION

We have presented a low-temperature process for fabrication of microstructures on HgTe quantum well wafers. We demonstrate that for quantum wells with low as-grown density, the quantum wells can be tuned into the quantum spin Hall regime without a topgate, opening up a path to a wide range of scanning probe experiments. We also show that thinning of the wafer substrate can increase the density change achievable with a backgate several times, potentially allowing higher as-grown density wafers to be tuned into the QSH regime.

ACKNOWLEDGMENTS

The process development for fabrication of devices suitable for scanning probe experiments was supported by the NSF Center for Probing the Nanoscale under Grant No. PHY-0830228. Characterization of undoped wafers and demonstration of QSH in backgated devices were supported by the DARPA Meso project under Grant No. N66001-11-1-4105. Part of this work was performed at the Stanford Nano Center (SNC) part of the Stanford Nano Shared Facilities. The mechanical substrate thinning was carried out by the Ginzton Crystal Shop at Stanford. We thank Adam Sciambi for advice on substrate thinning and indium bonding, and Reyes Calvo, Katja Nowack and Eric Spanton for useful discussions.


14See supplementary material at http://dx.doi.org/10.1063/1.4767362 for details on Hall resistance in the localized regime; for band structure calculations.