Hydrogen-terminated diamond FET and GaN HEMT delivering CMOS inverter operation at high-temperature

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Introduction: An increasing number of applications in power electronics, sensor signal conditioning, and RF communication are demanded to operate beyond 200°C (e.g., engine and geothermal wellbore monitoring). These applications require integrated circuits such as mixed-signal circuits featuring analog circuitry, analog to digital converters as well as embedded microcontrollers and on-chip memories. The Si-based complementary metal-oxide-semiconductor (CMOS) technology combining a P-type MOS (PMOS) and N-type MOS (NMOS) to achieve different logic functions is not reliable for stable and sustained operations at high temperatures (>125 °C) [1]. In this work, we report the successful development of a CMOS building block using wide bandgap (WBG) technology that demonstrated operations up to >350 °C. The CMOS was developed using two wide bandgap material systems known for their high-temperature capability: diamond and gallium nitride (GaN). The "PMOS" utilizes a hole channel FET achieved using a hydrogen-terminated diamond field-effect transistor (diamond FET) and the "NMOS" is made out of an electron channel GaN high electron mobility transistor (GaN HEMT) as shown in Figure 1.

Device Fabrication: The PMOS formed by the hydrogen-terminated diamond FET, which was fabricated from the type-IIa <100> CVD single-crystalline diamond substrates. The Figure 2 illustrated the formation of conductive two-dimensional hole gas (2DHG) in diamond subsurface [2], which achieved by hydrogen plasma treatment (30 min @ 800 °C) in the microwave plasma-assisted CVD (MPCVD). Following the device fabrication process as shown in Figure 3, the device isolation was achieved by reactive-ion etching (RIE) oxygen plasma (5 min @ 200 W). A 20 nm thick Ti first deposited on the isolation area followed by a larger Au ohmic layer on the top, which overlapped on the conductive channel shown in Figure 3(d). Then an Al_2O_3 dielectric (25 nm) passivation was deposited with atomic layer deposition (ALD) at low temperature (200 °C). Finally, an Al/Au metal gate was deposited on the top of the dielectric. For the NMOS, the enhancement-mode GaN HEMTs were fabricated from AlGaN/GaN epi layer on the sapphire substrate. The normally off channel was achieved by appropriate amount of etching of AlGaN under the gate.

Results: Both diamond FET and GaN HEMT were first tested independently to record their performance as a function of different gate biases. The threshold voltages recorded were 0 V for the diamond based PMOS and +1.5 V for the GaN based NMOS, respectively. For the diamond FET, the Hall mobility and carrier concentration were measured at 48 cm^2/Vs and 5×10^{13} cm^{-2} respectively. The Al_2O_3 passivation of diamond FET preserved the diamond surface preventing any remarkable current loss up to 350 °C as shown in Figure 4(b). To form a CMOS inverter, the diamond FET (PMOS) and GaN HEMT (NMOS) were wire-bonded as demonstrated in Figure 5. The input of the CMOS V_{in} was selected based on the independent threshold voltages of PMOS and NMOS. By voltage sweeping the V_{in}, the output V_{out} of the CMOS inverter was recorded in a Voltage Transfer Characteristics (VTC) diagram as V_{out} vs V_{in}. At room-temperature, the CMOS VTC reached the high-state completely as biased at different V_{dd} (from +3 to +7 V) and reached the low-state as grounded (at 0 V), as shown in Figure 6(a). At high temperatures (up to 350 °C), the VTC was also achieved as expected, as shown in Figure 6(b). In the meanwhile, the switching performance at a high temperature of 275 °C was measured by an oscilloscope as shown in Figure 7.

Significance: This work first-time demonstrated the prospect of diamond-GaN CMOS technology as an excellent solution for high-temperature (>350 °C) applications. Furthermore, the integrated diamond-GaN CMOS logic gates such as NAND and NOR on the same substrate are expected in the future.

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References: [1] Edwards C, *Engineering & Technology, IET*, 2008. [2] H. Kawarada, *Japanese Journal of Applied Physics*, 2012.

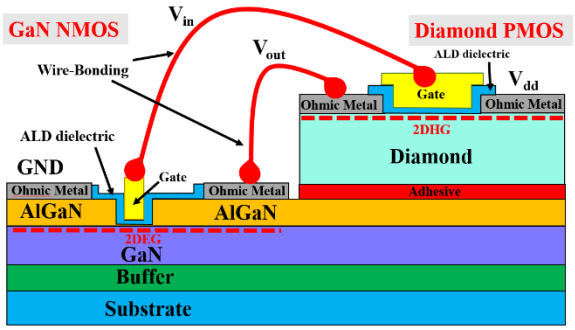

Figure 1. The schematic diagram of the wire-bonded CMOS inverter.

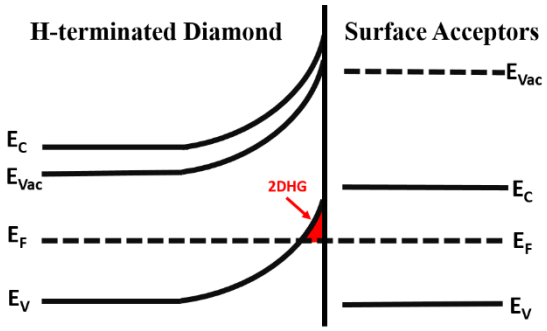

Figure 2. Formation of conductive two-dimensional hole gas (2DHG) in H-terminated diamond subsurface.

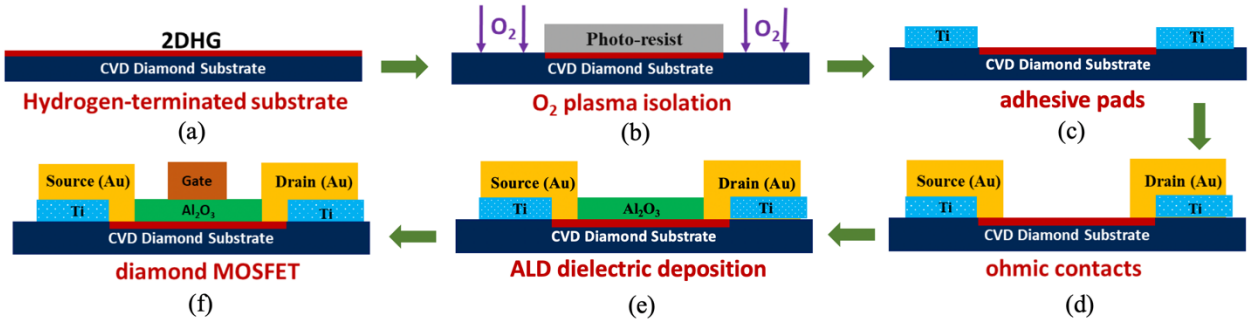

Figure 3. The schematic diagram of the diamond FET fabrication process: (a) Hydrogen-terminated diamond substrate. (b) Device isolation using RIE O_2 plasma. (c) Ti adhesive pads deposition. (d) Au deposition for the source and drain ohmic contacts. (e) Al_2O_3 dielectric passivation deposition. (f) Al/Au gate deposition

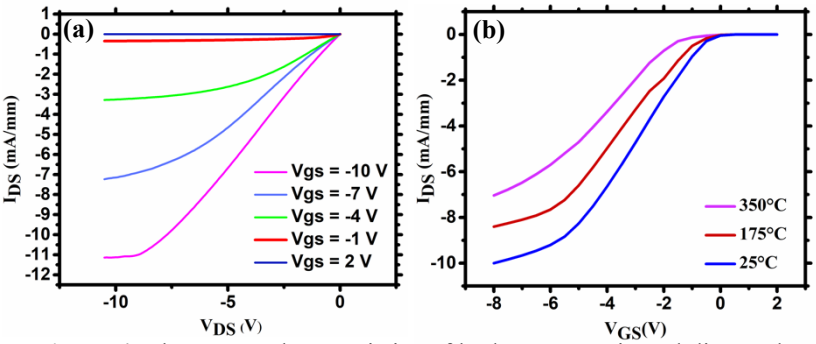

Figure 4. The output characteristics of hydrogen-terminated diamond FET (a) I_{DS} vs V_{DS} at room temperature. (b) I_{DS} vs V_{GS} at different temperatures.

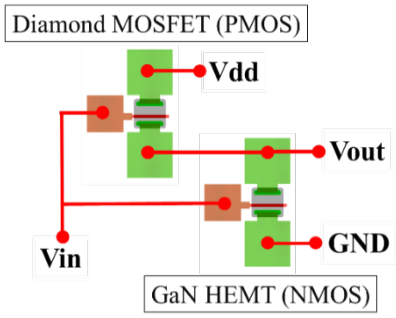

Figure 5. The schematic diagram of the wire-bonded CMOS inverter.

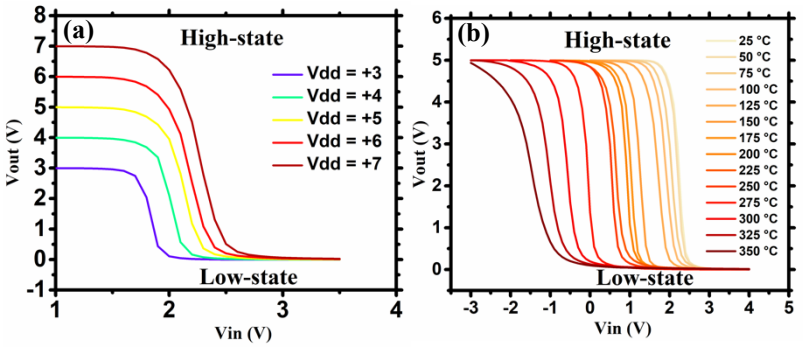

Figure 6. The Voltage Transfer Characteristics (VTC) diagrams of diamond FET and GaN HEMT inverter. (a) Inverter performance at Vdd = +3 to +7 V at room temperature. (b) Inverter performance at Vdd = +5V from 25 to 350 °C.

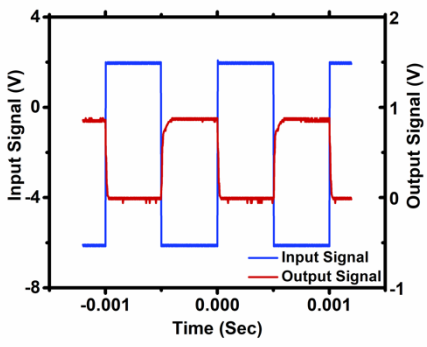

Figure 7. The switching output of the CMOS inverter with the input signal of 1kHz at 275°C.