Synchrony in Silicon: The Gamma Rhythm

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***Abstract*—In this paper, we present a network of silicon interneurons that synchronize in the gamma frequency range (20–80 Hz). The gamma rhythm strongly influences neuronal spike timing within many brain regions, potentially playing a crucial role in computation. Yet it has largely been ignored in neuromorphic systems, which use mixed analog and digital circuits to model neurobiology in silicon. Our neurons synchronize by using shunting inhibition (conductance based) with a synaptic rise time. Synaptic rise time promotes synchrony by delaying the effect of inhibition, providing an opportune period for interneurons to spike together. Shunting inhibition, through its voltage dependence, inhibits interneurons that spike out of phase more strongly (delaying the spike further), pushing them into phase (in the next cycle). We characterize the interneuron, which consists of soma (cell body) and synapse circuits, fabricated in a 0.25-μm complementary metal–oxide–semiconductor (CMOS). Further, we show that synchronized interneurons (population of 256) spike with a period that is proportional to the synaptic rise time. We use these interneurons to entrain model excitatory principal neurons and to implement a form of object binding.**

***Index Terms*—Binding, conductance-based neuron circuit, delay model of synchrony, inhibitory interneuron, neuromorphic engineering, shunting inhibition, synaptic rise time.**

I. Gamma Synchronization

NEUROMORPHIC engineering aims to reproduce the spike-based computation of the brain by morphing its anatomy and physiology into custom silicon chips. Using mixed analog and digital circuits enables engineers to build dense integrated networks of silicon neurons that run in real time. But this performance comes at a price: A fixed silicon area can accommodate a few large neurons that express little variation or many small neurons that express great variation. This tradeoff between resources and variance is fundamental to physical systems including neurobiological ones, which employ large neuron populations and tolerate variance. Modeling neural systems in hardware provides a means to explore and exploit tactics used by biology to manage this tradeoff and build robust computing systems.

Having successfully implemented models of sensory regions (such as the retina [1], [2] and the cochlea [3], [4]), the current trend in neuromorphic engineering is to implement models of cortical regions [5], [6]. However, certain aspects of cortex remain largely ignored, such as the ubiquitous gamma rhythm (20–80 Hz). Gamma controls spike timing, thereby influencing systems that encode information using synchrony or learn with spike-timing-dependent plasticity (STDP) [7]. Although some posit that the gamma rhythm is merely an epiphenomenon, evidence suggests it is necessary in fine odor discrimination (in insects) [8], and models of odor learning in the olfactory cortex [9] and sequence memory in the hippocampus [10] require it. Further, gamma has been implicated in (visual) object binding [11], a fundamental function that may be its raison d'être.

Cortical regions can bind neurons that represent various aspects of an object using gamma because it is more than a mere global clock. When two distinct groups of neurons are excited, neurons within each group synchronize, but the two groups have independent rhythms, failing to phase-lock. However, when the two groups overlap, all the neurons synchronize, signaling that these two groups represent a single object. Evidence suggests that this binding phenomenon requires distributed rhythmic synchrony generated by locally interacting inhibitory interneurons [12].

In this paper, we realize gamma synchrony in a population of model spiking interneurons in the same way that neurobiology does by relying on mutual inhibition. We have developed a novel silicon interneuron that includes the necessary properties that were lacking in simple neuromorphic neuron and synapse models: synaptic delay (rise time) and shunting inhibition (conductance based). Our special-purpose implementation allows us to instantiate more silicon interneurons in a fixed area while minimizing variance by avoiding increased complexity. We fabricated a network of 256 silicon inhibitory interneurons on a custom chip.

In Section II, we explain how delay and shunting enable inhibition to realize synchrony. In Section III, we describe the circuits that implement our interneuron. In Section IV, we characterize these circuits. In Section V, we use a network of these interneurons to generate synchrony. In Section VI, we use a network of interneurons to entrain excitatory principal neurons and to implement spatial binding. In Section VII, we discuss the implications of our new circuit designs.

II. Roles of Delay and Shunting

Inhibition often impedes synchrony while excitation promotes it. Mutual inhibition retards spiking, pushing nearly synchronous neurons apart, whereas mutual excitation advances the neuron that is late to spike [13], [14], bringing neurons together. Although more potent inhibition can reset the entire population, neurons do not spike together due to variations in excitability, leading to winner-takes-all behavior where only the most excitable neurons spike. Thus, inhibition often results in asynchrony and excitation in synchrony. However, these relationships can be reversed by delays.

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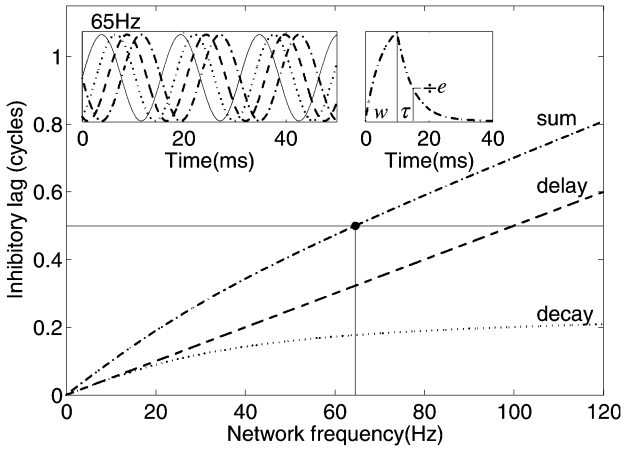

Fig. 1. Inhibition lags network activity by half a cycle at the synchronous frequency (65 Hz). The lag is the sum (dot–dash) of contributions from delay (dashed) and decay (dotted). Delay's contribution increases linearly with frequency, whereas decay's contribution saturates at a quarter cycle. Left inset: Lag of decay, delay, and their sum at the synchronous frequency; continuous line is network activity. Right inset: Inhibition has a rise time of w (10 ms) and a decay constant of τ (5 ms), obtained by low-pass filtering a pulse, which is evoked by spike. In this case, the delay ($d = w/2$) is half the rise time (Appendix II).

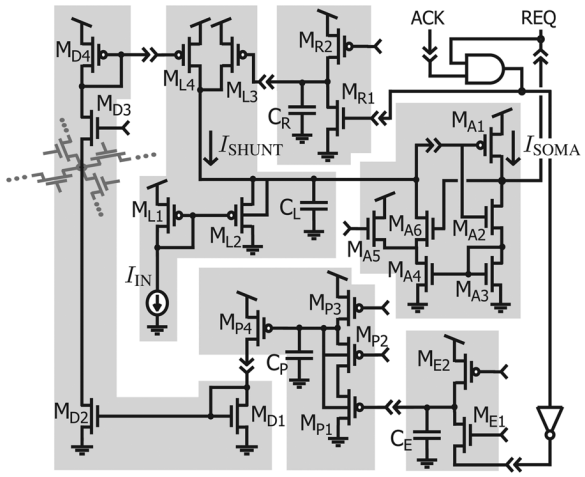

Fig. 2. Interneuron circuit comprises two modules, both based on log-domain low-pass filters: the soma and the synapse. The soma includes the membrane ($M_{L1\text{-}4}$), the axon-hillock ($M_{A1\text{-}6}$), and the refractory period ($M_{R1\text{-}2}$). The synapse includes the cleft ($M_{E1\text{-}2}$) and the receptor ($M_{P1\text{-}4}$). A diffusor with current mirrors spreads inhibition to neighboring interneurons ($M_{D1\text{-}4}$). Single arrows represent bias voltages; double arrows represent inputs and outputs. The AND gate resets the interneuron's spike (REQ), gated by an off-chip spike acknowledgment (ACK). See Appendix I for transistor sizes and capacitor values.

Synaptic delay enables inhibition to promote synchrony. In fact, for gamma, the synaptic delays found in biology are significant compared to the rhythm's period. When inhibition lags network activity, it pushes out-of-phase neurons into phase in subsequent cycles, promoting synchrony. Intuitively, delay provides an opportune period for neurons to spike together before inhibition arrives. Synchrony is stable when inhibition lags network activity by half a cycle. On the contrary, delayed excitation impedes synchrony by promoting out-of-phase spiking.

Indeed, two recent studies have shown, both numerically and analytically, that the gamma rhythm's period is proportional to the delay (axonal plus synaptic) and depends only weakly on low-pass filtering at the synapse, which responds to a spike with a rapid onset followed by an exponential decay [15], [16]. These two studies corrected earlier work that posited the decay-constant determined the network period [17], establishing unequivocally that delay is the critical parameter influencing the period of synchrony—the delay model of synchrony (DMS).

The decay constant's role is purely modulatory. Although both synaptic delay and decay contribute to inhibition's half-cycle lag at the synchronous frequency, decay can only contribute $\arctan(2\pi\tau/T)$, where τ is the decay constant and T is the network period (Fig. 1). This function saturates for small T, reaching a maximum of a quarter cycle. In that case, delay must contribute the remaining quarter cycle, resulting in $T = 4d$, where d is the delay. For large T, on the other hand, decay's contribution is negligible, so delay must contribute an entire half cycle, resulting in $T = 2d$. Thus, decay can only cause a twofold change in the network period set by delay.

In addition to delayed inhibition, synchrony requires inhibition to act as a shunt (i.e., nonzero conductance). Unlike a current sink, the current passed by a shunt is proportional to the voltage across it. Thus, neurons that have just reset their spikes receive negligible inhibition while those that are close to the spiking threshold receive massive inhibition. As a result, neurons that spike in synchrony (within the synaptic delay) remain unaffected while those that are late to spike are pushed away. Shunting inhibition also combats variations among interneurons: Excitable interneurons have higher potentials than average, increasing shunting inhibition's efficacy in reducing their rates, whereas lethargic interneurons have lower potentials, decreasing efficacy [18].

Lacking these properties, simple neuromorphic synapse and neuron models synchronize poorly when using inhibition. Current-mirror synapses (CMSs) [19] lack delay and integrate-and-fire neurons (IFNs) [20] lack shunting inhibition. Systems composed of these elements can achieve a moderate degree of synchrony, but it is fragile, requiring recurrent excitation to rescue it [21]. Another system used pulsed inhibition, which, similar to our approach, yields an effective delay, but lacking shunting inhibition, the model was sensitive to initial conditions, displaying asynchrony as well as synchrony [22]. More sophisticated neuromorphic neurons include conductance-based inhibitory synapses, but they consume silicon area, failing to reach the number of neurons necessary to support system-level phenomena [23].

Our silicon interneuron (soma and synapse circuits) remedies these deficiencies, using synaptic rise time as a surrogate for synaptic delay to synchronize robustly, while being compact in size.

III. Neuromorphic Implementation

We construct the interneuron from two circuit modules based on log-domain low-pass filters (LPFs) [24]: the soma and the synapse (Fig. 2). The soma implements membrane dynamics and spiking; the synapse supplies shunting inhibition.

A. Soma Circuit

We construct the soma from three subcircuits: the membrane, the axon-hillock, and the refractory period (Fig. 2). The mem-

brane realizes a leaky integrator (RC) response to excitatory current and shunting inhibition. An input current drives the capacitor (C_L) through a source-coupled current mirror ($M_{L1\text{-}2}$). As the capacitor voltage approaches M_{L2}'s gate voltage, the current decreases, compensating for the transistors' nonlinear (logarithmic) voltage-current relation [25]. In this paper, the input current is constant (or pulsed), whereas the leak current I_{SHUNT} varies in time; it comprises the sum of a constant current (not shown), an inhibitory synaptic current (M_{L4}), and a refractory current (M_{L3}).

The membrane's output (analogous to the potential of an RC circuit) is the soma current $I_{\mathrm{SOMA}}(M_{A1})$. Increasing I_{SHUNT} reduces the membrane's steady-state output and decreases its time-constant (identical to increasing the conductance in an RC circuit). We derive the soma behavior (ignoring the axon-hillock) by applying Kirchhoff's current law to node C_L, which yields

$$C_L \frac{dV_C}{dt} = I_{\mathrm{SHUNT}} - \frac{I_{\mathrm{IN}} I_0}{I_{\mathrm{SOMA}}} \tag{1}$$

where V_C is the potential at node C_L, I_{IN} is the input current, and I_0 is a transistor parameter. I_{SOMA} is in the denominator because we connected M_{L2}'s source and bulk nodes to C_L: As I_{SOMA} increases, M_{L2}'s source and bulk (V_C) decrease reducing its current. The result is exactly equivalent to reducing I_{IN} by the same factor.

Next, we take the derivative of $I_{\mathrm{SOMA}} = I_0\, e^{\kappa\,(V_{\mathrm{DD}} - V_C)/U_T}$ with respect to time, where V_{DD} is the voltage supply and κ and U_T (thermal voltage) are transistor parameters

$$\frac{dI_{\mathrm{SOMA}}}{dt} = -I_{\mathrm{SOMA}} \frac{\kappa}{U_T} \frac{dV_C}{dt} \tag{2}$$

which we solve for dV_C/dt and substitute into (1). Then, we multiply and divide each side of the equation by $-I_{\mathrm{SOMA}}$ and I_{SHUNT}, respectively, which results in

$$\tau \frac{dI_{\mathrm{SOMA}}}{dt} + I_{\mathrm{SOMA}} = \frac{I_{\mathrm{IN}}\, I_0}{I_{\mathrm{SHUNT}}} \tag{3}$$

where $\tau = (C_L U_t / \kappa I_{\mathrm{SHUNT}})$ is the soma's time-constant.[1]

In addition to the constant excitatory input and variable leak, the membrane also receives a positive feedback current from the axon-hillock (modified from [26] by Kai Hynna). As I_{SOMA} increases, the feedback current (M_{A6}) turns on more strongly, overpowering the leak to cause a spike. When a spike occurs, the axon-hillock initiates the process of sending it off chip, which activates the refractory period.

The refractory period shunts I_{SOMA} to near zero (pulls C_L to V_{DD}) for a brief period (a few milliseconds) after a spike, using a pulse extender (PE). The PE interfaces fast (about 10 ns) digital signals to slow (several milliseconds) analog ones by generating a current-pulse output (M_{L3}) from a voltage-pulse input. Its capacitor (C_R) is pulled to ground during a spike (M_{R1}), which causes M_{L3} to drive C_L to V_{DD}, until the leak through M_{R2} restores C_R.

[1]Equation (3) is analogous to a conductance-based equation where E, the reversal potential, is zero

$$\tau \frac{dV}{dt} + (V - E) = \frac{I_{\mathrm{IN}}}{G}.$$

Here, V is the soma potential, G is the shunting conductance to E, and $\tau = C/G$ is the time-constant.

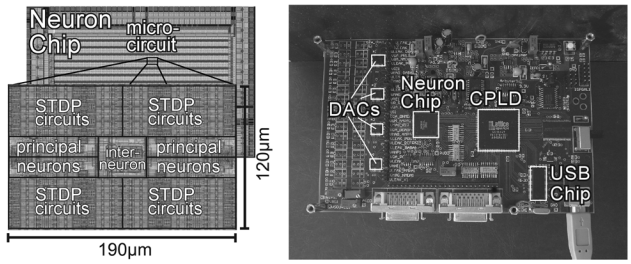

Fig. 3. (a) Neuron chip has a 16-by-16 array of microcircuits; one microcircuit includes one inhibitory interneuron and four principal neurons, each with 21 STDP circuits. (b) Neuron chip is embedded in a circuit board including DACs, a CPLD, and a USB chip, which communicates with a PC.

B. Synapse Circuit

We construct the synapse from two subcircuits: the receptor and the cleft (Fig. 2). The receptor, implemented with an LPF, sets the synapse's decay constant (similar to [27]), while the cleft, implemented with a PE, sets its rise time. The receptor differs from the soma's membrane in that its input (from the cleft) is a fixed-height pulse, which allows for a simpler circuit: a voltage-limited source follower ($M_{P1\text{-}2}$), whose voltage limit (applied to M_{P2}'s gate) sets the pulse height, and hence, the maximum current level that the receptor's output (M_{P4}) can achieve (synaptic strength). It saturates at this level when driven at a high rate or with a pulse width that is long relative to its decay constant.

The synapse's output current drives a diffusor [28], which spreads the synaptic current to neighboring silicon interneurons, realizing all-to-all inhibition (unless otherwise noted).

C. Chip Architecture

We have designed, submitted, and tested a chip with an array of our silicon interneurons [14]. Our circuits are similar in size and complexity to IFNs with CMSs (256 interneurons use only 2.6% of the chip's 10-mm^2 area), yet are capable of modeling phenomena that depend on synaptic rise time or shunting inhibition. Our log-domain neuron and its synapse are generally applicable to neuromorphic systems; we used neurons with similar somas and synapses in a previous model of hippocampal associative memory [29].

The neuron chip was fabricated through MOSIS in a 1P5M 0.25-μm complementary metal–oxide–semiconductor (CMOS) process, with just under 750 000 transistors in just over 10 mm^2 of area [Fig. 3(a)]. It has a 16 by 16 array of microcircuits. Each microcircuit contains one inhibitory interneuron (28μm by 36μm each) commingled with four principal neurons. Each principal neuron has 21 STDP circuits that are not used here [14]. The neuron chip uses the address–event representation (AER) to transmit spikes off chip and to receive spike input [30]–[32]. In addition, it includes an analog scanner that allows us to observe the state of one neuron at a time (either its synapse or soma) [33].

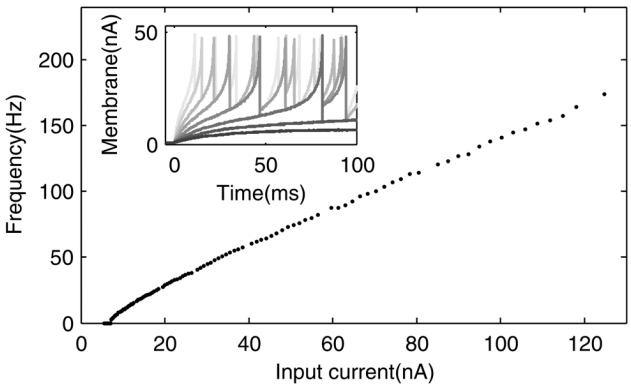

Fig. 4. Soma responds sublinearly to current (above a threshold). Inset: Membrane (current) traces for several step-input current levels show an RC rise and a positive-feedback spike.

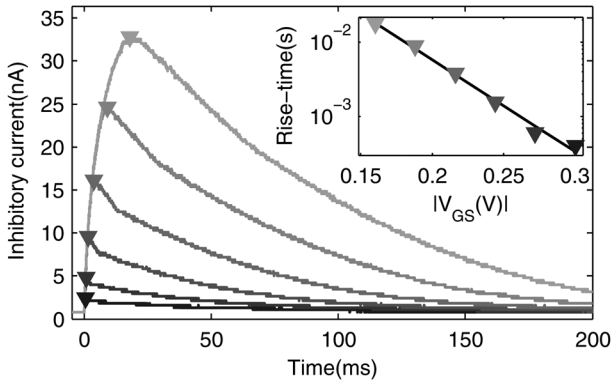

Fig. 5. Synapse responds to a spike with a low-pass filtered pulse. Inset: The time-to-peak (triangles) depended exponentially on the gate-source voltage of the cleft's leak transistor (M_{E2} in Fig. 1).

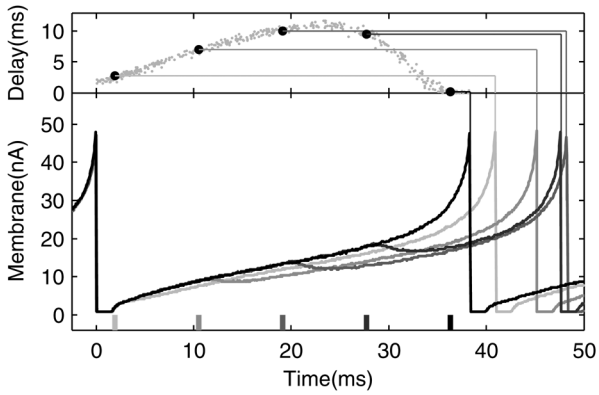

Fig. 6. Increase in interspike interval depends on when inhibition occurs. Bottom: Membrane (current) traces of an interneuron that we drove with a constant current and inhibited at various phases reveal that the response to inhibition depended on when it occured (vertical bars). Top: The PRC shows that inhibition is most effective between 15 and 30 ms after the interneuron spikes, adding over 8 ms to its interspike interval (38 ms).

To test the silicon interneurons, we embedded the neuron chip in a circuit board [Fig. 3(b)]. The board has four primary components: a complex programmable logic device (CPLD), the neuron chip, a universal serial bus (USB) interface chip, and digital-to-analog converters (DACs). The central component in the system is the CPLD; it mediates communication between the neuron chip and the USB chip, which provides a bidirectional link with a PC. The DACs enable the PC to control the analog biases in the system.

IV. Neuron Characterization

In characterizing the interneuron, we focused on three aspects: the frequency-current curve (FIC), the synaptic rise time, and the phase-response curve (PRC). The PRC summarizes the effects of synaptic rise time and shunting inhibition on the soma. These three aspects describe the properties relevant to generating synchrony.

A. Frequency-Current Curve

When various current levels are injected into the soma, its spike frequency increases sublinearly above a threshold (Fig. 4). Below this threshold (8 nA), the input current drove the soma to a steady-state level too low for the positive feedback to overcome the leak (see the inset in Fig. 4).[2] Above it, the input current invoked sufficient positive feedback to overcome the leak resulting in a spike (which shut off the input by lowering M_{L2}'s source).

B. Synaptic Rise Time

When stimulated with a spike, the synaptic current increased linearly (far from the maximum level), and then decreased exponentially (decay-constant fit was 70 ms). We characterized the synaptic rise time, defined as the time-to-peak (Fig. 5), by varying the cleft's leak current (adjusting M_{E2}'s gate voltage) and hence the pulse width. The rise time depended exponentially on M_{E2}'s gate voltage, because the pulse width is inversely proportional to the current through this transistor. Also, the peak current increased with the pulse width, since the receptor's current had more time to rise.

C. Phase-Response Curve

The effect of synaptic inhibition depended on the phase at which it occurred. We characterized this phase dependence by inhibiting the interneuron at a random point in its cycle, once every five cycles, observing the increase in interspike interval (ISI). We repeated this process several hundred times and plotted the resulting PRC (top of Fig. 6). The rise time was set to 1.5 ms and the synaptic decay constant was 5 ms, as found in biology [34], [35].

The interneuron was most sensitive to inhibition between 15 and 30 ms after it spiked (its uninhibited ISI was 38 ms). In this sensitive region, each inhibitory spike added more than 8 ms to the interneuron's ISI. During this phase of its cycle, the interneuron's membrane (current) was high, resulting in more effective shunting inhibition (bottom of Fig. 6). On the other hand, inhibition applied less than 5 or more than 32 ms after it spiked added less than 4 ms to the interneuron's ISI. During these phases, either its membrane potential was low, so shunting inhibition was less effective, or the inhibition did not have time to rise to its peak

[2]To estimate the input current to an interneuron, we measured its amplified soma current ($I_{\mathrm{SOMA}} = (I_{\mathrm{IN}} I_0 / I_{\mathrm{SHUNT}})$) through a current-out pad, which yields I_{IN} when $I_{\mathrm{SHUNT}} = I_0$. Hence, we disabled the inhibitory synapse (by lowering its synapse strength); we also disabled the axon-hillock (by raising its spike threshold). We estimated the input current as the pad current divided by the pad amplifier's gain (3564). Because the gain decreased for currents above 34 nA, we fit lower values with an exponential to extrapolate the input current.

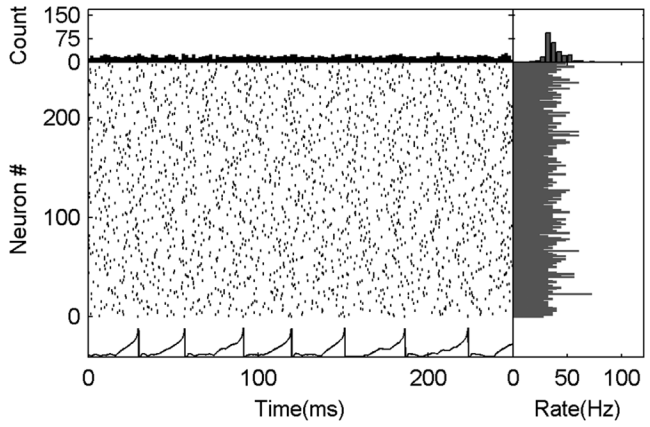

Fig. 7. Uncoupled interneurons spike asynchronously. Bottom left: Rasters of all 256 interneurons and membrane potential (current) of one representative interneuron. Top left: Histogram of spike activity (2 ms bins). Bottom right: Average spike rate for each interneuron. Top right: Distribution of spike rates for all interneurons.

effectiveness. Near the cycle's end, the positive feedback from the axon-hillock turned on, overpowering the inhibition.

V. Silicon Synchronization

Having characterized an individual interneuron's properties, we tested several aspects of the silicon interneuron network's ability to generate synchrony, focusing specifically on the direct role of the synapse's rise time and the modulatory role of its decay constant. DMS predicts the synaptic rise time should control the network period, modulated by the decay constant. We also varied the values of the interneuron's other parameters for comparison. To further challenge the network, we investigated its ability to synchronize with noisy inputs as well as when reciprocally connected to the excitatory principal neurons.

A. Uncoupled Network

For the uncoupled (16 by 16) network, we configured each interneuron to inhibit only itself (analogous to a calcium-dependent potassium channel population) by limiting the diffusor spread (Fig. 7). Each interneuron spikes asynchronously at its own rate with a constant input current (31 nA); together the interneurons express a frequency coefficient of variation (CV) of 0.24. The intrinsic variations among the neurons result in spike rates between 16 Hz for the least excitable interneuron and 72 Hz for the most excitable one.

B. Synaptic Rise Time

We tested the network's ability to synchronize for infinitesimal (0.1 ms) and finite (11.7 ms) rise times. We drove each interneuron with a constant current (31 nA) and configured it to inhibit itself and all of its neighbors, using a diffusor biased to spread synaptic current globally (all to all). When the rise time was infinitesimal, inhibition had less time to rise, reaching a lower peak. Therefore, we increased the amplitude of inhibition (by increasing the maximum level) in that case. In both cases, the interneurons received about the same amount of inhibition, spiking at about the same rate, with about the same number of interneurons active. The average rate was 36 Hz versus 38 Hz and the number of active interneurons (those that spiked at least once in 250 ms) was 115 (45%) versus 120 (47%) with the finite and infinitesimal rise times, respectively.

Synchrony by inhibition required a synaptic rise time. Using an infinitesimal rise time, the network did not synchronize [Fig. 8(a)], whereas using a finite rise time, the network synchronized at 38 Hz [Fig. 8(b)]. We quantified synchrony by calculating the network's vector strength (VS) [36]. VS is a normalized sum of unit-length vectors, one for each spike: Their angles correspond to the spike's phase relative to the strongest frequency (from an FFT of 3 s of the population histogram). If all of the neurons' spikes lined up at the same phase (perfect synchrony), VS would equal one. Conversely, if the neurons' spikes distributed themselves at random phases (asynchronous), VS would approach zero. Unlike other synchrony measures, VS does not penalize suppression of neurons, which is useful in our system. VS penalizes frequency drift and phase shift, however. To minimize this effect, we only calculated VS across a brief period—750 ms. VS equaled 0.18 and 0.83 for the infinitesimal and finite rise times, respectively.

To confirm the synaptic rise time's pivotal role in synchrony (DMS), we varied it and measured the network period (the inverse of the strongest frequency). The network period was one to two times the rise time, depending on the fall time (i.e., synaptic decay constant), plus an offset, caused by the axon-hillock's positive feedback overpowering inhibition shortly before a spike. With a rise time of 11.7 ms, and a synaptic decay constant of 5 ms [same as Fig. 8(b)], the network period (24.2 ms), minus an offset (7.3 ms), was 1.44 times the rise time. This same proportionality constant yielded a good fit for rise times ranging from 7 to 100 ms (Fig. 9). The period deviated from the linear fit as the rise time approached the decay constant (5 ms). The network was synchronous (VS > 0.5) for rise times between 10 and 60 ms.

The offset had the effect of increasing the rise time by 5.1 ms (7.3 ms $\div$ 1.44), which corresponds to a axon-hillock delay of about 2.6 ms, since the rise time is twice the effective delay (See Appendix II). The axon-hillock circuit takes several milliseconds to fully depolarize the soma (and tens of nanoseconds to send the spike off chip) once positive feedback takes over. This effect is visible in the PRC: At the end of its period, the interneuron is resistant to inhibition (Fig. 6). Positive feedback's speed depends on how far above threshold the input current drives the soma and, therefore, on the magnitude of the input current (inset of Fig. 4).

C. Other Synaptic Parameters

We have verified that the synaptic rise time affects the network period directly. But because changing the rise time changes both the inhibitory delay and amplitude (Fig. 5), it is unclear which effect influences the period. If the change in network period is caused by the change in inhibitory delay, we expect that changing the synaptic strength (with a fixed rise time) would not change the network period.

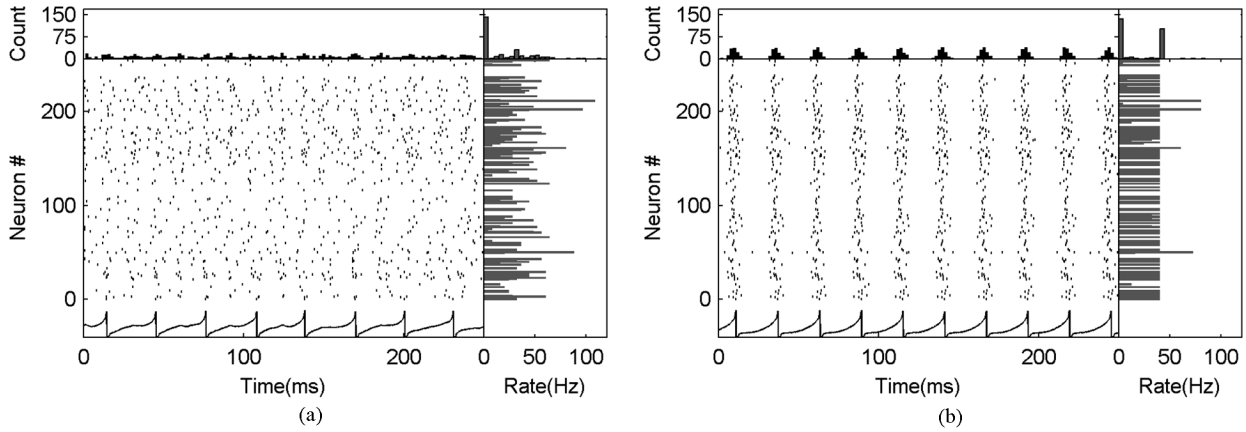

Fig. 8. Synchrony requires finite synaptic rise time. (a) With a infinitesimal rise time (0.1 ms), the interneurons (115 of 256 active) spiked asynchronously (vector strength = 0.18). (b) With a finite rise time (11.7 ms), the interneurons (120) spiked synchronously (vector strength = 0.83). Conventions are the same as in Fig. 7.

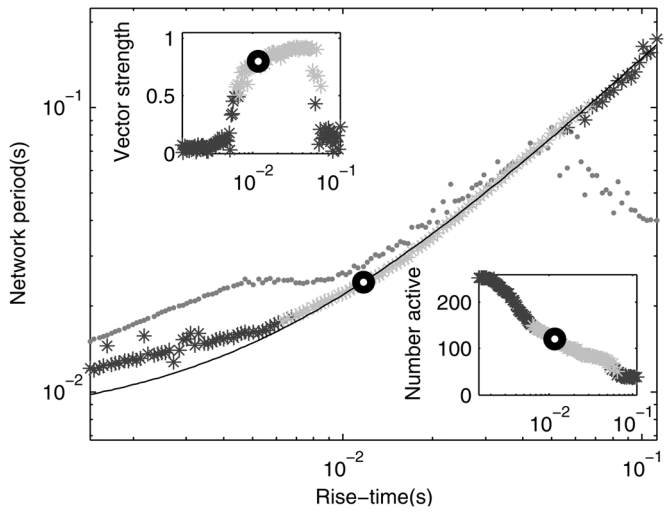

Fig. 9. Network period (asterisks) increases linearly (black line) with the rise time (fit from 7 to 58 ms). The network period ceases to be linear and saturates when the rise time is small (below 7 ms). The dots show the average interneuron period (excluding suppressed interneurons). Left inset: Vector strength peaks for a rise time of about 25 ms. Right inset: Number of active interneurons decreases as rise time increases. For all panels, light asterisks signify highly synchronous network states with vector strength greater than 0.5 and active interneurons greater than 50. The black circle is the baseline setting; it has the same parameter values across figures.

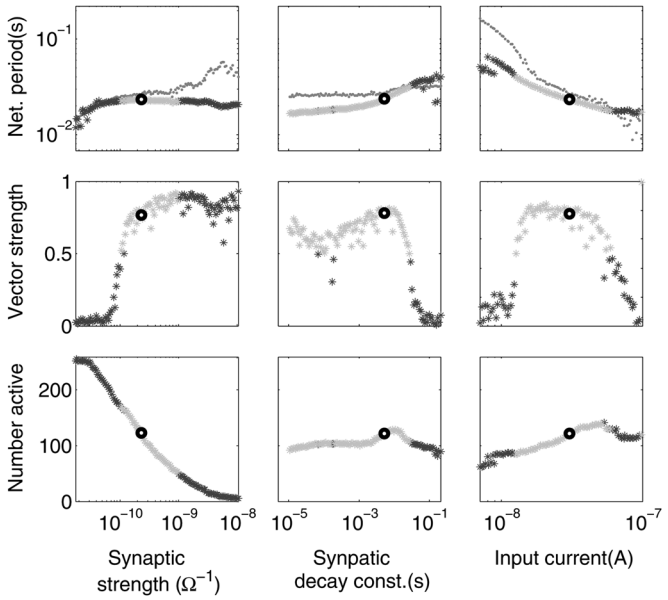

Fig. 10. Synaptic strength, synaptic decay constant, and input current influence network period as well as vector strength and number of active interneurons, but none affect the network period as strongly as the synaptic rise time. Conventions are the same as in Fig. 9.

To determine the synaptic strength's influence on synchrony, we varied it and measured the network period.[3] The network period was nearly constant, within 2 ms (7%), even though we varied the synaptic strength nearly an order of magnitude (left column of Fig. 10). Therefore, we conclude that rise time affects the network period by changing the inhibitory delay, supporting DMS.

The synaptic strength does not change the network period but it has a strong effect on VS and number of active interneurons (NAI). A small synaptic strength (less than 0.11 $G\Omega^{-1}$) results in asynchronous spiking, because interneurons only weakly interact and are, therefore, unable to entrain each other. As the synaptic strength increases, VS increases, until it reaches a critical point (about 1.0 $G\Omega^{-1}$) where NAI becomes low, the network exhibiting winner-take-all behavior.

We also investigated the synaptic decay constant's role by varying it and measuring the network period (middle column of Fig. 10). Our analysis (Appendix II) predicts that the network period is between two and four times the effective delay, with the proportionality constant's exact value determined by the synaptic decay constant, which has a modulatory role (Fig. 1). As predicted, the network period increased (16.5 to 31.9 ms) with increasing synaptic decay constant (1.1 μs to 27.3 ms) for synchronous network states. Thus, the network period ranged from 1.0 to 1.9 times the synaptic rise time (plus offset), consistent with DMS.

[3]To estimate the synaptic conductance, we measured the synapse's maximum current (achieved by stimulating the synapse fast enough to keep M_{P1} on) through a current-out pad, divided by the pad amplifier's gain (3564). We fit our measurements to an exponential for various gate voltages on M_{P2}, obtaining I_{MAX} and κ values, which we used to calculate the equivalent conductance ($\kappa I_{\mathrm{MAX}}/U_T$), where $U_T = 25.6$ mV.

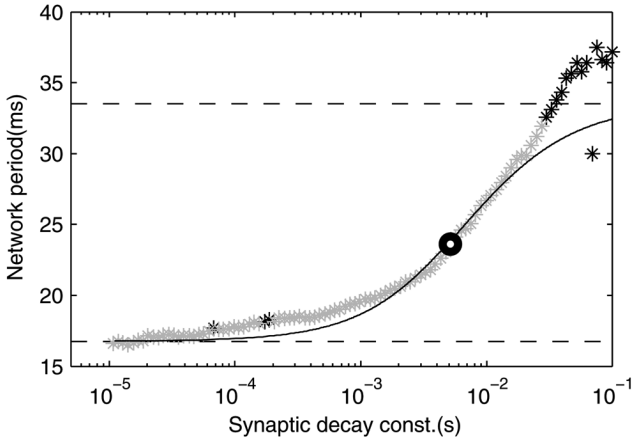

Fig. 11. Synaptic decay constant modulates network period (asterisks) in the range of two to four times the effective delay (dashed lines). For synchronous network states (light asterisks), the network period is similar to the predicted value (solid line) with a rise time of 11.7 ms (plus 5.1 ms from the axon-hillock, fit from Fig. 9).

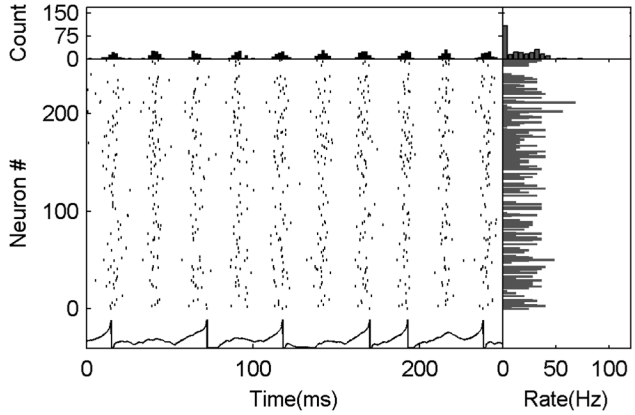

Fig. 12. Synchrony by inhibition is robust to noisy input. Interneurons driven by Poisson-generated spikes (1-ms pulses, 600-Hz mean rate) synchronize with the same frequency as with constant input [Fig. 8(b)]; however, the vector strength reduces from 0.83 to 0.75. On the contrary, the number of active interneurons increases from 120 to 148. Conventions are the same as in Fig. 7; parameters are the same as in Fig. 8(b).

We fit the synaptic decay constant's effect on the network period to our analytical prediction (See Appendix II)

$$\tan(\omega d) = -\omega\tau \tag{4}$$

where ω is 2π divided by the network period, τ is the synaptic decay constant, and d is the effective delay. Using the estimated effective delay and measured network period, we observe that for synchronous states the data are similar to the predicted value (Fig. 11).

D. Input Current

To evaluate the input current's influence on synchrony, we varied it, observing the change in network period. The input current had a modulatory effect on the network period, which decreased from 38.2 to 19.6 ms as the input current increased from 13 to 46 nA (right column of Fig. 10). The input current changes the network period indirectly by influencing the time it takes the axon-hillock to spike after the soma reaches threshold, which changes the delay offset. At medium input current (31 nA), an axon-hillock delay of 2.6 ms accounts for the observed network period of 24.2 ms. For a smaller input current (13 nA), a 7.4-ms delay accounted for the extended network period (38.2 ms); for a larger input current (46 nA), a 1.0-ms delay accounted for the truncated network period (19.6 ms).

In addition to the axon-hillock delay, input current influenced VS and NAI. At small input current levels (below 10 nA), interneurons spiked at low rates, resulting in a deficiency of inhibition in the network, insufficient to synchronize the population. As input current increased, spike rates and inhibition increased, enabling synchrony, and increasing NAI. Large input currents (above 50 nA) drove many interneurons hard enough to make them insensitive to inhibition, resulting in an asynchronous state. These most excitable interneurons suppressed the other interneurons that were still sensitive to inhibition, reducing NAI.

E. Poisson Input

Our results show that silicon interneurons synchronize in the gamma frequency range. However, most of our neurons spike at the network rhythm, which is inconsistent with biological observations: Individual interneuron's membrane potentials (currents) phase-lock with gamma, but they do not spike each cycle; instead, they skip cycles randomly due to suppression from other interneurons in the population [37]. A numerical study showed that neuronal variability and noise in excitatory synapses can account for this biological behavior [38].

To test our network in a noisy environment, we replaced the constant current input with Poisson pulses (1 ms) at an average rate of 600 Hz (equivalent to 100 inputs at 6 Hz), generated independently for each neuron (Fig. 12). With all parameters the same as without input noise [Fig. 8(b)], interneurons synchronized with a network period (25 ms) almost identical to the one without noise (26 ms).

As expected, interneurons failed to spike in every cycle, skipping them when they received less input (randomly), which rendered them susceptible to suppression by other interneurons (Fig. 12; compare membrane potential trace with those in Figs. 7 and 8). The random spiking provided an opportunity for less excitable interneurons to participate (NAI $=$ 148 compared to 120 with constant input), because more excitable interneurons, which inhibited them, did not spike every cycle. But it reduced the network coherence (VS $=$ 0.75 compared to 0.83 with constant input) by jittering interneurons' spiking phases. When we reduced the input rate, which increased the noise and reduced excitatory drive, VS and NAI decreased, but the network period remained constant (not shown).

VI. Excitatory–Inhibitory Interactions

Having characterized our interneurons' synchrony, we tested their ability to entrain the principal neurons. The interneurons inhibit the principal neurons through the same diffusor they use

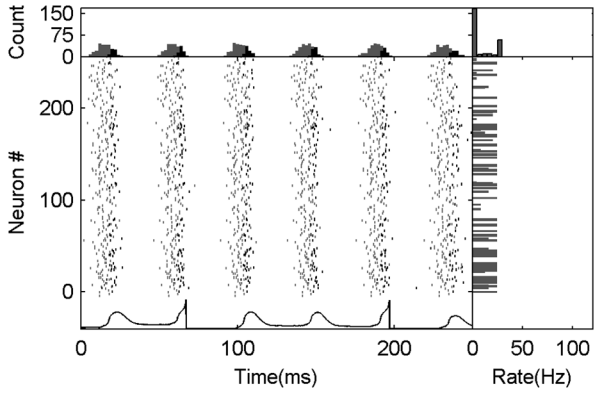

Fig. 13. Interneurons synchronize when driven by excitatory principal neurons, entraining them as well. The interneurons' degree of synchrony increases (vector strength = 0.95) with principal neuron input over constant input [Fig. 8(b)]; however, the number of active interneurons decreases from 120 to 89. Conventions are the same as in Fig. 7. Light rasters and histogram represent excitatory neurons; spikes from only one of four excitatory neurons from each microcircuit are shown.

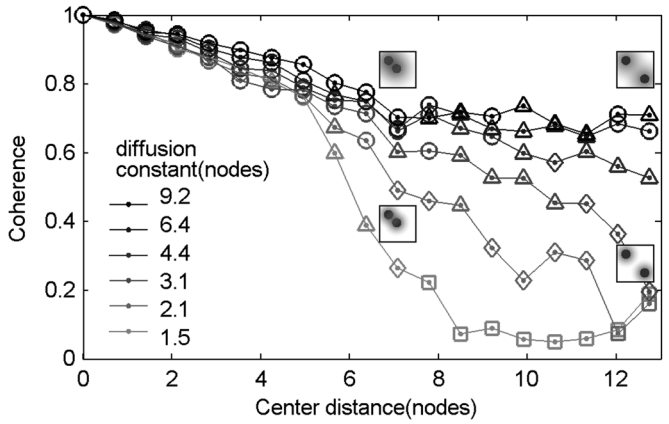

Fig. 14. Patches' coherence (see Section VI-B) decreases as either distance (x-axis) increases or diffusion (line style) decreases. □: Average periods differed by over 0.2 ms. ◇: Average phases differed by over 20°. △: Average phases differed by 10°–20°. ◯: Average phases differed by less than 10°. Icons: Black disks and gray halo represent stimulated patches of principal neurons and the range of inhibition, respectively.

to inhibit each other. The principal neurons drive the interneurons with fast excitatory synapses (1-ms current pulse) through an additional diffusor (that spreads excitation broadly).

A. Principal Neuron Entrainment

To confirm that interneurons entrain principal neurons, we drove the principal neurons with a constant current input. When the principal neurons spiked, they drove the interneurons to spike with some delay (6-ms average); the interneurons in turn inhibited the principal neurons (Fig. 13). The current drive to the interneurons then ceased, as did their spiking. Once the inhibition decayed sufficiently, the principal neurons spiked again, repeating the process. The network behavior was similar to the interneuron network alone but with added delay—the time the principal neurons spiked to the time the interneurons spiked. Adding twice the average time difference to the effective delay we found earlier (from the fit in Fig. 9) yielded a network period of 41.4 ms; we measured 42.9 ms.

The interaction between the interneuron and principal neuron populations provided a structured input to the interneurons, increasing VS to 0.95 [from 0.83 with the constant current input; Fig. 8(b)]. The interaction decreased NAI to 89 from 120, a result of the added variability in potency and timing from the principal neurons' excitatory drive to the interneurons. Unlike Poisson input, excitation from principal neurons was repetitive, providing approximately the same excitation each period; however, the drive received varied among interneurons. On one end of the spectrum, interneurons near excitable principal neurons that consistently spiked early and drove strong synapses, received potent excitation, causing many of them to spike. On the other hand, interneurons near lethargic principal neurons that consistently spiked late and drove weak synapses received feeble excitation, causing many of them to be silenced by inhibition.

B. Application to Binding

In addition to entraining principal neurons across the whole network, interneurons can entrain local, independent patches of principal neurons with spatially distributed synchrony. They generate spatially distributed synchrony when we reduce the spread of inhibition, such that each interneuron only inhibits principal neurons and other interneurons within a few microcircuits (nodes). This distributed synchrony can realize binding; we define two patches as binding if they synchronize coherently. We quantified the binding between two patches with their coherence, defined as the normalized dot product of the two patches' (interneuron) population histograms over 10 s, which yields a value between zero (nonoverlapping histograms) and one (identical histograms).

We tested binding in the network by stimulating (with constant current) two circular 145-principal neuron patches (3.4-node radii) spaced various distances apart; we also varied inhibition's diffusion constant (Fig. 14). Binding was largely independent of distance when the diffusion constant[4] was high (4.4 nodes or more); coherence remained above 0.5. In contrast, binding depended on distance when the diffusion constant was low; as the distance between patches increased, coherence decreased.

Coherence between patches was degraded by two factors: period and phase differences. To calculate the period or phase differences between patches, we subtracted the period or phase [found using a fast Fourier transform (FFT) as before] of the first patch from that of the second (one second of data). We calculated the average difference by repeating this procedure ten times (over 10 s of data) and taking the root mean square (rms) of the differences. When the rms period difference exceeded 0.2 ms (0.5%), coherence was low, ranging from 0.05 to 0.22. When the periods were similar but the rms phase difference exceeded 20°, coherence was moderate, ranging from 0.20 to 0.57. When the phase difference was between 20° and 10° or below 10°, coherence was high, ranging from 0.39 to 0.81 or from 0.60 to 1.00, respectively.

[4]We calculate the diffusion constant as $\sqrt{w_H/w_V}$, where $w_H = w_{H0}e^{\kappa V_H/U_T}$ and $w_V = w_{V0}e^{\kappa V_V/U_T}$ are the strengths of the diffusor's horizontal and vertical transistors. V_H and V_V are their gate voltages, and w_{H0} and w_{V0} are their width-to-length ratios, respectively. We set $\kappa = 0.75$ and $U_T = 26.5$ mV.

VII. Discussion

Our work extends DMS to include the synaptic rise time using the concept of effective delay and provides a quantitative description of the synaptic decay-constant's role as well (see Appendix II). Previous DMS models used pure delays to model synchrony in populations of inhibitory interneurons and only provided a qualitative description of the synaptic decay constant's role [15], [16]. We have shown that effective delay in the form synaptic rise time, generated by low-pass filtering of a pulse, acts as a surrogate for a pure delay equal to half the pulse width. Synaptic rise time is useful for generating synchrony in physical systems, such as silicon systems, where pure delays are hard to come by.

The rise time is not only necessary for synchrony; it determines the network period. We found the network period to be proportional to the rise time, which delayed inhibition by between a quarter and a half cycle (depending on the synaptic decay constant). This explains rise time's role in setting the period, as ideal network activity should be half a cycle out of phase with inhibition (Fig. 1) [15]. In addition to rise time, other sources of delay can influence the network period: Axonal propagation is the primary source of delay in biology.

Our network represents the first neuromorphic model of population synchrony by inhibition, verifying that synchrony by inhibition is robust to neuronal variability (from transistor mismatch). When inhibiting each other, 45%–47% of interneurons were active. In the asynchronous case (fast rise time), these interneurons had a frequency coefficient of variation (CV) of 0.52, whereas in the synchronous case (slow rise time), the CV decreased to 0.28 (in both cases the CVs were 0.24 when each neuron only inhibited itself). Further, this synchrony is robust to parameter variations with the network achieving synchrony when synaptic parameters varied nearly an order of magnitude or more (depending on the parameter) and when input current varied more than a factor of three.

Our silicon interneurons synchronize using shunting inhibition with a rise time, demonstrating that silicon is an appropriate medium to build dense networks of conductance-based neurons. Although synchrony is robust to variations, inhibition suppresses many lethargic interneurons. Augmenting inhibition with fast excitation (gap junctions) among interneurons may increase NAI by providing additional current to less excitable neurons, giving them the chance to spike before being inhibited. In addition, biology could employ other tactics (e.g., homeostasis) to reduce variance, and thereby, rescue suppressed interneurons.

We have shown that local inhibitory interactions, which generate synchrony in a spatially distributed manner, can mediate binding, which is not possible with a global clock. When these interactions are far-reaching (mediated by a diffusive grid), coherence was weakly dependent on distance; however, when the extent of the interactions is only a few nodes, coherence depends strongly on distance: Patches of neurons were incoherent until they fused into a single patch, realizing binding. The two groups need only to have overlapping memberships to synchronize, thus this mechanism is generally applicable—connections among a few neurons that represent each aspect of an object are sufficient to synchronize them all.

TABLE I
Transistor Sizes and Capacitor Values

Transistor	Width / Length (μm / μm)	Transistor	Width / Length (μm / μm)
M_{A1}	1.4 / 3.7	$M_{E2, L4, P3}$	0.7 / 4.7
$M_{A2\text{-}4,6}$	0.6 / 2.4	$M_{L1\text{-}2}$	1.4 / 2.0
M_{A5}	0.6 / 2.2	M_{L3}	0.7 / 1.4
$M_{D1\text{-}2}$	0.7 / 5.1	M_{P1}	1.2 / 4.7
M_{D3}	1.2 / 1.2	M_{P2}	1.7 / 2.5
$M_{D4, P4}$	1.4 / 2.0	M_{R1}	0.6 / 1.1
M_{E1}	1.0 / 1.6	M_{R2}	0.6 / 3.1

Capacitor	Value (fF)	Capacitor	Value (fF)
C_E	78	C_P	1500
C_L	1400	C_R	37

Appendix I

See Table I.

Appendix II
Synaptic Rise Time in Synchronization

DMS quantitatively describes the synchronous behavior of populations of interneurons with axonal and synaptic delay, pure delay. In this section, we extend DMS to include synaptic rise time using the concept of effective delay. Specifically, we show that the effective delay of a synapse whose impulse response (i.e., spike response) is a low-pass filtered pulse is equal to half the pulse width. Further, unlike previous analyses, we derive an explicit role for the inhibitory decay constant. Building on the arguments in [16], we show that it sets the network period to between two and four times the effective delay, or equivalently between one and two times the pulse width.

Consider a population of inhibitory interneurons whose activity $A(t)$ is modeled by the following differential equation:

$$\lambda \dot{A(t)} = -A(t) + F(I - k(t) * A(t)) \tag{5}$$

where I is the constant input current, $k(t)$ is the synaptic impulse response, F is the neuronal transfer function, and λ is the soma's time-constant; $*$ represents convolution in time. λ can be instantaneous when the feedback inhibition (or any input) is fast [39], therefore, we set it to zero, which is equivalent to assuming the network activity is 180° out of phase with the inhibition [15].

We wish to determine if a rhythmic solution exists. To this end, we linearize the neuronal transfer function about the asynchronous state $A(t) = C$ (in this state neuronal firing is constant), which gives

$$0 = -y(t) - ak(t) * y(t) \tag{6}$$

where $y(t) = A(t) - C$ is the difference of network activity from the asynchronous state and a is the linearized neuronal transfer function at the asynchronous state.

Next, we assume $y(t)$ is periodic with a solution of the form $y(t) = e^{i\omega t}$ ($\omega = 2\pi/T$, where T is the network period) and transform (6) into the frequency domain

$$0 = -Y(\omega) - aY(\omega)K(\omega). \tag{7}$$

We use a synapse whose impulse response is a convolution of a pulse (width T_p) and an exponential [40], which in the frequency domain is represented by

$$K(\omega) = 2dB\mathrm{sinc}(\omega d)e^{-i\omega d} \times \frac{G}{\left(\frac{1}{\tau} + i\omega\right)} \tag{8}$$

where τ is the synaptic decay constant, $d = T_p/2$ is the effective synaptic delay, B is the pulse amplitude, and G is the exponential amplitude. The pulse provides effective delay (whereas the convolution of two exponentials would not).

We substitute (8) into (7) and separate it into two equations, one for the real part and one for the imaginary part, using the identity $e^{ix} = \cos(x) + i\sin(x)$, which gives

$$\begin{aligned} \sin(\omega d) &= \frac{\omega\tau}{2ad\tau BG\mathrm{sinc}(\omega d)} \\ \cos(\omega d) &= \frac{-1}{2ad\tau BG\mathrm{sinc}(\omega d)}. \end{aligned} \tag{9}$$

Assuming a solution exists (the right side of each equation is between negative and positive one), the two equations can be combined to obtain (4), which is identical to the relation for a synapse with a (purely) delayed exponential impulse response (similar to [16]).

Since $\tan(x)$ is negative for $\pi/2 < x < \pi$, we see from (4) that if $\tau \gg d$, $\omega d \Rightarrow \pi/2$, yielding $T = 4d$, where T is the network period. Conversely, if $\tau \ll d$, $\omega d \Rightarrow \pi$, yielding $T = 2d$. Therefore, T depends strongly on d, which provides its absolute minimum and maximum ($2d < T < 4d$), and weakly on τ, which determines the value it takes within this range. If we relate the network period back to the pulse width, we see $T_p < T < 2T_p$. Thus, we have extended the model put forth by [16] to include the synaptic rise time (using a pulse), which describes the behavior of our silicon inhibitory interneuron network that uses nonzero synaptic rise time instead of pure synaptic delay to synchronize.

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REFERENCES

[1] M. Mahowald and C. A. Mead, "The silicon retina," *Scientific American*, vol. 264, no. 5, pp. 7682–7682, 1991.

[2] K. A. Zaghloul and K. Boahen, "Optic nerve signals in a neuromorphic chip I: Outer and inner retina models," *IEEE Trans. Biomed. Eng.*, vol. 51, no. 4, pp. 657–666, Apr. 2004.

[3] R. F. Lyon and C. A. Mead, "An analog electronic cochlea," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. ASSP-36, no. 7, pp. 1119–1134, Jul. 1988.

[4] B. Wen and K. Boahen, "Active bidirectional coupling in a cochlear chip," in *Advances in Neural Information Processing Systems*, Y. Weiss, B. Schölkopf, and J. Platt, Eds. Cambridge, MA: MIT Press, 2006, vol. 18, pp. 1497–1504.

[5] T. Y. W. Choi, P. A. Merolla, J. V. Arthur, K. A. Boahen, and B. E. Shi, "Neuromorphic implementation of orientation hypercolumns," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 6, pp. 1049–1060, Jun. 2005.

[6] P. A. Merolla, J. V. Arthur, B. E. Shi, and K. A. Boahen, "Expandable networks for neuromorphic chips," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 2, pp. 301–311, Feb. 2007.

[7] G. Q. Bi and M. M. Poo, "Synaptic modifications in cultured hippocampal neurons: Dependence on spike timing, synaptic strength, and postsynaptic cell type," *J. Neurosci.*, vol. 18, pp. 10464–72, 1998.

[8] M. Stopfer, S. Bhagavan, B. H. Smith, and G. Laurent, "Impaired odour discrimination on desychronization of odour-encoding neural assemblies," *Nature*, vol. 390, pp. 70–74, 1997.

[9] J. J. Hopfield and C. D. Brody, "Learning rules and network repair in spike-timing-based computation networks," *Proc. Nat. Acad. Sci.*, vol. 101, pp. 337–342, 2004.

[10] O. Jensen and J. E. Lisman, "Theta/gamma networks with slow NMDA channels learn sequences and encode episodic memory: Role of NMDA channels in recall," *Learn. Memory*, vol. 3, pp. 264–278, 1996.

[11] R. Eckhorn, R. Bauer, W. Jordan, M. Brosch, W. Kruse, M. Munk, and H. J. Reitboeck, "Coherent oscillations: A mechanism of feature linking in the visual cortex? multiple electrode and correlation analyses in the cat," *Biol. Cybern.*, vol. 60, pp. 121 130–121 130, 1988.

[12] A. Bragin, G. Jando, Z. Nadasy, J. Hetke, K. Wise, and G. Buzsáki, "Gamma (40–100 Hz) oscillation in the hippocampus of the behaving rat," *J. Neurosci.*, vol. 15, pp. 47–60, 1995.

[13] S. R. Campbell, D. L. Wang, and C. Jayaprakash, "Synchrony and desynchrony in integrate-and-fire oscillators," *Neural Comput.*, vol. 11, pp. 1595–1619, 1999.

[14] J. V. Arthur and K. Boahen, "Learning in silicon: Timing is everything," in *Advances in Neural Information Processing Systems*, Y. Weiss, B. Schölkopf, and J. Platt, Eds. Cambridge, MA: MIT Press, 2006, vol. 18, pp. 75–82.

[15] N. Brunel and X. J. Wang, "What determines the frequency of fast network oscillations with irregular neural discharges? I. synaptic dynamics and excitation-inhibition balance," *J. Neurophysiol.*, vol. 90, pp. 415–430, 2003.

[16] R. Maex and E. D. Schutter, "Resonant synchronization in heterogeneous networks of inhibitory neurons," *J. Neurosci.*, vol. 23, pp. 10 503–10 514, 2003.

[17] X. J. Wang and G. Buzsáki, "Gamma oscillations by synaptic inhibition in a hippocampal interneuron network," *J. Neurosci.*, vol. 16, pp. 6402–6413, 1996.

[18] I. Vida, M. Bartos, and P. Jonas, "Shunting inhibition improves robustness of gamma oscillations in hippocampal interneuron networks by homogenizing firing rates," *Neuron*, vol. 49, pp. 107–117, 2006.

[19] K. A. Boahen, "A retinomorphic vision system," *IEEE Micro*, vol. 16, no. 5, pp. 30–39, Oct. 1996.

[20] C. A. Mead, *Analog VLSI and Neural Systems*. Reading, MA: Addison-Wesley, 1989.

[21] S. C. Liu and R. Douglas, "Temporal coding in a silicon network of integrate-and-fire neurons," *IEEE Trans. Neural Netw.*, vol. 15, no. 5, pp. 1305–1314, Sep. 2004.

[22] G. S. Cymbalyuk, G. N. Patel, R. L. Calabrese, S. P. DeWeerth, and A. H. Cohen, "Modeling alternation to synchrony with inhibitory coupling: A neuromorphic VLSI approach," *Neural Comput.*, vol. 12, pp. 2259–2278, 2000.

[23] M. Mahowald and R. Douglas, "A silicon neuron," *Nature*, vol. 354, pp. 515–518, 1991.

[24] D. R. Frey, "Log-domain filtering: An approach to current-mode filtering," *Inst. Electr. Eng. Proc.*, vol. 140, pp. 406–416, 1993.

[25] W. Himmelbauer and A. G. Andreou, "Log-domain circuits in subthreshold MOS," in *Proc. 40th Midwest Symp. Circuits Syst.*, 1997, pp. 26–30.

[26] E. Culurciello, R. Etienne-Cummings, and K. Boahen, "A biomorphic digital image sensor," *IEEE J. Solid State Circuits*, vol. 38, no. 2, pp. 281–294, Feb. 2003.

[27] R. Z. Shi and T. Horiuchi, "A summating, exponentially-decaying CMOS synapse for spiking neural systems," in *Advances in Neural Information Processing Systems*, S. Thrun, L. Saul, and B. Schölkopf, Eds. Cambridge, MA: MIT Press, 2004, vol. 16.

[28] A. G. Andreou and K. A. Boahen, "Translinear circuits in subthreshold MOS," *J. Anal. Integr. Circuits Signal Process.*, vol. 9, pp. 141–166, 1996.

[29] J. V. Arthur and K. Boahen, "Recurrently connected silicon neurons with active dendrites for one-shot learning," in *Proc. Int. Joint Conf. Neural Netw.*, 2004, pp. 1699–1704.

[30] K. Boahen, "A burst-mode word-serial address-event link-I: Transmitter design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 7, pp. 1269–1280, Jul. 2004.

[31] K. Boahen, "A burst-mode word-serial address-event link-II: Receiver design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 7, pp. 1281–1291, Jul. 2004.

[32] K. Boahen, "A burst-mode word-serial address-event link-III: Analysis and test results," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 7, pp. 1292–1300, Jul. 2004.

[33] C. A. Mead and T. Delbruck, "Scanners for visualizing activity of analog VLSI circuitry," *Anal. Integr. Circuits Signal Process.*, vol. 1, pp. 93–106, 1991.
[34] M. Bartos, I. Vida, M. Frotscher, A. Meyer, H. Monyer, J. R. P. Geiger, and P. Jonas, "Fast synaptic inhibition promotes synchronized gamma oscillations in hippocampal interneurons networks," *Proc. Nat. Acad. Sci.*, vol. 99, pp. 13 222–13 227, 2002.
[35] A. Gupta, Y. Wang, and H. Markram, "Organizing principles for a diversity of gabaergic interneurons and synapses in the neocortex," *Science*, vol. 287, pp. 244–246, 2000.
[36] J. M. Goldberg and P. B. Brown, "Responses of binaural neurons to dichotic stimulation," *J. Neurophysiol.*, vol. 32, pp. 940–958, 1969.
[37] T. F. Freund and G. Buzsáki, "Interneurons of the hippocampus," *Hippocampus*, vol. 6, pp. 347–470, 1996.
[38] P. H. E. Tiesinga and J. V. José, "Robust gamma oscillations in networks of inhibitory hippocampal interneurons," *Network: Comput. Neural Syst.*, vol. 11, pp. 1–23, 2000.
[39] W. Gerstner, "Population dynamics of spiking neurons: Fast transients, asynchronous states, and locking," *Neural Comput.*, vol. 12, pp. 43–89, 2000.
[40] A. Destexhe, Z. F. Mainen, and T. J. Sejnowski, "Synthesis of models for excitable membranes, synaptic transmission and neuromodulation using a common kinetic formalism," *J. Comput. Neurosci.*, vol. 1, pp. 195 230–195 230, 1994.

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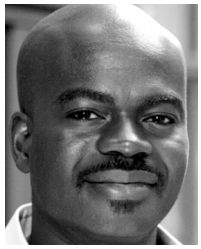

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From 1997 to 2005, he was on the faculty of the University of Pennsylvania, Philadelphia, where he held the Skirkanich Term Junior Chair. Currently, he is an Associate Professor at the Bioengineering Department, Stanford University, Stanford, CA. He is a bioengineer who is using silicon-integrated circuits to emulate the way neurons compute, linking the seemingly disparate fields of electronics and computer science with neurobiology and medicine. His contributions to the field of neuromorphic engineering include a silicon retina that could be used to give the blind sight and a self-organizing chip that emulates the way the developing brain wires itself up. His scholarship is widely recognized, with over 60 publications to his name, including a cover story in the May 2005 issue of the *Scientific American*.

Dr. Boahen has received several distinguished honors, including a Fellowship from the Packard Foundation in 1999, a CAREER award from the National Science Foundation in 2001, a Young Investigator Award from the Office of Naval Research in 2002, and the National Institutes of Health Director's Pioneer Award in 2006. He is a member of Tau Beta Kappa. At Caltech, he held a Sloan Fellowship for Theoretical Neurobiology.