

Calibrating Silicon-Synapse Dynamics using Time-Encoding and Decoding Machines

Eric Kauderer-Abrams and Kwabena Boahen

{ekabrams@stanford.edu, boahen@stanford.edu}

Electrical Engineering and Bioengineering, Stanford University, Stanford, CA, U.S.A

Abstract—We present an approach to mapping synaptic models onto neuromorphic hardware using Time-Encoding and Decoding Machines. This framework allows us to transform a spiking soma-circuit into an analog-to-digital converter (ADC), one for each synapse circuit. We verify that the measurements obtained with these ‘virtual’ ADCs closely match those obtained with an on-chip ADC. Using the massively parallel measurement capability that these virtual ADCs afford us, we demonstrate the first large-scale calibration of synapse circuits’ dynamic parameters. This advance opens the door to programming neuromorphic chips on the more intuitive level of dimensionless models, rather than by setting raw voltage biases, as is currently done.

I. MAPPING DIMENSIONLESS MODELS ONTO SILICON

Neuromorphic engineers have adopted a model-driven approach to current-mode circuit design [1]. Given a dimensionless differential equation modeling the behavior of interest, a subthreshold CMOS circuit is designed in which the model’s state-variable is represented by a current. While this model-driven approach greatly simplifies many aspects of system design and operation, it also introduces a heavy reliance on calibration.

Calibration is necessary because of the large variation in behavior—caused by transistor mismatch—between different copies of the same circuit. On the level of dimensionless models, these variations cause circuits with the same applied biases to exhibit behavior corresponding to different values of the model’s parameters. The relationships between individual circuit’s biases and the model parameters are captured by mapping parameters extracted for each circuit during calibration. Spiking soma circuits have been calibrated by exploiting the relationship between the model parameters and the neuron’s steady-state spike-rate, derived using techniques from dynamical systems theory [2]. However, no such relationship exists for the dynamic parameters of a synapse circuit, thus a new calibration technique is needed.

We present a new approach to calibration that uses Time-Encoding and Decoding machines to endow each synapse circuit with a ‘virtual’ analog-to-digital converter. In our approach, each synapse circuit’s output waveform is captured in a massively parallel fashion, greatly reducing the time required to calibrate the chip. In this paper, we present a refined analysis of the synapse circuit (Section II), a summary of the time-encoding and decoding paradigm and its adaptation to our hardware (Section III), and results obtained from calibrating the dynamic parameters of over 2,000 of Neurogrid’s synapse circuits [3], [4] (Section IV).

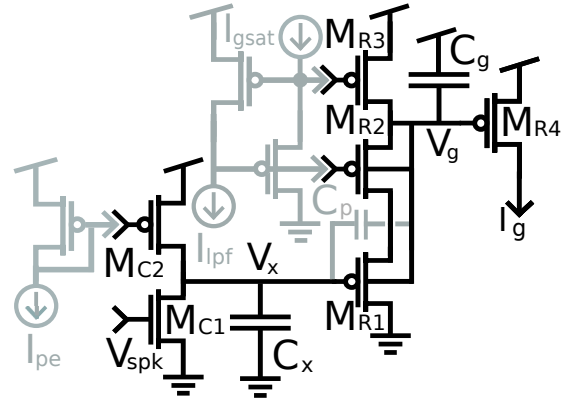


Fig. 1: Synapse circuit with biasing circuitry (gray). M_{C1} and M_{C2} model spike-triggered release and reuptake of neurotransmitter, respectively. M_{R1-3} model receptor-binding and unbinding: M_{R1} discharges C_g to a limit set by M_{R2} and M_{R3} recharges it back up to V_{dd} . M_{R4} produces a current, I_g , that is proportional to the postsynaptic conductance. C_p is a parasitic capacitance that affects the postsynaptic conductance’s time-constant and initial value.

II. SYNAPSE CIRCUIT

The synapse circuit models the release and reuptake of neurotransmitter, triggered by the arrival of a spike (Fig. 1). Its dynamics are described by

$$\tau \dot{g} + g = g_{sat} x_{t_{rise}}(t) + g_0 \delta(t) \quad (1)$$

where τ is the synaptic time-constant, g_{sat} is the maximum conductance, $x_{t_{rise}}(t)$ is a unit-input pulse with duration t_{rise} triggered by a spike, $\delta(t)$, and g_0 is an artifact of the parasitic capacitance. We show how this artifact arises and also demonstrate that $x_{t_{rise}}(t)$ has a step-like rising-edge and a sigmoidal trailing-edge through a refinement of previous analyses [3].

To demonstrate how the synapse circuit implements (1), we derive expressions for the two currents that discharge C_g . We start with I_p , the current across C_p , the capacitor between M_{R1} ’s gate and well. This current, which flows between V_g and V_x , is given by $I_p = C_p \frac{d}{dt}(V_g - V_x)$. Since V_x is the voltage across C_x , which is discharged by the arrival of a spike and recharged by I_{pe} , we have $(C_x + C_p) \dot{V}_x = I_{pe} - (C_x + C_p) V_{dd} \delta(t)$. Substituting this expression into the previous equation yields

$$I_p = C_p \dot{V}_g - p_c I_{pe} + C_p V_{dd} \delta(t) \quad (2)$$

where $p_c = C_p/(C_x + C_p)$. Next, we derive an expression for $I_{in}(t)$, the current conducted by M_{R2} . Applying the translinear principle [5] to M_{R2} 's forward and reverse currents yields an expression that is valid in both the ohmic and saturation regimes

$$I_{in}(t) = \frac{1}{I_g} \left(\frac{1}{I_0^2 e^{\frac{\kappa}{U_T}(V_{dd} - V_x(t))}} + \frac{1}{I_{lpf} I_{gsat}} \right)^{-1} \quad (3)$$

$$= \frac{I_{lpf} I_{gsat}}{I_g} \frac{1}{1 + e^{\frac{\kappa}{U_T}(V_x(t) - V_{gsat})}} \quad (4)$$

where we define $V_{gsat} = V_{dd} - \frac{U_T}{\kappa} \log(I_{gsat} I_{lpf} / I_0^2)$, which equals M_{R2} 's gate-voltage. U_T is the thermal voltage, κ is the subthreshold-slope coefficient, and I_0 is the leakage current of a transistor.

Combining these currents with the current I_{lpf} , which recharges C_g , we obtain

$$C_g \dot{V}_g = I_{lpf} - I_{in}(t) - I_p \quad (5)$$

Substituting (2), (4), and $\dot{V}_g = -(U_T/\kappa I_g) \dot{I}_g$, yields

$$\begin{aligned} \frac{(C_g + C_p)U_T}{\kappa I_{lpf}} \dot{I}_g + \left(1 + p_c \frac{I_{pe}}{I_{lpf}} - \frac{C_p V_{dd}}{I_{lpf}} \delta(t) \right) I_g \\ = \frac{I_{gsat}}{1 + e^{\frac{\kappa}{U_T}(V_x(t) - V_{gsat})}} \end{aligned} \quad (6)$$

after multiplying both sides by $-I_g/I_{lpf}$. Next, we note that $V_x(t) = \frac{I_{pe}}{C_x + C_p} t$ and we define the model-parameter t_{rise} to be the time at which $V_x(t_{rise}) = V_{gsat}$. Thus we obtain

$$\tau \dot{I}_g + I_g = \frac{1}{1 + p_c \frac{I_{pe}}{I_{lpf}}} \frac{I_{gsat}}{1 + e^{\frac{\kappa V_{gsat}}{U_T} \left(\frac{t}{t_{rise}} - 1 \right)}} + Q_c \delta(t) \quad (7)$$

after dividing both sides by $1 + p_c I_{pe}/I_{lpf}$ and defining $\tau = (C_g + C_p)U_T/(\kappa(I_{lpf} + p_c I_{pe}))$ and $Q_c = (I_g(0^+) - I_g(0^-))\tau$. We obtain $I_g(0^+) = I_g(0^-) \exp(\frac{\kappa C_p V_{dd}}{(C_g + C_p)U_T})$ by integrating (6) an infinitesimal time past $t = 0$.

To convert (7) into dimensionless form, we divide both sides by a normalization current, chosen to be the bias I_{lk} of the soma circuit [3], which yields (1) with $g = I_g/I_{lk}$, $g_{sat} = I_{gsat}/I_{lk}$, $g_0 = Q_c/I_{lk}$, and

$$x_{t_{rise}}(t) = \frac{1}{1 + p_c \frac{I_{pe}}{I_{lpf}}} \frac{1}{1 + e^{\frac{\kappa V_{gsat}}{U_T} \left(\frac{t}{t_{rise}} - 1 \right)}} \quad (8)$$

The solution to (1) is given by

$$g(t) = u(t) e^{-\frac{t}{\tau}} * (g_{sat} x_{t_{rise}}(t) + g_0 \delta(t)) \quad (9)$$

where $u(t)$ is the unit-step function (Fig. 2). We fit the model given by (9) to the synapse-circuits' measured outputs to calibrate these circuits.

III. VIRTUAL ANALOG-TO-DIGITAL CONVERTERS

To measure the synaptic waveforms, we employ Time-Encoding and Time-Decoding Machines: a class of asynchronous, nonuniform sampling techniques introduced by Lazar and Toth [6]. Using these methods, we recover the

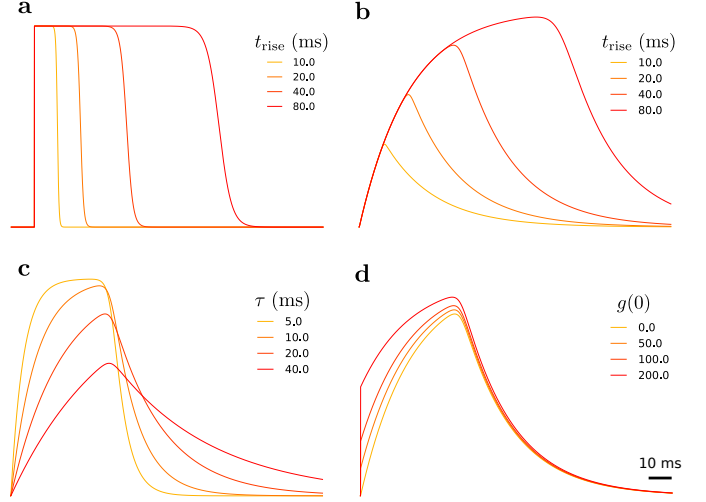


Fig. 2: Synapse circuit's ideal waveforms. **a** $x(t)$'s duration increases and its trailing-edge's slope becomes less steep as t_{rise} increases. **b** $g(t)$'s rising phase lengthens and its peak value increases as t_{rise} increases. **c** $g(t)$'s rising and falling phases becomes less steep and its peak value decreases as τ increases. **d** $g(t)$'s discontinuity (at $t = 0$) and peak value increase as g_0 increases. In **a-d**, the default values are $t_{rise} = 30$ ms, $\tau = 30$ ms, $g_0 = 0$, and $V_{gsat} = 1.1$ V.

synapse circuit's output from the spike-trains of a soma circuit. In this way, we endow each synapse circuit with a 'virtual' analog-to-digital converter (ADC) that can be operated in parallel due to the high-throughput spike-routing architecture of the chip [7].

A. Time-Encoding and Time-Decoding

To time-encode a signal, it is fed into a spike-generator, which encodes the signal-amplitude as a sequence of spike-times. These spike-times are time-decoded to recover the input signal using an algorithm that minimizes a smoothness criterion subject to a set of linear constraints. These constraints on the input signal are derived from the observed sequence of spike-times and the differential equations governing the spike-generator's state-variable [8]. Recoveries are highly accurate given certain Nyquist-like constraints on the input-signal's bandwidth relative to the spike-generator's spike-rate [6], [9].

We now derive a set of linear constraints on the input signal. The first step is to reparameterize the spike-generator by its phase along its limit cycle [10], defined as

$$\theta = t \bmod T \quad (10)$$

where T is the limit-cycle's period. The utility of this reparameterization is evident when we consider the system's response to *weak* perturbations. Such a perturbation, $g(t)$, only manifests as an advance or delay of the phase along the limit cycle [11]. This perturbed phase $\tilde{\theta}$ is described by

$$\frac{d\tilde{\theta}}{dt} = 1 + Z(\tilde{\theta}, b)g(t) \quad (11)$$

where $Z(\theta)$ is the spike-generator's infinitesimal Phase Response Curve (PRC). It describes the phase change that an

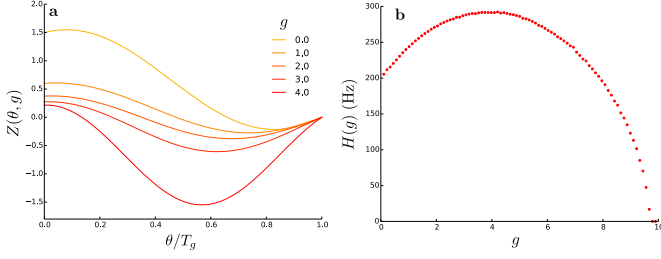


Fig. 3: **a**, **b** Dependence of QIF neuron’s phase-response $Z(\theta, g)$ and steady-state spike-rate $H(g)$ on its input conductance g ; $T(g)$ is the corresponding period. in **a**, $e_{\text{rev}} = 7$, $x_0 = 4$, and $\tau_{\text{soma}} = 4$ ms; in **b**, $e_{\text{rev}} = 2$, $x_0 = 3$, and $\tau_{\text{soma}} = 5$ ms.

impulse evokes as a function of the phase at which the impulse was received. The conditional form, $Z(\theta, b)$, captures how the PRC changes as a function of the input level b .

If $g(t)$ is not weak, we re-write it as a weak deviation $v(t)$ from a constant value g_k that corresponds to $g(t)$ ’s mean over the interspike interval $[t_k, t_{k+1}]$. That is

$$g(t) = v(t) + \sum_{k=0}^{M-2} \mathbb{1}_{[t_k, t_{k+1}]}(t)g_k \quad (12)$$

where M is the number of spikes. We obtain g_k by inverting the spike-generator’s transfer-function, $H(g)$. Defining $H^{-1}(f)$ to be the input value g that causes the spike-generator to spike at rate f , we estimate $\hat{g}_k = H^{-1}(f_k)$ where $f_k = 1/(t_{k+1} - t_k)$ is the instantaneous spike-rate. For small interspike intervals and $g(t)$ of sufficiently low bandwidth, $v(t)$ is weak enough that (11) is valid.

The next step is to use (11) to obtain a linear constraint on the input-signal’s value $g(t)$ during each interspike interval. Replacing $g(t)$ in (11) with $v(t)$, and b with g_k , and integrating over the interspike interval $[t_k, t_{k+1}]$ yields

$$\int_{t_k}^{t_{k+1}} d\tilde{\theta} = \int_{t_k}^{t_{k+1}} 1 + Z(\tilde{\theta}, \hat{g}_k)v(t)dt \quad (13)$$

We note that, over each interspike interval, $\tilde{\theta}$ begins at zero and ends at T_k , the instantaneous period of the spike-generator. Following [8], we make the approximation $Z(\tilde{\theta}, \hat{g}_k) \approx Z(t, \hat{g}_k)$ and re-express $v(t)$ in terms of $g(t)$ and g_k . Thus,

$$T_k = t_{k+1} - t_k + \int_{t_k}^{t_{k+1}} Z(t, \hat{g}_k)(g(t) - \hat{g}_k)dt \quad (14)$$

We define the constant $\chi_k = \int_{t_k}^{t_{k+1}} Z(t, \hat{g}_k)\hat{g}_k dt$, and note that $T_k = (t_{k+1} - t_k)$, since we estimated \hat{g}_k from the perturbed period. This yields a linear constraint on $g(t)$:

$$\frac{1}{\chi_k} \int_{t_k}^{t_{k+1}} Z(t, \hat{g}_k)g(t)dt = 1 \quad (15)$$

Finally, we cast the set of constraints given by (15) into matrix form. We define $Z[i; \hat{g}_k]$ and $g[i]$, for $0 \leq i < N$, to be $Z(t, \hat{g}_k)$ and $g(t)$ discretized over the interval $[0, t_{\text{max}}]$ with a

timestep Δ . We define the matrix $\mathbf{A} \in \mathbb{R}^{M \times N}$ whose $(k, i)^{\text{th}}$ element is given by

$$a_{ki} = \frac{1}{\chi_k} \mathbb{1}_{[\frac{t_k}{\Delta}, \frac{t_{k+1}}{\Delta}]}[i]Z[i; \hat{g}_k]\Delta \quad (16)$$

With these definitions, (15) is expressed by $\mathbf{A}\mathbf{g} = \mathbb{1}$, where \mathbf{g} has elements $g[i]$ and $\mathbb{1}$ has elements 1. This equation has many solutions because, in general, $M < N$. Among these solutions, we choose the one that satisfies

$$\text{minimize} \int_0^{t_{\text{max}}} \left\| \frac{\partial^2 g}{\partial t^2} \right\|^2 dt, \text{ subject to } \mathbf{A}\mathbf{g} = \mathbb{1} \quad (17)$$

thereby minimizing a second-order smoothness constraint [9].

B. QIF Neuron’s Phase-Response Curve

In order to obtain \mathbf{A} (see (16)) for our soma circuit, we derive its PRC, $Z(\theta, g)$, and measure its transfer function, $H(g)$, which maps constant synaptic inputs to steady-state spike-rates. The soma circuit implements a leaky quadratic-integrate-and-fire (QIF) model with conductance-based synapses. Its membrane voltage $v(t)$ is governed by

$$\tau_{\text{soma}} \frac{dv}{dt} = \frac{1}{2}v^2 - v + g(t)(e_{\text{rev}} - v) + x_0 \quad (18)$$

where τ_{soma} is its membrane’s time-constant, $g(t)$ is its synapse’s conductance, e_{rev} is this conductance’s reversal potential, and x_0 is a constant-current input.

To compute the PRC, we apply the adjoint method [12] to (18) and derive the analytical expression

$$Z(\theta, g) = \frac{2}{c^2}(e_{\text{rev}} - a) \cos^2(\beta\theta - \gamma) - \frac{c}{2} \sin(2\beta\theta - \gamma) \quad (19)$$

where $a = 1 + g$, $c = \sqrt{2e_{\text{rev}}x_0 - a^2}$, $\beta = \frac{2}{c\tau_{\text{soma}}}$, and $\gamma = \tan^{-1}(a/c)$ (Fig. 3a). To obtain the values of e_{rev} , x_0 , and τ_{soma} for each soma circuit, we use calibrated mapping parameters obtained through a previously described procedure [2].

To measure $H(g)$ for a particular soma circuit, we send spikes from the PC to its synapse-circuit at a rate sufficiently high to saturate its synapse circuit’s output at its maximum value g_{sat} . We sweep g_{sat} over a wide range and record the soma’s spike-rate for each value of g_{sat} (Fig. 3b).¹

To validate the recovery algorithm, we compare its recoveries of $g(t)$ with measurements taken with an on-chip ADC (Fig. 4). We observe a close match between these two measurements.²

IV. CALIBRATION PROCEDURE AND RESULTS

To calibrate the synapse-circuit’s dynamic parameters, we relate them to their respective biases:

$$t_{\text{rise}} = \frac{C_{\text{trise}}V_{\text{gsat}}}{I_{\text{pe}} + I_1} \quad \text{and} \quad \tau = \frac{Q\tau}{I_{\text{lpf}} + p_c I_{\text{pe}} + I_2} \quad (20)$$

¹Although $H(g)$ can be computed analytically [3], it is more accurate to measure it empirically as hourly temperature variation can cause the actual $H(g)$ curve to deviate from its ideal form.

²The recovered waveforms exhibit ripples due to quantization of the spike-times (50 μs resolution).

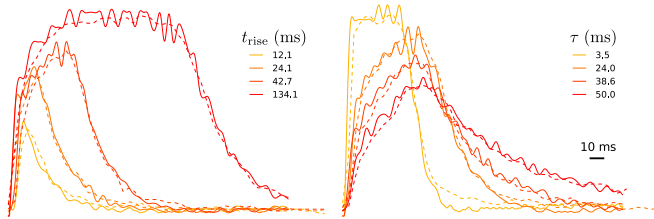


Fig. 4: The synapse-circuit’s conductance $g(t)$ measured with the on-chip ADC (dashed lines) and recovered with Time-Encoding and Decoding machines (solid lines) for several values of t_{rise} and τ . The default parameters values are $t_{\text{rise}} = 42.7$ ms and $\tau = 24.0$ ms

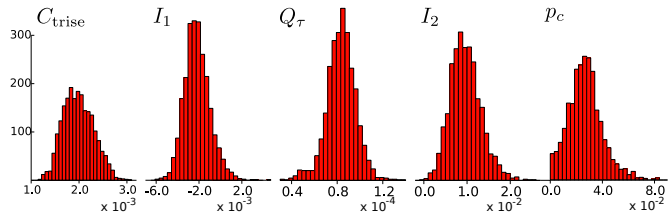


Fig. 5: Distributions of calibrated mapping parameters for 2,264 synapse circuits (12 outliers not shown). The mapping parameters’ magnitudes are determined by arbitrary DAC units.

where we define the mapping parameters $C_{\text{trise}} = C_x + C_p$, $Q_\tau = (C_g + C_p)U_T/\kappa$, $p_c = C_p/(C_x + C_p)$, I_1 and I_2 . The latter two are leakage currents in parallel with I_{pe} and I_{lpf} , respectively. We substitute (20) into (9) to relate the synapse-circuit’s output $g(t)$ to its mapping parameters

$$g(t) = \left(\frac{1}{1 + p_c \frac{I_{\text{pe}}}{I_{\text{lpf}}}} \frac{1}{1 + e^{-\frac{\kappa V_{\text{gsat}}}{U_T} \left(\frac{I_{\text{pe}} + I_1}{C_{\text{trise}} V_{\text{gsat}}} t - 1 \right)}} + g_0 \delta(t) \right) * u(t) e^{-\frac{I_{\text{lpf}} + p_c I_{\text{pe}} + I_2}{Q_\tau} t} \quad (21)$$

We fit this expression to recoveries of $g(t)$ —obtained using Time-Encoding and Decoding Machines—for many combinations of the biases I_{pe} and I_{lpf} .³ These fits yielded values for C_{trise} , Q_τ , p_c , I_1 , I_2 , and g_0 for 2,264 synapse circuits (Fig. 5).

With calibrated mapping parameters in hand, we can now program each synapse circuit on the more intuitive level of its dimensionless model’s parameters (Fig. 6). Given desired values of t_{rise} and τ for each synapse circuit, we substitute its mapping parameters into (20), solve for the corresponding values of the biases I_{pe} and I_{lpf} , and program its digital-to-analog converter (DAC) accordingly. In cases where a single DAC is shared by a population of synapse circuits, as in Neurogrid, we use the median values of the mapping parameters’ distributions [4].

³For each set of values of I_{pe} and I_{lpf} , a spike is sent from the PC to the synapse circuit, which causes the soma circuit to generate spikes. We time-decode these spikes to recover $g(t)$. In order to ensure accurate recovery, we set the soma’s parameters (x_0 , e_{rev} , and τ_{soma}) such that its free-running spike-rate is approximately 200 Hz. We also set g_{sat} so as to operate on the monotonically-increasing segment of the soma-circuit’s transfer function $H(g)$ (see Fig. 3).

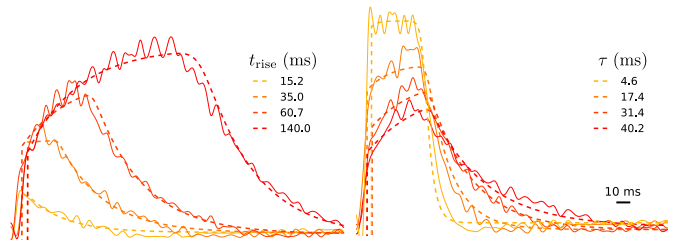


Fig. 6: Calibration results: Expected (dashed lines) and measured (solid lines) synaptic conductances closely match, validating that mapping parameters were accurately calibrated. The fitted values were $1.01t_{\text{rise}}$ and 1.03τ , an accuracy of 1 to 3%.

V. SUMMARY

We presented a fast, accurate method for calibrating synapse circuits’ dynamic parameters. In our approach, we use a soma circuit to time-encode a synapse circuit’s output. We then time-decode the soma circuit’s spike-train to recover the synapse circuit’s output. The recoveries closely matched measurements obtained using the on-chip ADC, and enabled us to acquire synapse waveforms in a massively parallel fashion. We fit these recovered waveforms to a refined model of the synapse circuit’s behavior (9). The mapping parameters obtained with this calibration procedure yield accurate predictions of the synapse-circuit’s behavior.

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