

An ON–OFF Log Domain Circuit That Recreates Adaptive Filtering in the Retina

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Abstract—We introduce a new approach to synthesizing Class AB log-domain filters that satisfy dynamic differential-mode and common-mode constraints simultaneously. Whereas the dynamic differential-mode constraint imposes the desired filtering behavior, the dynamic common-mode constraint solves the zero-dc-gain problem, a shortcoming of previous approaches. Also, we introduce a novel push–pull circuit that serves as a current-splitter; it rectifies a differential signal into the ON and OFF paths in our log-domain filter. As an example, we synthesize a first-order low-pass filter, and, to demonstrate the rejection of dc signals, we implement an adaptive filter by placing this low-pass circuit in a variable-gain negative-feedback path. Feedback gain is controlled by signal energy, which is extracted simply by summing complementary ON and OFF signals—dc signals do not contribute to the signal energy nor are they amplified by the feedback. We implement this adaptive filter design in a silicon chip that draws biological inspiration from visual processing in the mammalian retina. It may also be useful in other applications that require dynamic time-constant adaptation.

Index Terms—Adaptive filtering, artificial vision, class AB circuits, neuromorphic engineering.

I. LOG-DOMAIN FILTERING

DECREASING supply voltage with integrated circuit miniaturization is increasing interest in current-mode filters. Current-mode operation offers large dynamic range if the nonlinear device transconductance is compensated for in the filter design, such that operation remains linear outside the small-signal region. The existence of such externally linear but internally nonlinear filters was demonstrated by Adams, who first designed a circuit that “when placed between a log converter and an anti-log converter will cause the system to act as a linear filter” [1]. He named these circuits *log-domain* filters. The log and anti-log operations are readily realized using bipolar transistors or MOSFETs operating in weak inversion; these devices maintain logarithmic voltage-current relationships over six decades.

The principle of log-domain filter design is a simple one: use current to represent the signal x , voltage to represent its logarithm $\log(x)$, and note that $d\log(x)/dt = (1/x)dx/dt$. There-

fore, to obtain the derivative of the voltage, divide the derivative of the signal, dx/dt , by the signal, x . That is to say, divide the current you wish to supply to the capacitor by the current made by the transistor whose gate (or base) is connected to it. Intuitively, this division compensates for the slope of the exponential at the transistor’s operating point, such that its current changes at a constant rate. Current-division is readily realized with logarithmic elements by exploiting the translinear principle [8].

In theory, log-domain filters have limitless dynamic range; in practice, dynamic range is limited by the bias current. Seevinck and Frey have both proposed Class AB log-domain filters that address this shortcoming; they both use two copies of the log-domain circuit to filter the differential signal [7], [12]. In Seevinck’s approach, the outputs are cross coupled, each subtracting current from the others capacitor. In Frey’s approach, a current-splitter, which receives a bidirectional input current, is placed up front; it enforces a geometric mean constraint. Unfortunately, both designs suffer from distortion when the filter’s transfer function has zero gain at dc, or close to zero, due to a reduction in bandwidth and to offsets introduced by leakage currents.

In this paper, we introduce a new approach to synthesizing Class AB log-domain filters. Our synthesis procedure satisfies dynamic differential-mode and common-mode constraints simultaneously. Whereas the dynamic differential-mode constraint imposes the desired filtering behavior, as in the approaches of Frey and Seevinck [7], [12], the dynamic common-mode constraint solves the zero-dc-gain problem, a shortcoming of their approaches. Specifically, we introduce a second differential equation, with its own time-constant, that imposes the desired common-mode behavior, and, in particular, we find that imposing a geometric mean constraint that is satisfied with the same time-constant that describes differential behavior results in the simplest implementation.

The remainder of this paper is organized as follows. In Section II, we introduce a novel push–pull circuit that serves as a current-splitter in our log-domain filters; it rectifies a differential signal into ON and OFF paths. In Section III, taking these complementary signals as input, we synthesize a low-pass ON–OFF log-domain filter that constrains the geometric mean of its outputs dynamically. In Section IV, taking inspiration from the retina, we realize an adaptive filter by placing our ON–OFF log-domain low-pass in a variable-gain negative-feedback path. Feedback gain is controlled by signal energy, which is extracted simply by summing complementary ON and OFF signals. This application demonstrates the rejection of dc signals—they are not amplified in the feedback path nor do they contribute to the signal energy. Section V concludes the paper.

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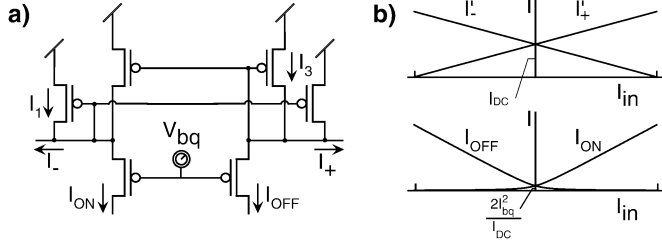


Fig. 1. Half-wave rectification. (a) Circuit implementation of half-wave rectification. Two currents I_+ and I_- are compared to one another. Both currents are mirrored on to one another, eliminating most of the common mode (i.e., dc) current and driving subsequent circuitry with the differential signals, I_{ON} and I_{OFF} . V_{bq} determines the level of residual dc signal present in I_{ON} and I_{OFF} . Additional copies of I_{ON} and I_{OFF} can be made to drive subsequent circuitry by connecting additional transistors in parallel. (b) In a purely differential representation, the difference between I_+ and I_- , I_{in} , is encoded as the difference between I'_+ and I'_- (top). In the ON-OFF representation, one signal or the other is active, depending on the sign of the difference between the input signals (bottom). When $I_+ = I_-$, residual dc currents are inversely proportional to the common-mode input, I_{DC} . Tick marks on the horizontal axis of both graphs represent units of I_{DC} .

II. ON-OFF RECTIFICATION

To construct our class AB log-domain filter, we first construct a circuit to divide input signals into complementary ON and OFF paths. Taking inspiration from Frey's current-splitter [7], we subtract the two input currents and completely divert the difference to the ON or OFF path based on its sign.

A. Implementation

We implement rectification using the circuit shown in Fig. 1(a). This circuit is similar to that proposed in [14], but the analysis presented in that paper includes effects of κ , which we ignore here. The circuit takes two input signals, I_+ and I_- , on either side, and compares them to one another. In our application (*see* Section IV-A), these currents represent a signal and its mean, such that current is diverted to either the ON or OFF pathways based on whether the signal lies above or below its mean. We define a current $I_{bq}^2 = I_o^2 e^{-V_{bq}/U_T}$ that sets the residual current level and assume a unity subthreshold slope coefficient (i.e., $\kappa = 1$). Hence, the currents in the current mirror can be expressed as $I_1 = I_{bq}^2/I_{ON}$ and $I_3 = I_{bq}^2/I_{OFF}$. Equating these currents to the input and output currents, we find

$$I_{ON} + I_- = \frac{I_{bq}^2}{I_{ON}} + \frac{I_{bq}^2}{I_{OFF}} = I_{OFF} + I_+ \quad (1)$$

assuming subthreshold operation ($I_{DS} = I_o e^{\kappa V_G/U_T} (e^{-V_S/U_T} - e^{-V_D/U_T})$, where $U_T = 25$ mV at room temperature and $\kappa \approx 0.7$, and where signs reverse for pMOS, referenced to V_{dd}) and saturation ($V_{DS} > 4U_T$). We can solve these equations for I_{ON} and I_{OFF} as a function of I_+ , I_- , and I_{bq}^2 . We note that mirroring the input currents on to one another preserves their differential signal, $I_+ - I_-$, which equals $I_{ON} - I_{OFF}$. In our ON-OFF circuit, I_{bq} imposes a common-mode constraint on the output currents I_{ON} and I_{OFF} through (1).

To determine the behavior of these ON-OFF signals subject to this I_{bq} constraint, we observe that (1) implies

$$I_{ON} + I_{OFF} + I_+ + I_- = 2I_{bq}^2 \left(\frac{1}{I_{ON}} + \frac{1}{I_{OFF}} \right).$$

Replacing the sum of I_+ and I_- with $2I_{DC}$, where I_{DC} is the common-mode input signal, we have

$$I_{ON}I_{OFF} = \frac{2I_{bq}^2}{\frac{1+2I_{DC}}{I_{ON}+I_{OFF}}}. \quad (2)$$

Thus, the geometric mean of I_{ON} and I_{OFF} is strictly less than $\sqrt{2}I_{bq}$. If $I_{OFF} \gg I_{bq}$, then $I_{ON} \ll I_{bq}$. Conversely, if $I_{ON} \gg I_{bq}$, then $I_{OFF} \ll I_{bq}$. Consequently, $I_{OFF} \approx I_- - I_+$ and $I_{ON} \approx 0$ in the first case, while $I_{ON} \approx I_+ - I_-$ and $I_{OFF} \approx 0$ in the second case. We can see that the circuit rectifies its inputs around a level determined by I_{bq} . Hence, once I_- exceeds I_+ by several I_{bq} , current is diverted entirely through the OFF path. Conversely, once I_+ exceeds I_- by several I_{bq} , current is diverted entirely through the ON path. Whereas a conventional differential circuit would maintain current in both paths (Fig. 1(b), *top*), our ON-OFF design maintains current in only one path as shown in the analytical solution presented in the bottom of Fig. 1(b).

We can also determine the predicted quiescent level I_q of I_{ON} and I_{OFF} when $I_+ = I_- = I_{DC}$, which represents the common-mode input current level, from (2)

$$I_{ON}I_{OFF} = \frac{2I_{bq}^2}{\frac{1+I_{DC}}{I_{ON}+I_{OFF}}} \quad (3)$$

$$I_q + I_{DC} = 2 \frac{I_{bq}^2}{I_q} \Rightarrow I_q \approx \frac{2I_{bq}^2}{I_{DC}} \quad (4)$$

when $I_{DC} \gg I_q$. Hence, the common-mode rejection in our ON-OFF circuitry is in fact not complete. Its outputs contain a residual dc component that is linearly proportional to $e^{-V_{bq}}$ and inversely proportional to the common-mode input signal, as shown in Fig. 1(b).

Finally, because we have assumed the transistors are in saturation, our results do not apply to input currents $I_+, I_- > I_o e^{-\kappa(V_{bq}+4U_T)/U_T}$, or $I_+, I_- > I_{bq}^2/100I_o$ (since $e^{4\kappa} \approx 100$ and $I_{bq}^2 = I_o^2 e^{-V_{bq}/U_T}$). For currents above this level, the current mirrors' output transistors enter the ohmic region, and hence I_{ON} and I_{OFF} start leveling off. The maximum level they can achieve is I_{bq}^2/I_o .

B. Simulation Results

To verify our rectifying ON-OFF design, we simulated the circuit of Fig. 1(a) by sweeping the dc currents at I_+ and I_- and recording the outputs, I_{ON} and I_{OFF} ¹. We show the relationship between the output currents, I_{ON} and I_{OFF} , and the differential input, $I_+ - I_-$ in Fig. 2, *top*. From the figure, we see that our simulation results replicate the theoretical prediction shown in Fig. 1(b). Specifically, as the difference $I_+ - I_-$ increases,

¹In this, and other simulations presented later, we use Tanner Tools T-Spice to simulate our circuits. We use the model file for the TSMC 0.35 μm fabrication process, SPICE 3f5 Level 5, HSPICE Level 49, UTMOST Level 8, released by MOSIS May 17, 2000.

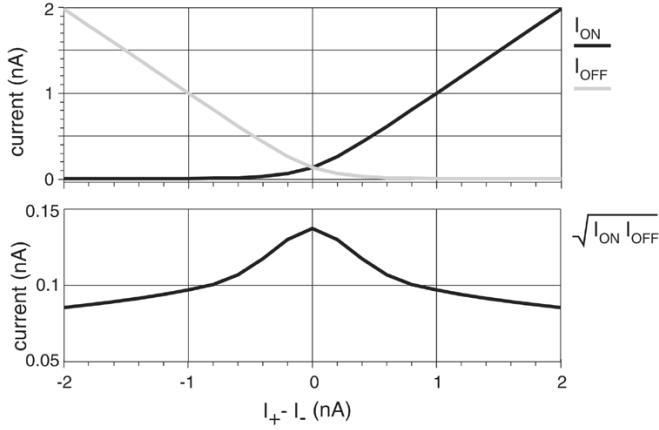


Fig. 2. Rectification circuit simulation. Simulation results for the rectifying circuit of Fig. 1 demonstrating the relationship between I_{ON} and I_{OFF} and $I_+ - I_-$ (top). The geometric mean of I_{ON} and I_{OFF} is also shown as a function of $I_+ - I_-$ (bottom). Circuit parameters: $V_{bq} = 2.2$ V, $V_{dd} = 3.3$ V.

current is diverted to the ON path, while decreasing the difference $I_+ - I_-$ causes current to be diverted to the OFF path. In both cases, as soon as the difference in input exceeds even just 1 nA, current is virtually diverted to one path. Furthermore, we also see from the simulation results that when the difference between input currents is very small, the circuit maintains a small residual common-mode current in both paths. The level of this current, as shown above, depends on V_{bq} . Hence, our rectification is soft, and can be made softer by decreasing V_{bq} .

To demonstrate the constraint imposed by I_{bq} on our circuit, we also plotted how the geometric mean of the output currents, $\sqrt{I_{ON}I_{OFF}}$, depends on the difference in input currents, $I_+ - I_-$. We find that $\sqrt{I_{ON}I_{OFF}}$ is indeed small for all $I_+ - I_-$ and rises around the region where $I_+ \approx I_-$ (Fig. 2, bottom). Because the common-mode output, $I_{ON} + I_{OFF}$, is minimum at this point, thereby maximizing the denominator in (3), our analysis predicts that $\sqrt{I_{ON}I_{OFF}}$ should actually fall in this region. This may be because we ignore κ in our analysis. A closer look at the circuit diagram of Fig. 1(a) reveals that as the input voltage falls on one side of the circuit, the output on that side decreases faster than the output on the other side increases. κ 's effect on our circuit causes the source voltage on the one side of the circuit to have a stronger effect on output current than the gate voltage on the complementary side. Thus, if we increase I_+ away from $I_+ \approx I_-$, for example, we find that the ON current increases slower than the OFF current decreases. Hence, we find a slight decrease in $\sqrt{I_{ON}I_{OFF}}$. The converse is true if we move in the other direction away from $I_+ \approx I_-$.

III. ON-OFF LOW-PASS FILTER

We present our class AB log-domain filter synthesis procedure using a first-order low-pass filter as an example. The time-domain equations that govern the inputs and outputs of this circuit are

$$I_t = \tau_n \frac{\partial I_n}{\partial t} + I_n \quad (5)$$

where τ_n is the time constant. I_t and I_n are the input and output signals.

A. Synthesis Procedure

Our circuit design is based on the log-domain filtering approach [7], [12]. To derive the circuit, first we implement complementary signaling by representing all signals differentially. Thus, (5) becomes

$$\tau_n \frac{\partial(I_n^+ - I_n^-)}{\partial t} = (I_t^+ - I_t^-) - (I_n^+ - I_n^-) \quad (6)$$

where I_t^+ and I_n^+ are the ON input and output currents, I_t^- and I_n^- are the OFF input and output currents. In subthreshold, these currents are an exponential function of their gate voltages (e.g., $I_n^+ = I_0 e^{\kappa V_n^+ / U_T}$) and so (6) becomes

$$\tau_n \frac{\kappa}{U_T} \left(I_n^+ \frac{\partial V_n^+}{\partial t} - I_n^- \frac{\partial V_n^-}{\partial t} \right) = (I_t^+ - I_t^-) - (I_n^+ - I_n^-). \quad (7)$$

Second, we force the ON and OFF outputs, I_n^+ and I_n^- , to satisfy a geometric mean constraint, implementing this dynamically. Thus, the product of their currents always equals I_q^2 , which sets quiescent output activity. This relationship is also governed by its own time constant, τ_c , and so we derive the second equation for our filter

$$\tau_c \frac{\partial I_n^+ I_n^-}{\partial t} = I_q^2 - I_n^+ I_n^-.$$

Expanding the derivative using the same subthreshold voltage-current relationship as above, we find that

$$\tau_c \frac{\kappa}{U_T} \left(\frac{\partial V_n^-}{\partial t} + \frac{\partial V_n^+}{\partial t} \right) = \frac{I_q^2}{I_n^+ I_n^-} - 1. \quad (8)$$

If we express both τ_n and τ_c in terms of actual capacitances and bias currents ($\tau_n = (C_n U_T / \kappa I_n)$, $\tau_c = (C_c U_T / \kappa I_c)$), (7) and (8) become

$$\frac{C_n}{I_n} \left(I_n^+ \frac{\partial V_n^+}{\partial t} - I_n^- \frac{\partial V_n^-}{\partial t} \right) = (I_t^+ - I_t^-) - (I_n^+ - I_n^-) \quad (9)$$

$$\frac{C_c}{I_c} \left(\frac{\partial V_n^-}{\partial t} + \frac{\partial V_n^+}{\partial t} \right) = \frac{I_q^2}{I_n^+ I_n^-} - 1. \quad (10)$$

Substituting (10) into (9) to eliminate V_n^- , we find that

$$\begin{aligned} \frac{C_n}{I_n} (I_n^+ + I_n^-) \frac{\partial V_n^+}{\partial t} \\ = \frac{I_c C_n}{I_n C_c} \left(\frac{I_q^2}{I_n^+ - I_n^-} \right) + (I_t^+ - I_t^-) - (I_n^+ - I_n^-). \end{aligned}$$

If we assume that the two time constants, τ_n and τ_c , are equal, we can take advantage of the fact that $I_c / C_c = I_n / C_n$. Thus, we define $C_n = C_c = C$ and $I_n = I_c = I_\tau$, where C and I_τ determine the filter's time constant for both common-mode and differential signals. The equation then simplifies to

$$C \frac{\partial V_n^+}{\partial t} = \frac{I_\tau}{I_n^+ + I_n^-} \left[(I_t^+ - I_t^-) - \left(\frac{I_n^+ - I_q^2}{I_n^+} \right) \right]. \quad (11)$$

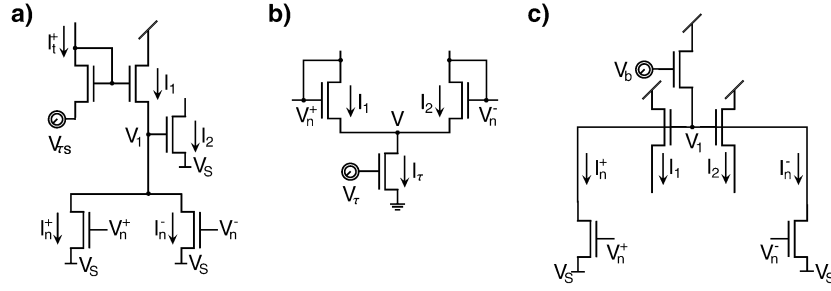


Fig. 3. ON-OFF temporal filter subcircuits. (a) Subcircuit used to compute $I_2 = (I_\tau / (I_n^+ + I_n^-)) I_t^+$. I_2 is subsequently used to excite the positive output node, V_n^+ , and to inhibit the negative output node, V_n^- . (b) Subcircuit used to inhibit the positive output node, V_n^+ , with $I_1 = (I_\tau / (I_n^+ + I_n^-)) I_t^+$, and to inhibit the negative output node, V_n^- , with $I_2 = (I_\tau / (I_n^+ + I_n^-)) I_n^-$. (c) Subcircuit used to excite the positive output node with $(I_\tau / (I_n^+ + I_n^-)) (I_2^q / I_n^+)$ and to excite the negative output node with $(I_\tau / (I_n^+ + I_n^-)) (I_2^q / I_n^-)$.

Similarly

$$C \frac{\partial V_n^-}{\partial t} = \frac{I_\tau}{I_n^+ + I_n^-} \left[(I_t^- - I_t^+) - \left(\frac{I_n^- - I_q^2}{I_n^-} \right) \right]. \quad (12)$$

A CMOS circuit that is described by (11) and (12) will realize the computations needed to implement low-pass filtering in our push-pull model. By dividing the right-hand sides into two current terms that charge or discharge the filter's capacitors (i.e., V_n^+ and V_n^-), we can derive the subcircuits that will realize these computations.

B. Implementation Procedure

Starting with the first term on the right of the equations, we construct the subcircuit shown in Fig. 3(a). Current entering this subcircuit I_t^+ is modulated through a tilted nMOS mirror that generates the current I_1 . For simplicity, we ignore κ and express all voltages in units of the thermal voltage, U_T . Thus

$$I_1 = I_t^+ e^{V_{\tau s} - V_1}.$$

By setting this current, I_1 , equal to the sum of the positive and negative output currents, I_n^+ and I_n^- , we can show that the current I_2 in Fig. 3(a) is equal to the I_t^+ terms in (11) and (12). Specifically

$$I_2 = I_0 e^{V_1 - V_S} = \frac{I_t^+ I_0 e^{V_{\tau s} - V_S}}{I_n^+ + I_n^-}.$$

By setting $V_{\tau s} = V_S + V_\tau$, the current I_2 , which we use to charge up V_n^+ , equals $I_t^+ I_\tau / (I_n^+ + I_n^-)$. An identical circuit on the negative side of the circuit generates a current $I_t^- I_\tau / (I_n^+ + I_n^-)$. Taking the difference between these two currents with a current mirror (shown in Fig. 4) yields the first terms of (11) and (12). A bias V_{os} at the source this current mirror keeps the drain voltages of the current mirror's transistors similar, insuring that excitation on to one side of the circuit is matched by equal inhibition from the complementary side.

The first part of the second term of (11) and (12) represents a leakage current. We implement this using a current divider that links ON and OFF sides of the circuit, as shown in Fig. 3(b). The current drawn through both sides, I_τ , is equal to $I_0 (e^{V_n^+ - V} +$

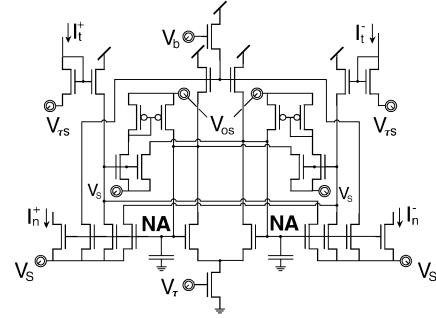


Fig. 4. Log-domain low-pass filter. The complete log-domain low-pass filter circuit that implements (11) and (12). The differential signals, I_t^+ and I_t^- , are inputs to the circuit, which produces the differential signals, I_n^+ and I_n^- , at its output.

$e^{V_n^- - V}$). Hence, the current on one side of the current divider, I_1 , is

$$I_1 = I_0 e^{V_n^+ - V} = \frac{I_\tau I_n^+}{I_n^+ + I_n^-}.$$

This current drains charge away from the capacitor on the positive side of the circuit, and a complementary current drains charge from the capacitor on the negative side of the circuit. Hence, the first part of the second term of (11) and (12) is satisfied.

Finally, the second term of (11) and (12) includes a second current that is dependent on the quiescent activity, I_q^2 , which determines total output activity by charging both capacitors. The subcircuit that realizes this term is shown in Fig. 3(c). Current through the nMOS transistor gated by V_b is equal to the sum of the positive and negative output currents. Hence

$$e^{V_1} = \frac{I_0 e^{V_b}}{I_n^+ + I_n^-}.$$

This node V_1 gates two nMOS transistors that dump current back on to the capacitors (V_n^+ and V_n^-). On the positive side, this current is given by

$$I_1 = I_0 e^{V_1 - V_n^+} = \frac{I_0^2 e^{V_b}}{I_n^+ + I_n^-} e^{-V_n^+}.$$

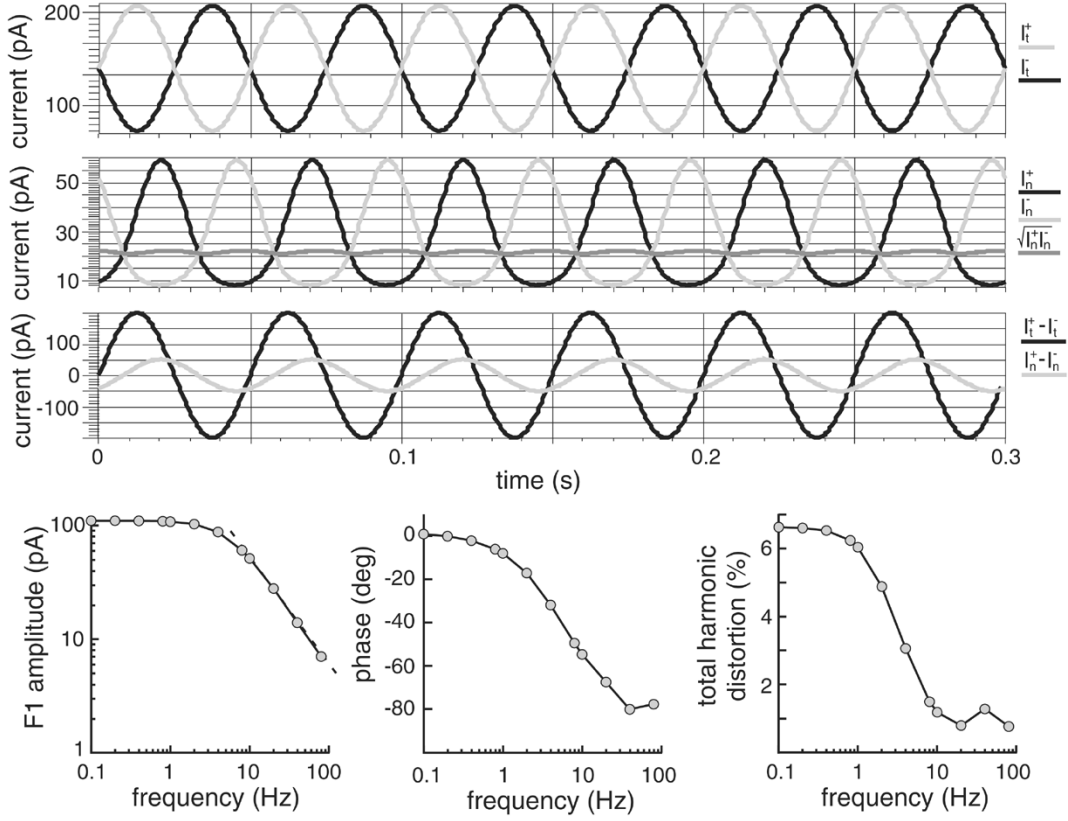


Fig. 5. Low-pass filter simulation. Low-pass filter simulation results with differential inputs I_t^+ and I_t^- (top trace). The differential outputs are I_n^+ and I_n^- (middle trace). We also show the square root of the product of these signals (middle trace) to verify the geometric mean constraint. Comparing the purely differential signals $I_t^+ - I_t^-$ and $I_n^+ - I_n^-$ demonstrates a 60° phase shift at 10 Hz (bottom trace). The amplitude and phase of the first Fourier component of $I_n^+ - I_n^-$, as well as the total harmonic distortion, are shown at different input frequencies (bottom). Dashed line on left curve indicates a one decade per decade slope. Circuit parameters: $V_\tau = 50$ mV, $V_S = 0.4$ V, $V_{\tau s} = 0.583$ V, $V_b = 1.4$ V, $V_{os} = 1.5$ V, $C = 1$ pF.

If we set $V_b = V_q + V_S + V_\tau$, then this current charging V_n^+ becomes

$$I_1 = \frac{I_\tau}{I_n^+ + I_n^-} \frac{I_0^2 e^{V_q}}{I_n^+}.$$

By defining the current I_q^2 as $I_0^2 e^{V_q}$, this current satisfies the last term of (11). A complementary current charges the negative capacitor. By combining these three subcircuits, we realize all the terms in (11) and (12), yielding the complete log-domain low-pass filter circuit shown in Fig. 4.

C. Simulation Results

To verify our ON-OFF low-pass filter implementation, we simulated the synthesized circuit, shown in Fig. 4, which satisfies (11) and (12). We provided two 100-pA peak-to-peak sinusoidal currents 180° out of phase with one another, centered around a mean of 110 pA, at the circuit inputs, I_t^+ and I_t^- . We measured I_n^+ and I_n^- in simulation and took the difference between them at different input frequencies to determine how well our design would filter high frequencies and to determine the amount of distortion created by our circuit.

The time-domain response of this circuit to 10-Hz inputs is shown in the top of Fig. 5. The differential inputs, I_t^+ and I_t^- , yield differential outputs, I_n^+ and I_n^- , that lag behind the input by roughly 60° . This relationship is best demonstrated when comparing the difference $I_t^+ - I_t^-$ to the difference $I_n^+ - I_n^-$.

Because, by design, we constrain the product of ON and OFF output activity with I_q^2 , we also show the geometric mean of the output currents, I_n^+ and I_n^- . We see that the geometric mean is relatively flat and only dips slightly when activity switches from one side of the circuit to the other.

The Fourier amplitude and phase of the circuit's differential output, $I_n^+ - I_n^-$, at different input frequencies is shown in Fig. 5 (bottom). We see that our push-pull log-domain circuit essentially implements a first-order low-pass filter whose corner frequency is ~ 8 Hz. This corner frequency is defined by the filter's time constant, which is determined by C and I_τ . In our simulation, we used values of $C = 1$ pF, and hence this corner frequency would correspond to an I_τ of 1.7 pA. However, when we measured I_τ in our simulation, we found it to be 0.6 pA. Because we are operating the circuit at such low currents, leakage currents could account for this discrepancy. Being such a small current, I_τ is directly affected by these leakage currents, and although we measure only 0.6 pA in our simulation, additional leakage currents in the simulation substrate may cause I_τ to appear to be 1.7 pA. Furthermore, we also find that the total harmonic distortion of the output signals reaches 6% at low frequencies and decreases with increasing frequency. Through our log-domain synthesis procedure, we have succeeded in designing a filter that remains quite linear for frequencies up to 100 Hz, which is the range of frequencies we are interested in for our biological model (see Section IV). More sophisticated

current multiplier/divider circuits that do not require $\kappa = 1$ may be used to achieve better performance [10].

IV. ADAPTIVE FILTER APPLICATION

We have used the class AB log-domain filtering approach presented here to construct a circuit inspired by adaptive filtering in the mammalian retina. The retina, one of the best studied neural systems, signals the onset or offset of visual stimuli in a sustained or transient fashion [15]. To encode these signals into spike patterns for transmission to higher processing centers, the retina has evolved intricate neuronal circuits that capture information contained within natural scenes efficiently [16]. This visual preprocessing, realized by the retina, occurs in two stages, in the outer and inner retina, and in two complementary paths. The retina's complementary signaling scheme is reminiscent of Seevinck and Frey's approaches, and so we adopt the class AB log-domain filtering approach to implement a proposed model of the inner retina [3], [19].

Our model for processing in the inner retina is based on the hypothesis that the inner retina adapts its low-pass and high-pass temporal filters to contrast and frequency in order to optimally encode signals [19]. Information theory stipulates that the optimal filter for capturing information contained in natural scenes is bandpass in space and time, with the filter's peak lying at the spatial and temporal frequencies where input signal power drops to the noise floor [2], [16]. As different stimuli are presented to the retina, optimal coding requires this filter's peak frequency to move accordingly. Thus, the retina adapts to temporal frequency to continue to convey information efficiently to higher cortical structures. Furthermore, in the case of increased contrast, which results in an increase in stimulus power, optimal filtering demands that the peak of this bandpass filter move to higher frequencies. Physiological data indeed demonstrates that the inner retina's temporal filter realizes this adaptation to contrast—ganglion cell responses compress in time and amplitude when driven by steps of increasing contrast [17]—by adjusting its time constant [13], [17].

A. ON-OFF Signaling

The second stage of visual processing begins with the bipolar cells, a class of feedforward neurons [15] that rectify signals received from the outer retina into complementary ON and OFF paths [4], [6], ensuring efficient information coding [9]. These pathways are realized through a sign-reversing synapse in one path and half-wave rectification in both [4], [6]. Complementary signaling is maintained in the inner retina through reciprocal inhibition between ON and OFF paths, realized by a set of narrow-field amacrine cells that ensure that only one path is active at any time. Such push-pull interactions between ON-OFF paths have been demonstrated physiologically through the existence of vertical inhibition between ON and OFF laminae [11]. Serial inhibition [5] may also play a vital role in these interactions.

We use our ON-OFF rectifying circuit, described in Section II, to implement the retina's complementary signaling scheme. Using currents computed in our outer retina circuit [19], we define cone terminal (CT) activity as I_- , which we compare to a reference current, which we define as I_+ . We set I_+ equal

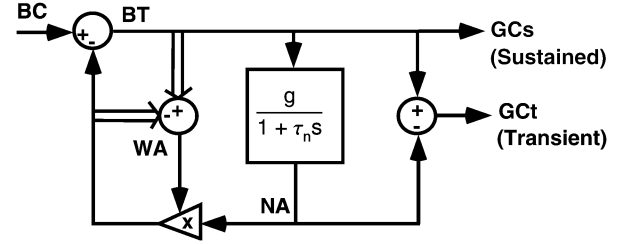


Fig. 6. Inner retina system-level diagram. Narrow-field amacrine cell (NA) signals represent a low-pass-filtered version of bipolar terminal (BT) signals and provide negative feedback on to the bipolar cell (BC). The wide-field amacrine cell (WA) network modulates the gain of NA feedback. WA receives full-wave rectified (double arrows) excitation from BT and full-wave rectified inhibition from NA. BT drives sustained ganglion cells (GCs) and the difference between BT and NA drives transient ganglion cells (GCt).

to the mean value of I_- such that the difference is positive when light is brighter (I_- decreases) and negative when light is dimmer (I_- increases). The outputs of this ON-OFF circuit represent activity at the ON and OFF bipolar terminals. Thus, this first stage of our circuit recreates computations performed by bipolar cells by diverting cone signals into complementary ON and OFF paths.

We use our ON-OFF low-pass filter, described in Section III, to recreate the synaptic interactions found in the inner retina. Bipolar terminals (BTs) excite narrow-field amacrine cells (NAs) in the inner retina. Large time-constants associated with NAs make this computation analogous to a low-pass filter. Furthermore, because of the retina's complementary signaling scheme, we implement this low-pass filter in complementary ON and OFF paths. Thus, we can simply define the inputs to our ON-OFF low-pass filter, I_t^+ and I_t^- , as ON and OFF BT activity, derived from our ON-OFF rectifying circuit. Similarly, the outputs of our ON-OFF low-pass filter, I_n^+ and I_n^- , are defined as ON and OFF NA activity.

B. Variable Gain Feedback

We propose in our model for processing in the inner retina that temporal adaptation is implemented through wide-field amacrine cell (WA) modulation of NA feedback (pre-synaptic inhibition) [19]. Thus far, our circuit synthesis procedure presented here only computes feedforward BT to NA excitation.

A system-level diagram of our complete inner retina model is shown in Fig. 6. Governed by this system diagram, we synthesize the remainder of our inner retina circuit by implementing NA to BT feedback inhibition, NA to GC (ganglion cell) feedforward inhibition, and BT to GC excitation. NA feedback inhibition is described by

$$I_{bt} = I_{bc} - wI_{na} \quad (13)$$

where w reflects WA activity, which is determined by the ratio of full-wave rectified BT excitation over full-wave rectified NA inhibition, as described in [19].

To implement NA feedback inhibition on to BT, modulated by WA, we use the subcircuit shown in Fig. 7. The voltage at node V represents WA activity and is the source of a transistor gated by V_n^+ . Thus, this activity modulates NA feedback inhibition on to BT—as voltage increases, gain, w , goes down

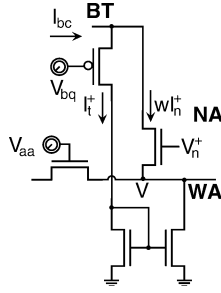


Fig. 7. Modulated negative-feedback subcircuit. Subcircuit that realizes modulation (WA) of negative feedback (NA) on to the input node (BT). WA activity, determined by voltage V , controls the source voltage of a feedback transistor, setting the feedback gain w . WA is excited by I_t^+ and inhibited by wI_n^+ (OFF inputs are not shown).

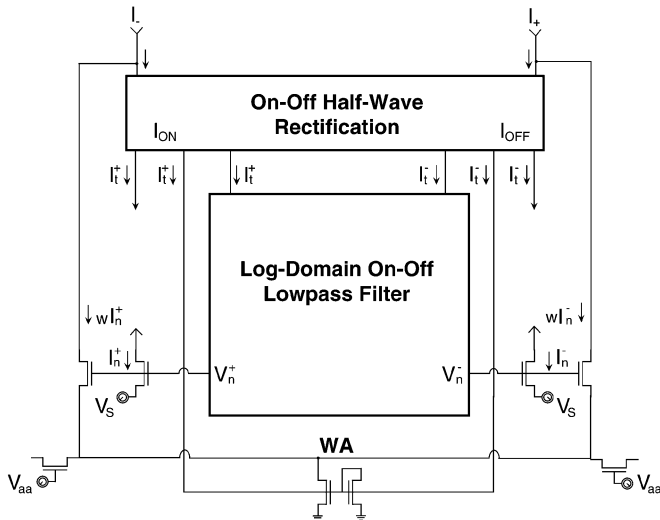


Fig. 8. Adaptive filter. The inputs to the circuit I_- and I_+ are fed to the ON-OFF rectifying circuit of Fig. 1(a), which produces three copies of its outputs (I_t^+ and I_t^-). One pair drives the ON-OFF low-pass filter. A second pair is used to excite wide-field amacrine cells (WA). The third pair is the high-pass output signal. The low-pass output signals are I_n^+ and I_n^- . The log-domain low-pass filter circuitry is shown in Fig. 4. Negative feedback is modulated by node WA, which multiplies I_n^+ and I_n^- by a gain, w .

and as voltage decreases, gain increases. Furthermore, WA activity at this node changes with BT excitation and NA inhibition. V decreases with increased current in I_t^+ and I_t^- (not shown), thus realizing excitation of WA activity (increased gain), and increases with increased current in I_n^+ and I_n^- (not shown), thus realizing shunting inhibition of WA activity. Convergence of ON and OFF signals implements full-wave rectified BT excitation and full-wave rectified NA inhibition. Finally, WA nodes are coupled to one another through an nMOS diffusion network gated by V_{aa} , which determines the strength of WA coupling. By adding this subcircuit, we can close the feedback loop in our inner retina model, producing the final circuit shown in Fig. 8.

For the biases, the relationship between $V_{\tau s}$, V_S , and V_τ determine BT-to-NA gain. Ideally, $V_{\tau s}$ should be set equal to $V_S + V_\tau$ for a gain of one. If $V_{\tau s} > V_S + V_\tau$, then the gain is greater than one, thus WA activity should be lower [19]. However, if $V_{\tau s} < V_S + V_\tau$, then the dc loop gain is less than one, causing the opposite effect [19]. V_{bq} determines residual current passed to the inner retina from BC. V_S acts as a reference for WA activity,

which is represented by voltage deviations below V_S . Finally, quiescent NA activity is controlled by V_b as discussed above.

C. Simulation Results

To demonstrate that WA modulation of NA feedback inhibition produces temporal adaptation, we simulated the inner retina circuit of Fig. 8. As we did not simulate an entire network, we could not exploit spatial averaging to compute mean WA activity, as the retina does. We used temporal averaging instead, which has the disadvantage of being slow, by connecting a large capacitor ($C = 1$ nF) to node WA.

In practice, one side of our bipolar circuit is tied to a reference voltage which sets the mean activity in the outer retina [20], while the other side fluctuates with light intensity. To maintain this convention, we input a fixed 5-nA current I_+ to one side of the bipolar circuit (the ON-OFF circuit shown in Fig. 1) and a 0.125-Hz frequency modulated sinusoidal 1 nA current I_- that fluctuates around a 5-nA mean level to the other side. The carrier frequency of this signal was 55 Hz, and we used an index of modulation of 360 (defined as the ratio between the depth of modulation, 45 Hz, which represents half the frequency range, and the modulation frequency, 0.125 Hz), thus giving us a signal whose frequency cycled from 10 to 100 Hz over an 8-s period. The outputs of this bipolar circuit feed our inner retina circuit.

The response of the inner retina circuit to these inputs is shown in Fig. 9(a). The input of the low-pass filter, bipolar terminal activity, is represented by a differential signal, $I_t^+ - I_t^-$, in the first trace. The output of the low-pass filter is also represented by a differential signal, $I_n^+ - I_n^-$ in the second trace of the figure. At the beginning and end of the cycle, this low-pass filter output is larger because of the low input frequencies, thus providing more inhibition on to wide-field amacrine cells. From the simulation, we find that wide-field amacrine cell voltage, V_{wa} , driven by inputs from narrow-field amacrine cells and bipolar cells, fluctuates at the 0.125-Hz modulation frequency of our input, as shown in the third trace. In regions where input frequency is low, narrow-field amacrine cell inhibition drives V_{wa} upwards. In regions where input frequency is high, bipolar terminal excitation drives V_{wa} downwards.

Because V_{wa} is at the source of the narrow-field amacrine cell's feedback transistor, WA activity is below the source bias, $V_S = 400$ mV, for our low-pass filter throughout the trace, and thus provides a gain, w , to our feedback signal, $I_n^+ - I_n^-$. By taking the exponential of V_{wa} , we can directly see what this gain term is in the fourth trace. Thus, modulated NA feedback, $w(I_n^+ - I_n^-)$, is larger than unmodulated NA activity, as the feedback gain, w , exceeds one. This modulated feedback signal roughly matches the bipolar signal, $I_t^+ - I_t^-$, as shown by the overlay in the first panel. We expand the central region of this trace in Fig. 9(b). The simulation demonstrates temporal frequency adaptation since, as the frequency of the input signal changes, the system changes WA activity such that BT excitation is balanced by NA inhibition.

By adjusting its time constant, our circuit design based on circuitry in the inner retina demonstrates temporal adaptation [20]. Because we modulate the input frequency sinusoidally, we can see this adaptation for different temporal frequencies by observing the simulation results over time. This adaptation

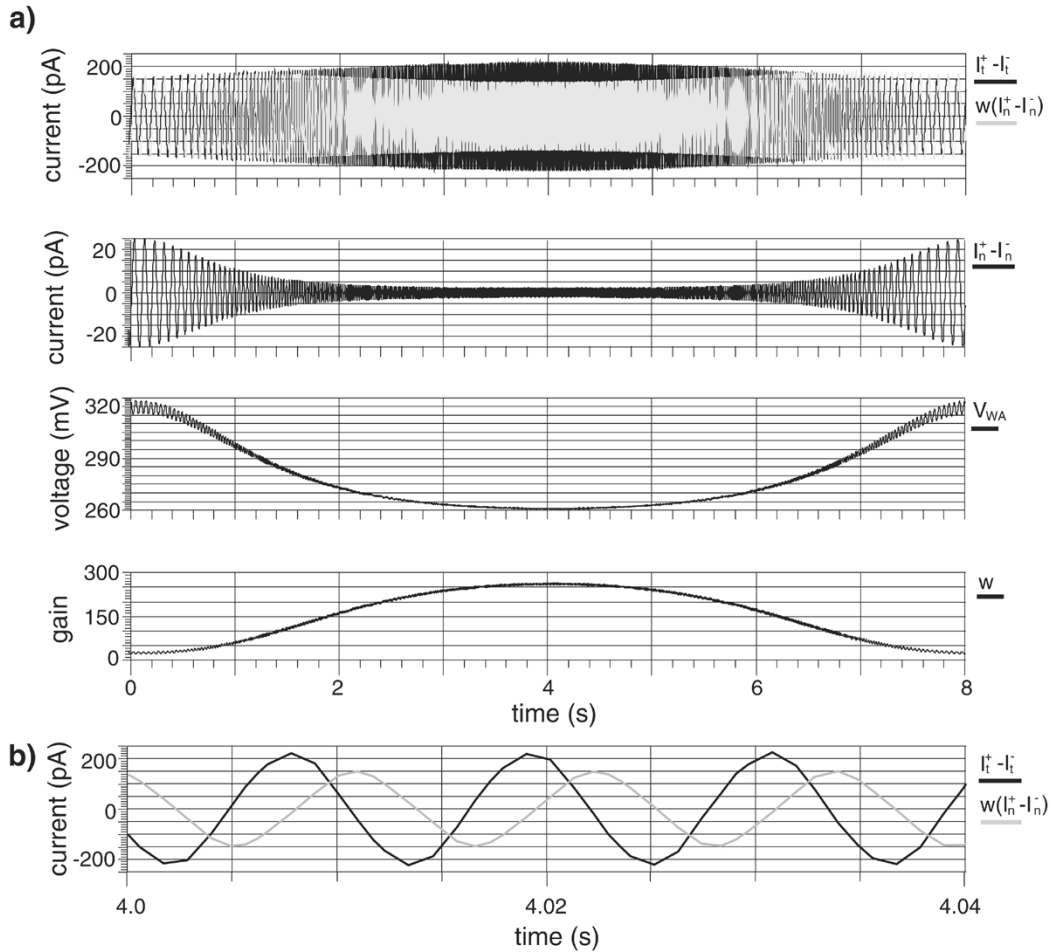


Fig. 9. Adaptive circuit simulation. (a) Circuit simulation of entire adaptive circuit. Circuit parameters are identical to Fig. 5, except we set $V_b = 1.1$ V to minimize the effect of dc signals on wide-field amacrine cell adaptation. $V_{bq} = 2.2$ V. Circuit activity is represented by differential signals. Note that the voltage at WA fluctuates with the same signal frequency, 0.125 Hz, as our input frequency is modulated. Through this frequency modulation, the input frequency to the system cycles from 10 to 100 Hz over a period of 8 s. V_{wa} sets the system loop gain (gain = $e^{(V_s - V_{wa})/U_T}$, bottom trace) greater than one, making the feedback (shown here as the differential signal $w(I_n^+ - I_n^-)$) larger than the unmodulated low-pass signal $I_n^+ - I_n^-$. (b) A magnified view of the first trace in (a) demonstrating adaptation in regions of higher temporal frequency.

matches the system's time constant to the input, as we expect the mammalian retina to do in response to changing scenes. In addition, low-pass and high-pass signals from our circuit have a quarter-cycle phase difference *and* equal amplitudes over a wide range of stimulus frequencies. Thus, the circuit approximates a Hilbert transform, which has been used to model human visual motion sensing [18]. Other visual computations, such as tracking algorithms, collision avoidance algorithms, and vision-based robotics, may benefit from this adaptation to temporal frequency, which produces a speed-invariant representation.

This approach and this design may be useful in any application necessitating dynamic time constant adaptation. When changing input frequencies unbalance amplitudes in the high-pass and low-pass paths, adaptation brings these signals into balance. This adaptation remains effective until the low-pass filter's output drops below its dc offset [19]. Furthermore, amplification of differential signals and rejection of dc signals in our filter preserves temporal stability that was absent in earlier designs [3]. Thus, our design presented here may be useful in other applications where adaptation and stability are

important. Our inner retina design corrects flaws in the design in [3], which failed to produce temporal adaptation.

V. CONCLUSION

Inspired by the mammalian retina's complementary ON-OFF paths, we implemented log-domain filtering through a push-pull circuit that extends dynamic range without increasing power consumption. Furthermore, by modeling variable gain negative-feedback in narrow-field amacrine cells, we realized time-constant adaptation. We replicated these nonlinear temporal filtering operations in subthreshold CMOS circuits using a new log-domain synthesis procedure that extends earlier implementations of current-mode class AB circuits [7], [12] by imposing a dynamic geometric-mean common-mode constraint. This approach simplifies the extraction of signal energy (full-wave rectification) required for adaptation and for modulation of loop gain without affecting common-mode gain or stability. Experimental test results from a retinomorph chip that uses these circuits to recreate visual processing in the mammalian retina are presented elsewhere [20].

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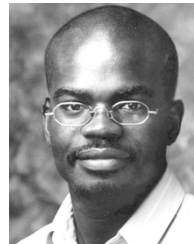
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