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Synthetic Neural Circuits Using Current–Domain Signal Representations

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We present a new approach to the engineering of collective analog computing systems that emphasizes the role of currents as an appropriate signal representation and the need for low-power dissipation and simplicity in the basic functional circuits. The design methodology and implementation style that we describe are inspired by the functional and organizational principles of neuronal circuits in living systems. We have implemented synthetic neurons and synapses in analog **CMOS VLSI** that are suitable for building associative memories and self–organizing feature maps.

1 Introduction

Connectionist architectures, neural networks, and cellular automata (Rumelhart and McClelland 1986; Kohonen 1987; Grossberg 1988; Toffoli 1988) have large numbers of simple and highly connected processing elements and employ massively parallel computing paradigms, features inspired by those found in the nervous system. In a hardware implementation, the physical laws that govern the cooperative behavior of these elements are exploited to process information. This is true both at the system level, where global properties such as energy are used, and at the circuit level, where the device physics are exploited. For example, Hopfield's network (1982) uses the stable states of a dynamic system to represent information; associative recall occurs as the system *converges* to its local energy minima. On the other hand, Mead's retina (1989) uses the native properties of silicon transistors to perform local automatic gain control.

In this paper we discuss the importance of signal representations in the implementation of such systems, emphasizing the role of currents. The paper is organized into six sections: Section 2 describes the roles played by current as well as voltage signals. The metal-oxide-semiconductor (MOS) transistor, the basic element of complementary-MOS (CMOS) very large scale integration (VLSI) technology, is introduced in Section **3.** In the subthreshold region, the MQS transistor's behavior strongly resembles that of the ionic channels in excitable cell

membranes. Translinear circuits, a computationally rich class of circuits with current inputs and outputs, are reviewed in Section 4. These circuits are based on the exponential transfer characteristics of the transistors, a property that also holds true for certain ionic channels. Simple and useful circuits for neurons and synapses are described in Section **5.** Proper choice of signal representations leads to very efficient realizations; a single line provides two–way communication between neurons. Finally, a brief disscussion of the philosophy behind the adopted design methodology and implementation style is presented in Section **6.**

2 Signals

In an electronic circuit, signals are represented by either voltages or currents.[1] A digital CMOS circuit depends on two well defined *voltage* levels for reliable computation. Currents play only an incidental role of establishing the desired voltage levels (through charging or discharging capacitive nodes). Since the abstract Turing model of computation does not specify the actual circuit implementation, two distinct current levels will work as well. In contrast, the circuits described here use *analog signals* and rely heavily on currents; both currents and voltages having continuous values.

At the circuit level, Kirchoff's current law (KCL) and Kirchoff's voltage law (KVL) are exploited to implement computational primitives. KCL states that the sum of the currents entering a node equals the sum of the currents leaving it (conservation of ,charge). So current signals may be summed simply by bringing them to the same node. KVL states that the sum of voltages around a closed loop is zero (conservation of energy). Therefore, voltage signals may be summed as well. Actually, the translinear circuits described in Section 4 rely on KVL while avoiding the use of differential voltage signals (not referenced to ground).

Voltages are used for communicating results to different parts of the system or for storing information locally. Accumulation of charge on a capacitor (driven by a current source) results in a voltage that represents *local* memory in the system. This also implements the useful function of temporal integration. Distributed memory can be realized using *spatiotemporal* patterns of charge, following the biological model (Freeman *et al.* 1988; Eisenberg *et al.* 1989). In this type of memory, stored information is represented by limit-cycles in the phase space of a dynamic system. However, in current VLSI implementations, memory is represented as point attractors (i.e., a stable equilibrium) in the spatial distributions of charge, as, for example, in our bidirectional associative memory chips (Boahen *et al.* 1989a,b).

[1] This may be an area in which biological systems have a distinct advantage by employing both chemical and electrical signals in the computation.

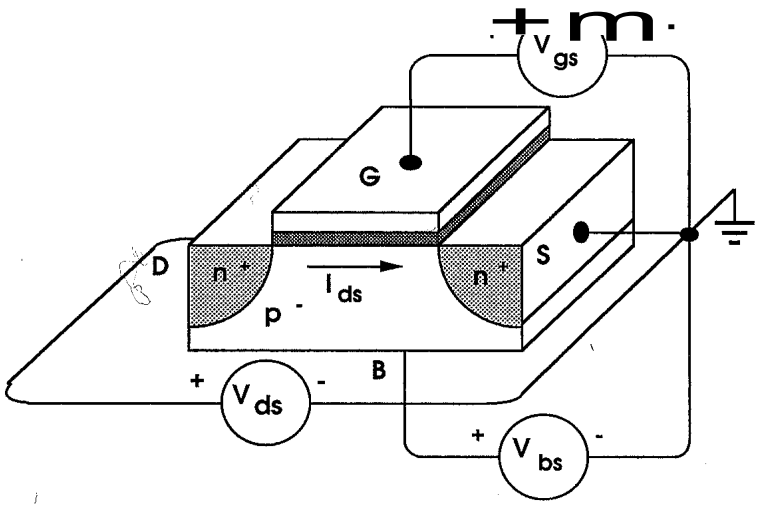

Figure 1: The MOS transistor. (a) Structure.

3 Devices

The MOS transistor, shown in Figure 1a, has four terminals: the gate (G), the source (S), the drain (D), and the substrate (B, for bulk). The gate and source potentials control the charge density in the channel between the source and the drain, and hence the current passed by the device. The MOS transistor is analogous to an *ensemble* of ionic channels in the lipid membrane of a cell controlled by the transmembrane potential.

We operate the MOS transistor in the so-called "off" region, characterized by gate source voltages that are below the threshold voltage. In this region charge transport is by *diffusion* from areas of high carrier concentration to energetically preferred areas of lower carrier concentration. This is referred to as *weak–inversion* (ViHoz and Fellrath 1977) or *subthreshold conduction* (Mead 1989; Maher *et al.* 1989). The transfer characteristics are shown in Figure 1b. These curves are very similar to those for the calcium–controlled sodium channel, Hille (1984, **p.** 317). In both cases the exponential relationships arise from the Boltzmann distribution.

The subthreshold current is given by[2]

$$I_{ds} = I_0 e^{[(1-K)Vbs]/VT} e^{KVgs/VT} (1 - e^{-Vds/VT} + Vds/V_0) \quad (3.1)$$

[2]For the sake of brevity, we discuss only the n-type device whose operation depends on the transport of negative charges. The operation of a p-type device is analogous.

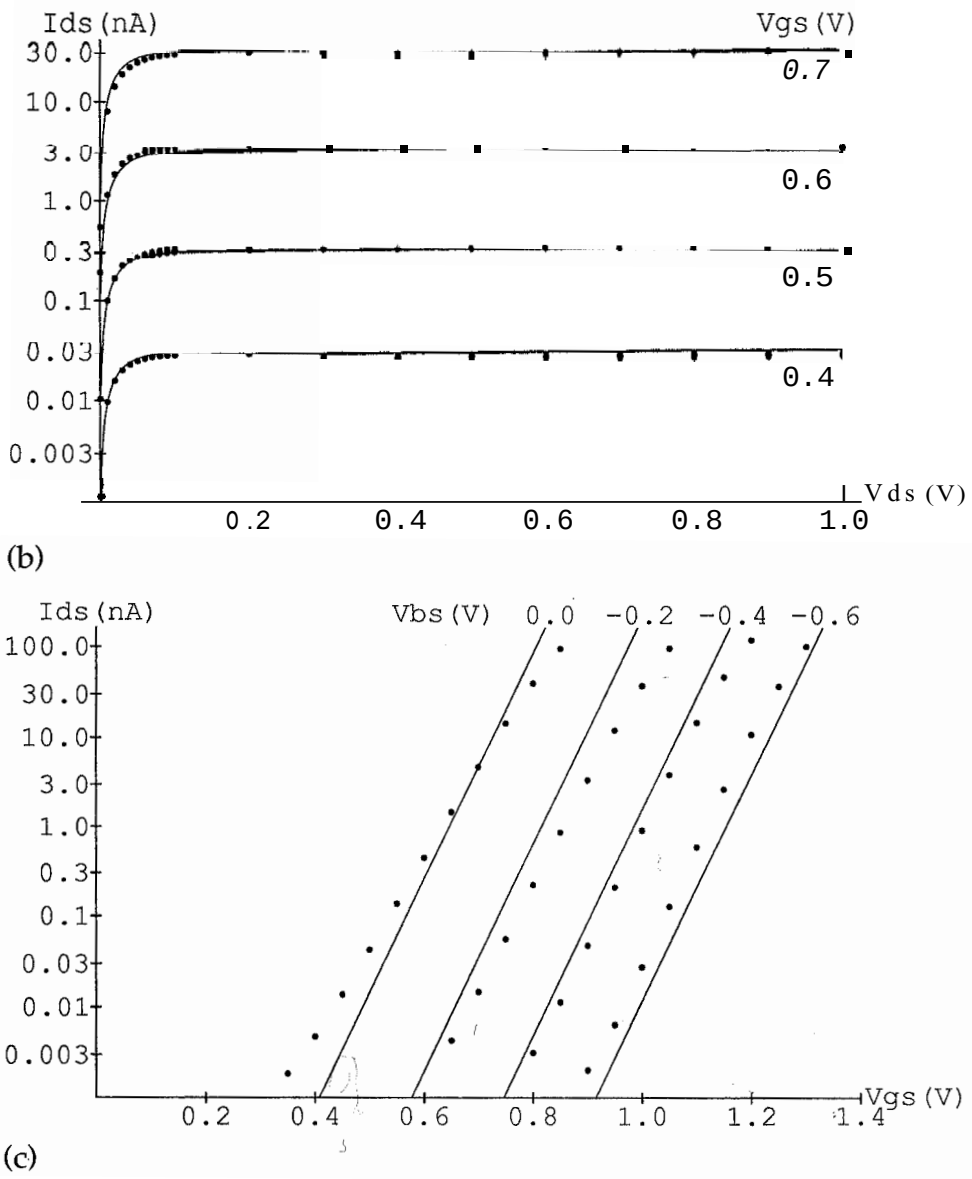

Figure 1: *Cont'd* (b) transfer characteristics, (C) output characteristics. To first order, the current is exponentially dependent on both the substrate and the gate voltages. In (b) the dots show measured data from an n–type transistor of size 4 x 4 μm, with $V_{ds} = 1.0\,V$. The solid lines are obtained using equation 3.1 with $I_0 = 0.72 \times 10^{-18}$A and $\kappa = 0.75$. The data in (b) are for a similar device with $V_{bs} = 0$; it is fitted with $V_O = 15.0\,V$.

where I_0 is the zero–bias current and κ measures the effectiveness of the gate potential in controlling the channel current. To first order, the effectiveness of the substrate potential is given by $(1-\kappa)$; $V_T = kT/q$, the thermal voltage, equals 26 mV at room temperature, and V_0 is the Early voltage, which can be determined from the slope of the I_{ds} versus V_{ds} curves. Notice that I_{ds} changes by a factor of e for a $V_T/K = \mathbf{33.0}\ mV$ change in V_{gs}. This drain current equation is equivalent to that in Maher

et al. (1989); however, in this form the dependence on the substrate voltage is explicit. This three parameter model is adequate for rough design calculations but not for accurate simulation of device operation. Refer to Mead (1989, Appendix B) for a more elaborate model. Subthreshold currents are comparable to currents in cell membranes; they range from a few picoamps to a few microamps.

For a given gate–source voltage V_{gs}, the MOS transistor has two distinct modes of operation, determined by the drain–source voltage V_{ds}, as shown by the output characteristics in Figure 1c. The behavior is roughly linear if V_{ds} is less than $V_{dsat} \approx 100\,mV$; small changes in V_{ds} cause proportional changes in the drain current. For voltages above V_{dsat}, the current saturates. In this region the MOS transistor is a current source with output conductance:

$$g_{dsat} = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{I_{ds}}{V_0} \tag{3.2}$$

The change in drain current for a small change in gate voltage is given by

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{\kappa I_{ds}}{V_T} \tag{3.3}$$

g_m is called the *transconductance* because it relates a current between two nodes to a voltage at a third node. As we shall see, the subthreshold MOS transistor is a very versatile circuit element because $g_m \gg g_{dsat}$.

4 Circuits

Area–efficient (compact) functional blocks can be obtained by using the MOS transistor itself to perform as many circuit functions as possible. The three possible circuit configurations for the transistor are shown in Figure **2:**

In the common–source mode, it is an *inverting amplifier* with high voltage gain: g_m/g_{dsat}.

In the common–drain mode, it is a *voltage follower* with low output resistance; $1/g_m$

In the common–gate mode, it is a *current buffer* with low output conductance; g_{dsat}.

In the synthetic neuronal circuits described in the next section the inverting amplifier is used as a feedback element to obtain more ideal circuit operation while the voltage follower and the current buffer are used to effectively transfer signals between different circuits.

The actual computations are performed by current–domain (or current–mode) circuits. **A** *Current–Domain* (CD) circuit is one whose input signals and output signals are currents. The simplest CD circuit is shown in Figure **3.** This circuit copies the input current to the output and reverses its direction. It is appropriately named a *current mirror.* The circuit has just two transistors: an input transistor and an output transistor. The input current I_{in} is converted to a voltage V_b by the input transistor. This voltage sets the gate voltage of the output transistor. Thus, both devices have the same gate–source voltages and will pass the same current if they are identical and have the same drain and substrate voltages.

In practice, device mismatch produces random variations in the output current, while the nonzero drain conductance results in systematic variations. More complicated mirror circuits, for example, the Wilson mirror or the Complex mirror (Pavasovic *et al.* 1988), may be used to obtain lower output conductance. By using more output devices, several copies of the input current can be obtained. The current mirror is analogous to a basic synapse structure in biological systems: it is simple in

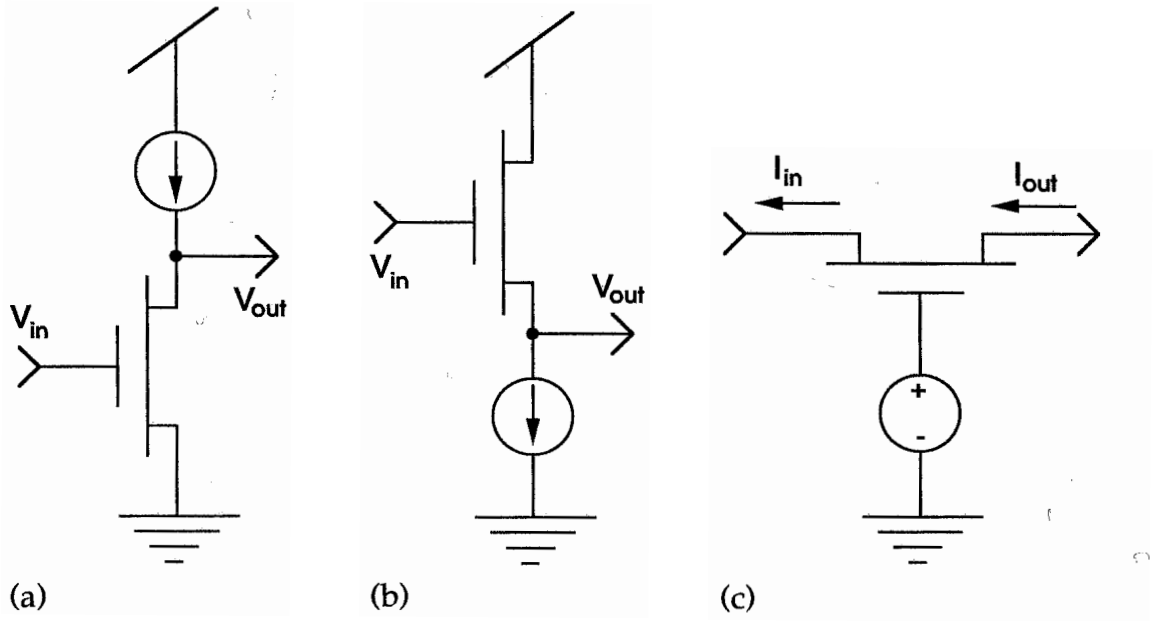

Figure 2: MOS transistor circuit configurations. (a) Common–source, (b) common-drain, and (c) common–gate modes of operation. In (a) voltage gain is obtained by converting the current produced by the device's transconductance to a voltage across its drain conductance. In (b) a voltage follower/buffer is realized; the gate–source drop is kept constant by using a fixed bias current and setting $V_{bs} = 0$. In (c) the device serves as a current buffer by transferring the signal from its high conductance source terminal to the low conductance drain node.

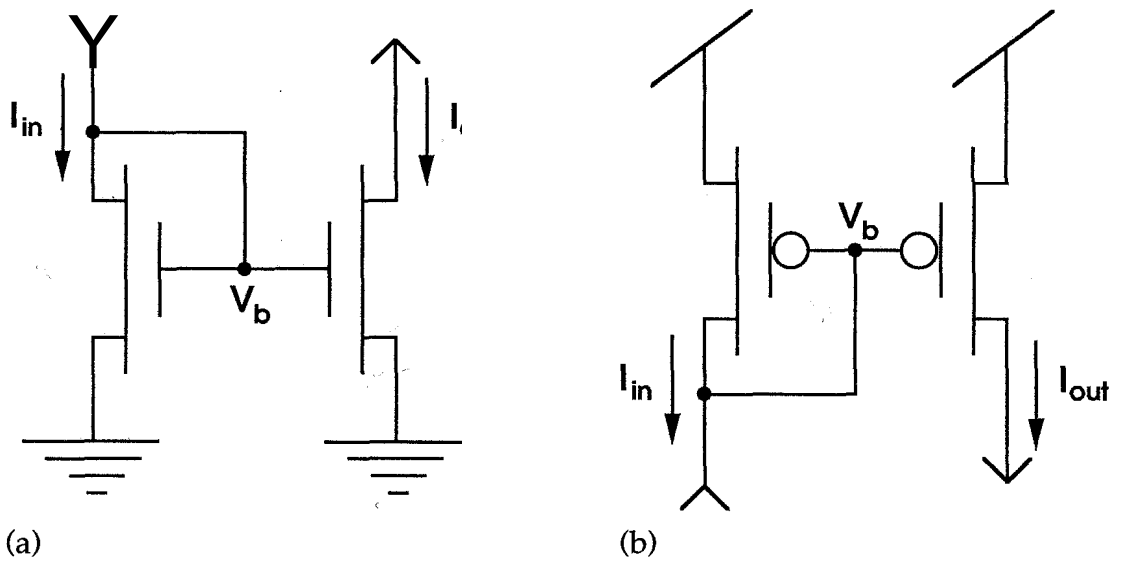

Figure 3: Current mirror circuits using (a) n–type and (b) ptype transistors. These circuits provide an output current that equals the input current if the devices are perfectly matched. For subthreshold operation, we observe variations of about 10%, on average: using 4 x *4pm* devices.

form, it enforces *unidirectional* information flow, and it can function over a large range of input and output signal levels.

Translinear circuits (Gilbert 1975) are a computationally powerful subclass of CD circuits. A *translinear circuit* is defined as one whose Operation depends on the linear relationship between the transconductance and the channel current of the active devices (Equation **3.3**).[3] The current mirror in subthreshold operation is an example of a translinear circuit. The *Translinear Principle* (Gilbert 1975) can be used to synthesize a wide variety of circuits to perform both linear and nonlinear operations on the current inputs, including products, quotients, and power terms with fixed exponents. The Gilbert current multiplier is one of the better known translinear circuits. Gilbert's elegant analog array normalizer (1984) is an example of a more powerful translinear circuit. One fascinating aspect of translinear circuits is that although the currents in its constitutive elements (the transistors) are exponentially dependent on temperature, the overall input/output relationship is insensitive to isothermal temperature variations. The effect of small local variations in fabrication parameters can also be shown to be temperature independent. Finally, translinear circuits are simple, because an analog representation is used and the native device properties provide the computational primitives.

[3]Translinear circuits have traditionally been built using bipolar transistors.

5 Synapses and Neurons

In a neuronal circuit, the interaction between neurons is mediated by a large variety of synapses (Shepherd 1979). **A** neuron receives its inputs from other neurons through synaptic junctions that may have different efficacies. In a VLSI system, the synapses are implemented as a two–dimensional array with the neurons on the periphery. This is because $O(N^2)$ synapses are required in a network with N neurons. Generally, two sets of lines (buses) are run between the neurons and the synaptic array; one carries neuronal output to the synapses and the other feeds input to the neurons. However, in networks with reciprocal connections, such as the bidirectional associative memory (Boahen *et al.* 1989a,b), proper choice of signal representations leads to a more efficient implementation.

Our circuit implementations for neurons and synapses are shown in Figure 4. These circuits use voltage to represent a neuron's output (presynaptic signal) and current to represent its inputs (postsynaptic Signals). Since currents and voltages may be *independently* transmitted along the same line, these signal representations allow a neuron's output and

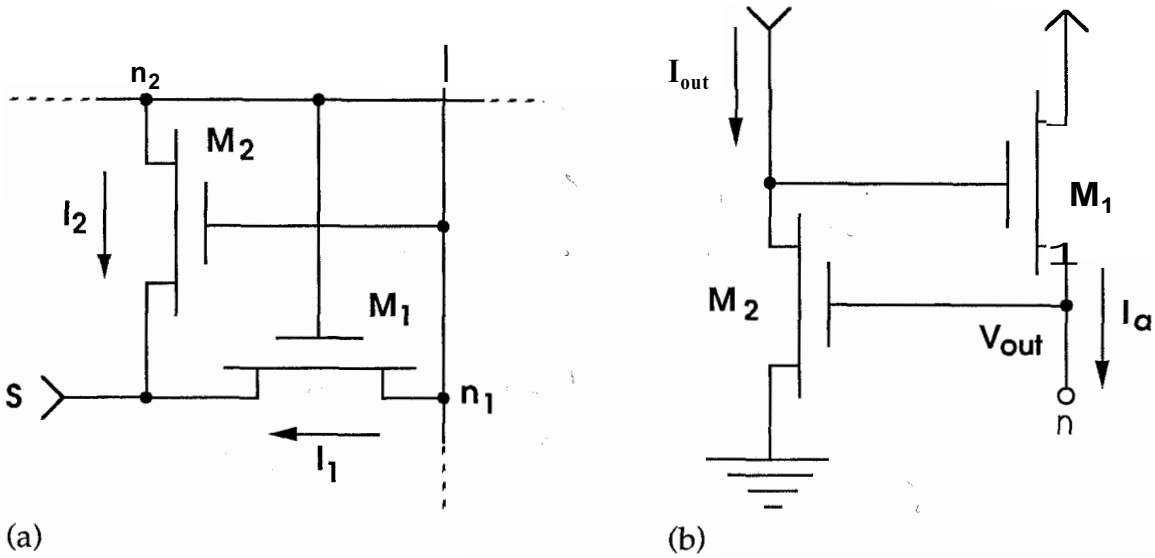

Figure 4: Circuits for synapses and neurons. (a) Reciprocal synapse and (b) neuron. These circuits demonstrate efficient signal representations that use a single line to provide two–way communication. **A** voltage is used to represent information going one way while a current is used to send information the other way. The synapse circuit in (a) provides bidirectional interaction between two neurons connected to nodes n_1 and n_2. The neuron circuit in (b) sends out a voltage that mirrors its output current I_{out} in the synapses while receiving the total current I_a from these synapses.

inputs to be communicated using just one line. Voltage output facilitates fan–out while current input provides summation. Thus, in close analogy to actual neuronal microcircuits, the output signal is generated at the same node at which inputs are integrated.

The two transistor synapse circuit (Figure 4a) provides *bidirectional* interaction between neurons connected to nodes n_1 and n_2; each transistor serves **as** a synaptic junction. When s is at ground, voltages applied at nodes n_1 and n_2 are transformed into currents by the transconductances of M_2 and M_1, respectively. If these voltages exceed V_{dsat}, the transistors are in saturation and act as current sources. Thus, changes in the voltage at $n_1(n_2)$ do not affect the current in $M_1(M_2)$. Actually, for a small change in Vn_1, the changes in I_1 and I_2 are related by

$$\frac{\Delta I_1}{\Delta I_2} = \frac{g_{dsat_1}}{g_{m_2}} = \frac{I_1}{I_2}\frac{V_T}{\kappa V_0}$$

This gives

$$\frac{\Delta I_1}{I_1} = \frac{1}{450}\frac{\Delta I_2}{I_2}$$

Hence, we can double I_2 (using the voltage at n_1) while disturbing I_1 by only 0.2%. The interaction is turned off by setting s to a high voltage, or modulated by applying an analog signal to the substrate.

The circuit for the neuron also uses just two transistors (Figure 4b). The net input current I_a (for activation), formed by summing the inputs at node n, is available at the drain of M_1. This device buffers the input current and controls the output voltage. I_a is fed through a nonlinearity, for example, thresholding (not shown), to obtain I_{out}, which sets the output voltage V_{out}. This is accomplished by using M_1 as a voltage follower and providing feedback through M_2, which functions as an inverting amplifier; M_1 adjusts V_{out} so that the current in M_2 equals I_{out}. Hence, V_{out} will mirror I_{out} in the synapses. The feedback makes the output voltage insensitive to changes in the input current, I_a. Actually, the output conductance is approximately $g_{m1}g_{m2}/g_{dsat2}$; it is increased by a factor equal to the gain provided by M_2.

In this case, a small change in V_{out} produces changes in I_a and I_s (the postsynaptic copy of I_{out}) given by

$$\frac{\Delta I_s}{\Delta I_a} = \frac{g_{m\,synapse}}{g_{m_1}g_{m_2}/g_{dsat_2}} = \frac{I_s}{I_a}\frac{V_T}{\kappa V_0}$$

Hence, if I_s doubles, the resulting change in V_{out} decreases I_a by only 0.2%-just as in the previous case. Note that I_{out} must always exceed a few picoamps to keep V_{out} above V_{dsat}. The characteristics of these

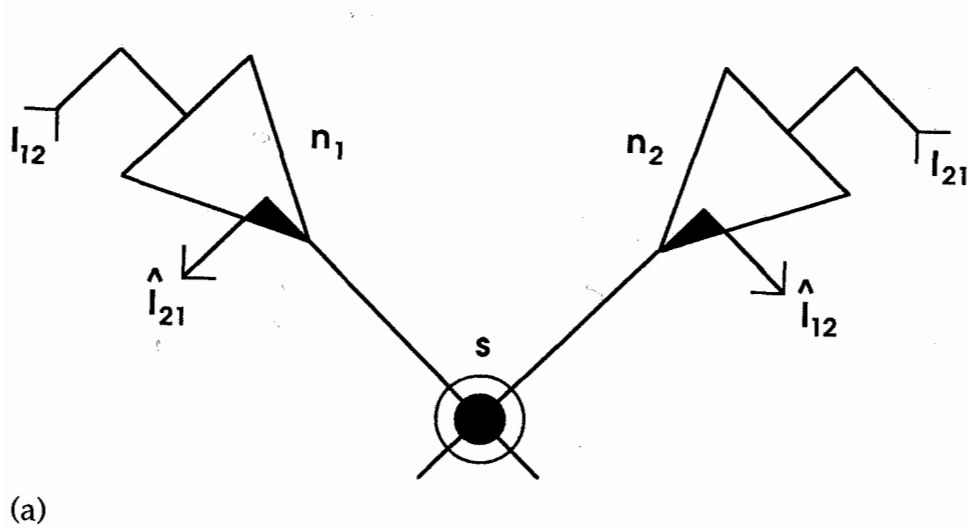

Figure 5: Characteristics of a synthetic neuronal circuit. (a) A simple circuit consisting of two neurons (n_1 and n_2) and a synapse (s) was built and tested to demonstrate the proposed communication scheme. The currents sent by $n_1(n_2)$ and that received by $n_2(n_1)$ are denoted by $I_{12}(I_{21})$ and $\hat{I}_{12}(\hat{I}_{21})$, respectively. Continued on next page.

circuits, designed using $4\,p\,m \times 4\,p\,m$ devices and fabricated through MOSIS, are shown in Figure 5a–c.

6 Discussion

The adopted design methodology is governed by three simple principles: First, the computation is carried out in the analog domain; this gives simple functional blocks and makes efficient use of interconnect lines. Second, the physical properties of silicon-based devices and circuits are used synergetically to obtain the desired result. Third, circuits are designed with power dissipation and area efficiency as prime engineering constraints, not accuracy or speed. We believe power dissipation will be a serious limitation in large scale-analog computing hardware. Unlike digital integrated circuits, the massive parallelism and concurrency attainable with analog computation impose serious limits on the amount of power that each circuit can dissipate. This is why we operate the devices with currents in the nanoamps range and, if possible, picoamps, about the same current levels found in biological systems.

This approach is similar to, and strongly influenced by, that of Mead's group at Caltech. Our approach is more minimalistic, we view the transistor itself as the basic building block; not the transconductance amplifier. Thus, currents, rather than differential voltages, are the primary signal representation.

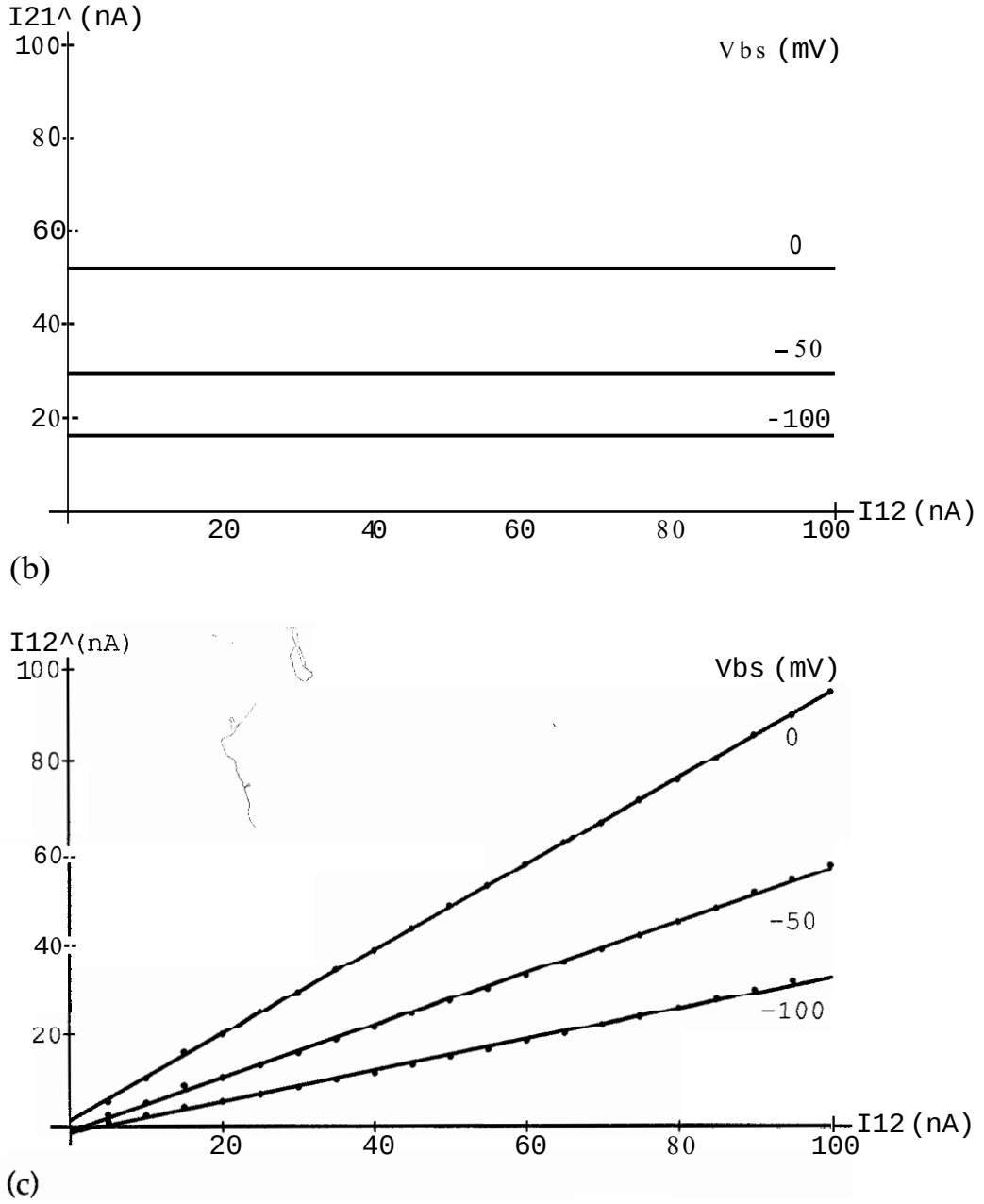

Figure 5: *Cont'd* Plots (b) and (c) show how $I\hat{}_{12}$ and $I\hat{}_{21}$ vary as I_{12} is stepped from *2.0nA* to 100nA while I_{21} is held at *50nA,* for various substrate bias voltages. The values V_{bs} = 0, –50, and -100mV correspond to weights of 0.93, 0.57, and **0.33,** respectively. Notice that these weights modulate signals going both ways symmetrically.

We are not concerned about accuracy or matching in the basic elements because biological systems perform well despite the limited precision of their neurons and synaptic connections. The emerging view is that this is a result of the collective nature of the computation performed—whereby large numbers of elements contribute to the final result. From

a system designer's point of view, this means that random variations in transistor characteristics are not deleterious to the system's performance, whereas systematic variations are and must therefore be kept to a minimum. Indeed, we have observed this in silicon chips.

The translinear property of the subthreshold MOS transistor provides a very powerful computational primitive., This property arises from the highly nonlinear relationship between the gate potential and the channel current. In fact, the exponential is the strongest nonlinearity relating a voltage and a current in solid-state devices (Shockley 1963; Gunn 1968). It is interesting to note that the same property holds for voltage–activated ionic channels, however, the conductance dependence is steeper due to correlated charge control of the current (Hille 1984, p. 55). In translinear (current–domain) circuits we have seen a classical example of how a rich form for circuit design emerges from the properties of the basic units (MOS transistor in subthreshold).

To summarize, we have addressed some issues related to the engineering of collective analog computing systems. In particular, we have demonstrated that currents are an appropriate analog signal representation. Current levels comparable to those in excitable membranes are achieved by operating the devices in the subthreshold region resulting in manageable power dissipation levels. This design methodology and implementation style have been used to build associative memories (Boahen *et al.* 1989a, b) and self–organizing feature maps in analog VLSI.

Acknowledgments

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