

AMORPHOUS SILICON CORE-SHELL NANOWIRE SOLAR CELLS

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ABSTRACT

Nanostructures such as nanoparticles and nanowires have been demonstrated as powerful tools to improve light absorption[1-4], to enable low temperature process[5], to demonstrate multi-exciton generation[6], and to decouple the absorption depth and carrier diffusion length[7, 8]. Here we demonstrated the first amorphous silicon core-shell nanowire solar cells, which can be fabricated through a low temperature, scalable processes. A simple Schottky based nanowire device structure is used to demonstrate the concept[9]. The device demonstrated much higher short circuit current (>150%) compared to the control thin film device, because of improved carrier collection. A core-shell nanowire solar cells based on p-i-n configuration is also proposed to further increase the efficiency. It provides a viable pathway to solve the mismatch between carrier diffusion length and absorption depth in amorphous silicon and to dramatically improve the device performance.

INTRODUCTION

Hydrogenated amorphous silicon is considered as one of the most important solar cell technologies [9, 10]. It is based on abundant, non-toxic materials, and can be fabricated through low temperature roll-to-roll processes (around 200°C)[11]. More importantly, a-Si:H can absorb light efficiently, with an absorption depth of only 1 μ m (at around 1.8eV), several hundred times thinner than that of crystalline silicon. However, a-Si:H has poor transport properties, with a short carrier diffusion length of around 300 nm[10]. In addition, there is 10%-30% efficiency degradation under light soaking, due to the Stabler-Wronski effect. It is found that degradation is less severe with thinner a-Si:H films (below 300 nm)[10].

To solve the mismatch between carrier diffusion length and absorption depth, and reduce the efficiency degradation, here we demonstrate a new device structure nanowire based solar cells. Because of asymmetry geometry of nanowires and the core-shell structure, the carrier collection and light absorption can be decoupled into different directions. Carrier collection can be greatly improved without sacrificing light absorption. Therefore, much higher short circuit current density is achieved in nanowire core-shell devices compared to the control device. However, the performance of this type of solar cells suffered from the increased surface area, which will increase the dark current and series resistance. A new device structure (p-i-n core-shell structure) is also

proposed to solve these problems and further improve the performance.

EXPERIMENT

The schematic of a-Si:H core-shell nanowire solar cells is shown in Figure 1. 10nm n-type a-Si:H and 1 μ m intrinsic a-Si:H layers were deposited on glass substrates by plasma-enhanced chemical vapor deposition (PECVD) at 250°C. SiH₄, H₂ gas mixture was used for intrinsic layer growth. PH₃ was used as the dopant gas for n-layer growth. All the films contain a bonded hydrogen concentration around 10 at.-%, to reduce the broadening of the conduction and valence band-tails as well as the occurrence of dangling bonds.

The nanowire arrays were achieved by combining Langmuir-Blodgett (LB) assembly with reactive ion etching (RIE)[1, 12]. It is a low temperature, scalable process, which provides precise control of diameters, spacings and shapes across a wide range, from tens of nanometers to several microns. Monodisperse SiO₂ particles with diameters from 50 to 800 nm were first produced by a modified Stöber synthesis[13]. The particles were then modified with aminopoly methyldiethoxysilane to terminate them with positively charged amine groups to prevent aggregation. Monodisperse SiO₂ nanoparticles were assembled into a close packed monolayer on top of a wafer using the Langmuir-Blodgett (LB) method. Nanowires can be obtained by using Cl₂ based selective and anisotropic RIE etching. The diameter and spacing of these nanostructures are determined by the initial nanoparticle sizes and etching time. SiO₂ particles can be removed by hydrofluoric acid if needed. Once the nanowire array was formed, 10nm Pt was evaporated on top of that to form a Schottky junction at the interface between intrinsic a-Si:H layer and the metal film. For the solar cell test, the light is coming from the bottom of the whole structures (through the glass substrate).

For the control device, 10nm Pt is deposited directly on top of intrinsic a-Si:H layer. It is a simple schottky device, which used to be a very important a-Si:H configuration in its early stage development. The control device is very similar to the very early work demonstrated by Carlson and Wronski [9]. Since intrinsic a-Si:H layer is about 1 μ m, which is comparable to its absorption depth, most of photons with energy above the bandgap can be efficiently absorbed. So it was expected that device performance

can be greatly boosted if carrier collection can be improved. It was reported that peak collection efficiency is only around 20% [9], leaving much room for further improvement through structure innovations.

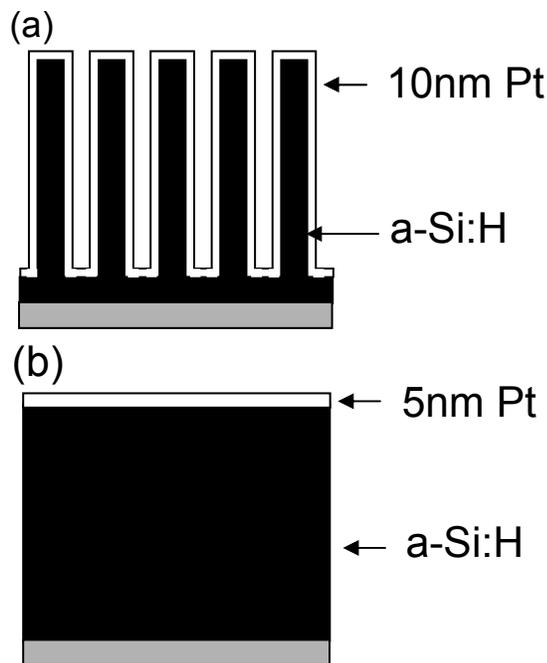


Figure 1. (a) Schematic of a-Si:H Nanowire Core-Shell Solar Cells. (b) Schematic of a-Si:H Thin Film Schottky Solar Cells

RESULTS AND DISCUSSION

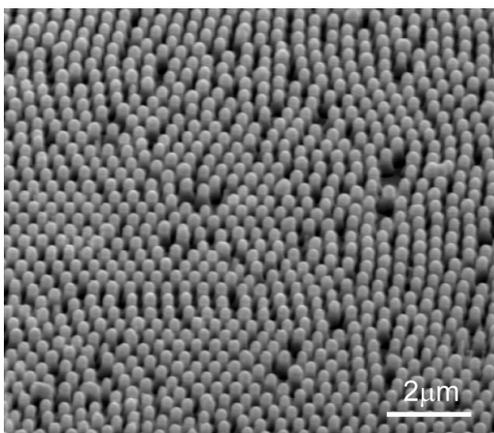


Figure 2. SEM image of a-Si:H Nanowires

The fabricated a-Si:H nanowire arrays are shown in Figure 2. The diameter of nanowires can be tuned from 100nm to 800nm through SiO₂ nanoparticle size and reactive ion etching conditions. By tuning the etching conditions, nanocone arrays can also be obtained, which have demonstrated an excellent anti-reflection property[1]. It is noted during experiment that the best performed devices

came from the nanowire arrays with diameter around 300nm. That is expected since the carrier diffusion in intrinsic a-Si:H layer is around that range. Therefore all the device performance reported in this paper is based on nanowires with 300nm diameter, and 700nm length.

The solar cell devices are tested in a solar simulator with 1 sun AM1.5G illumination. The device performance is shown in Fig. 3 and Fig. 4. For the a-Si:H thin film schottky device, the performance is very consistent with the results in the literature [9]. Because the carrier diffusion length (~300nm) is significantly shorter than the thickness of intrinsic layer (1µm), the device performance suffered from inefficient carrier collection, as evidenced by the low short circuit current density (J_{sc} :3.5mA/cm²). The open circuit voltage (V_{oc}) is about 0.74V, and fill factor (ff) is 0.51, very close to the results obtained in the literature [9].

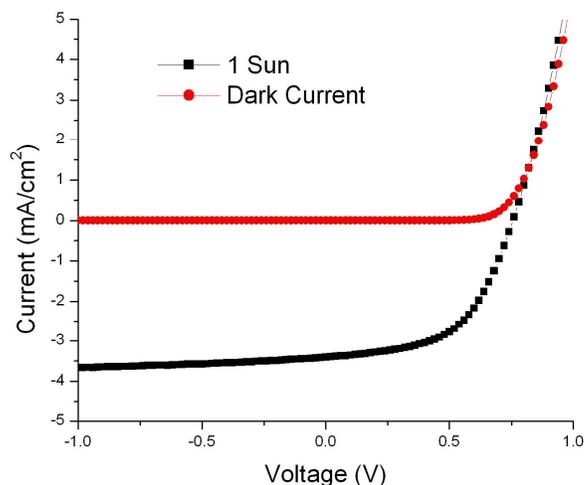


Figure 3. I-V curve of traditional Schottky Cells

For a-Si:H nanowire core-shell devices, the improvement in short circuit current density is very significant (Fig. 4). J_{sc} of 9.3mA/cm² is obtained, which is 150% larger than that of the control device. However, the dark current is significantly increased because of much increased surface area (Fig. 4 red curve). Because of that, open circuit voltage is reduced down to 0.46V. The increased surface area and the surface damage caused by reactive ion etching also caused significant increase in series resistance, which dramatically reduce fill factor down to 0.26. So the overall conversion efficiency is about the same for both thin film and nanowire devices (~1.2%).

It is noted that for solar cell efficiency test, light went through glass substrate, and the surface of a-Si:H nanowire arrays were coated with 10nm Pt films. Because of this highly reflective thin metal film, the light trapping effect within nanowire arrays is largely eliminated. Also the absorption depth for a-Si:H is 1µm (~1.8ev), which is the film thickness used in a-Si:H thin film schottky. So light

absorption is assumed to be efficient in both cases even without light trapping effect. Therefore, it is very obvious that the enhancement in short circuit current for core-shell nanowire devices is mainly due to the enhanced carrier collections.

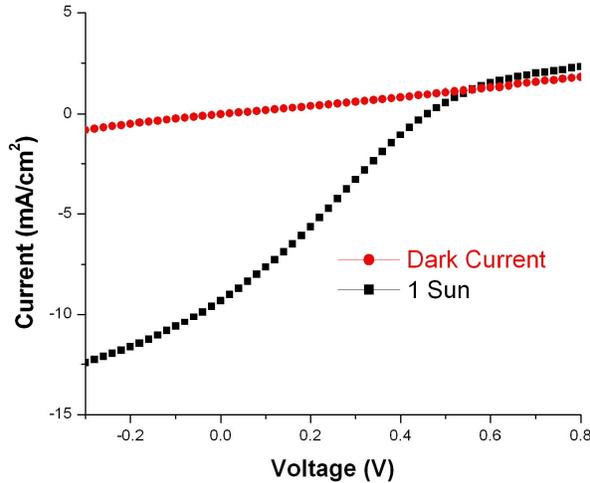


Figure 4. I-V curve of Nanowire based Solar Cells

To reduce the surface area, to minimize the surface damages, and to take advantage of light trapping effect in nanowire arrays, we propose a a-Si:H core-shell nanowire solar cells by using p-i-n structures (Fig.5) instead of schottky cells.

Besides improved open circuit voltage and electric field, there are several advantages to use n-i-p structures in core shell nanowire solar cell devices. First, transparent conducting oxide layer can be used to replace metal layers. Light can come from the top. Strong anti-reflection and absorption enhancement effects in nanowire arrays can be used to further improve device performance reduce material usage and process time. Second, nanostructures are formed for bottom contact materials. So there are no surface damages caused in active absorber layers as in the case of schottky cells. Third, because of strong absorption in nanowire arrays, the length of nanowire can be greatly reduced to several hundred nanometers, which will reduce the surface area and dark current. Fourth, since light does not go through the substrate, cheap substrates (such as stainless steel, polyimide) can be utilized, which also enable low cost high-throughput process (such as roll-to-roll). Therefore n-i-p based a-Si:H core-shell nanowire solar cells hold great promise for both high performance and low cost.

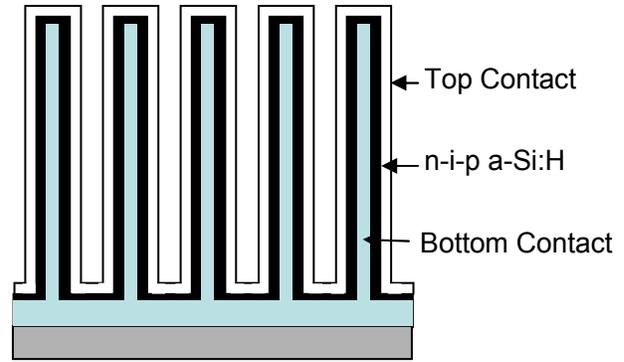


Figure 5. a-Si:H p-i-n Core-Shell Nanowire Solar Cells

SUMMARY

We have demonstrated for the first time a-Si:H core shell nanowire solar cells, using a simple Schottky configuration. Because of asymmetric geometry of nanowires, which can decouple the carrier diffusion length and absorption depth into different directions, nanowire devices demonstrated much higher short-circuit current compared to the control devices, because of improved carrier collections. However, the overall efficiency for nanowire devices is about the same as the control devices, due to reduced open circuit voltage and fill factor, caused by increased surface area and surface damage during the process. Combining significant light trapping effects, reduced surface area/damages with large open circuit voltage, it is expected the performance can be further boosted using n-i-p based core-shell nanowire based device structures.

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