Gate-Induced Metal−Insulator Transition in MoS_2 by Solid Superionic Conductor LaF_3

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S *Supporting Information*
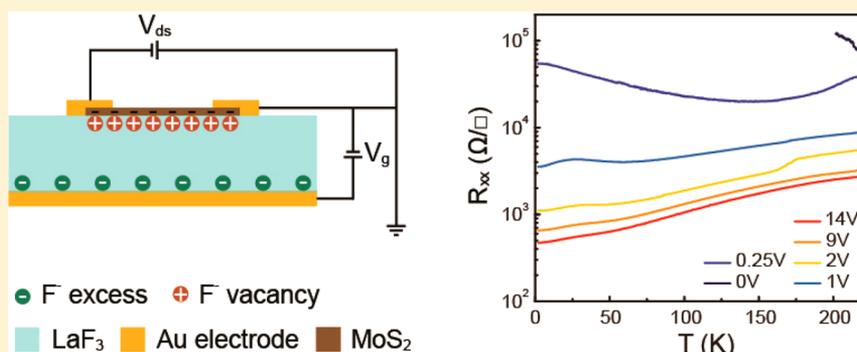
ABSTRACT: Electric-double-layer (EDL) gating with liquid electrolyte has been a powerful tool widely used to explore emerging interfacial electronic phenomena. Due to the large EDL capacitance, a high carrier density up to 10^{14} cm^{-2} can be induced, directly leading to the realization of field-induced insulator to metal (or superconductor) transition. However, the liquid nature of the electrolyte has created technical issues including possible side electrochemical reactions or intercalation, and the potential for huge strain at the interface during cooling. In addition, the liquid coverage of active devices also makes many surface characterizations and *in situ* measurements challenging. Here, we demonstrate an all solid-state EDL device based on a solid superionic conductor LaF_3, which can be used as both a substrate and a fluorine ionic gate dielectric to achieve a wide tunability of carrier density without the issues of strain or electrochemical reactions and can expose the active device surface for external access. Based on LaF_3 EDL transistors (EDLTs), we observe the metal−insulator transition in MoS_2. Interestingly, the well-defined crystal lattice provides a more uniform potential distribution in the substrate, resulting in less interface electron scattering and therefore a higher mobility in MoS_2 transistors. This result shows the powerful gating capability of LaF_3 solid electrolyte for new possibilities of novel interfacial electronic phenomena.

KEYWORDS: *Solid electrolyte, electric-double-layer transistor, two-dimensional materials, metal−insulator transition*

Carrier density is a key parameter in determining the electronic phase in materials. In a transistor geometry, an electric field can be applied across the gate dielectric and modulate the density of mobile charges in the channel material. The traditionally used dielectrics such as SiO_2 and HfO_2 are air-stable, easy to handle, and readily compatible with device fabrication. However, due to their low capacitance (∼10 nF/cm^2), the maximum charge density accessible is only around 10^{12} cm^{-2}, which is not high enough to induce electronic phase transitions in some materials. To reach a higher carrier density, a technique called electric-double-layer (EDL) gating using electrolytes (e.g., $LiClO_4(PEO)$)[1,2] or ionic liquids (e.g., DEME-TFSI)[3−6] has been widely adopted recently. The high

capacitance (∼10 μF/cm^2) and large ionic conduction (ionic conductivity = 10^{-6}−10^{-4} Ω cm) of these electrolytes enable the realization of phenomena that require a high carrier density. For example, gate-induced insulator−metal transition,[7,8] gate-induced superconductivity,[9−13] and the modulation of the charge density wave state[14] have been observed through the EDL gating method. However, intrinsic properties of these liquid electrolytes such as glass transition often exert huge stress
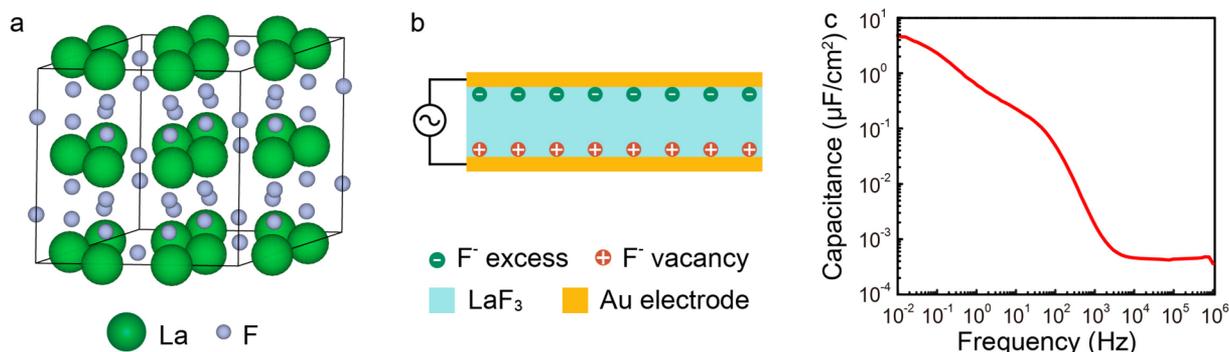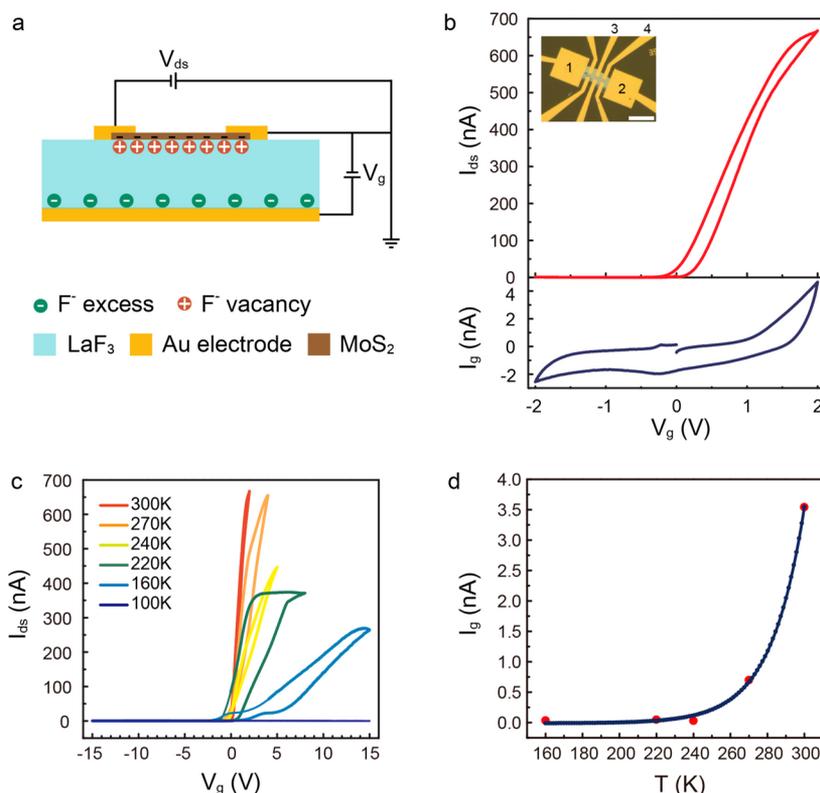
Figure 1. (a) Crystal structure of LaF_3. Fluorine ions transport in the crystal via hopping assisted by the naturally existing fluorine vacancies. (b) Schematic diagram of a LaF_3 EDLC and (c) capacitance−frequency plot of a LaF_3 EDLC in this geometry.


Figure 2. (a) Schematic diagram of a MoS_2/LaF_3 EDLT when $V_g > 0$. (b) Typical transfer curve and gate leakage current observed in MoS_2/LaF_3 EDLTs at $V_{ds} = 0.5$ V. Inset: optical image of the Hall bar device. (Scale bar: 10 μm.) V_{ds} is applied across pins 1 and 2. I_{ds} is measured using the four-probe method across pins 3 and 4. (c) Temperature-dependent transfer curves measured on a MoS_2/LaF_3 back-gate device from 300 to 100 K. (d) Temperature-dependent gate leakage current measured at a channel resistance of 28 kΩ, showing an exponential decay with decreasing temperature.

between electrolyte and channel material as temperature varies, and thus, devices are damaged easily. In addition, given the liquid nature, possible side reactions and sensitivity to moisture further complicate device fabrication and physical/chemical measurement. The liquid coverage also limits the access to the active device surface and makes many surface or *in situ* characterizations challenging.

To resolve these undesirable properties due to the liquid nature, researchers started exploring the potential of solid-state electrolytes as gating dielectric to provide the essential EDL. In recent years, several solid-state electric-double-layer transistor (EDLT) systems based on different types of ions have been experimentally demonstrated. For example, microporous SiO_2 thin films[15] and a chitosan-based electrolyte[16] were demon-

strated to provide EDL gating via proton conduction. The use of lithium- and sodium-based solid electrolytes as potential alternatives has also been demonstrated.[17−19] While cations provide excellent EDL capacitance in these systems, the use of anions as the charging media in solid-state EDLTs has not been explored before.

In this work, we demonstrate EDL gating-induced insulator−metal transition in two-dimensional MoS_2 achieved by lanthanum fluoride (LaF_3), a solid-state superionic conductor which conducts fluorine ions. EDLTs are fabricated with few-layer and monolayer MoS_2, an archetypal layered semiconductor. An on/off ratio of 10^4-10^5 is observed in all measured MoS_2 EDLTs, regardless of the channel thickness, with the maximum induced carrier density up to 4.1×10^{13}
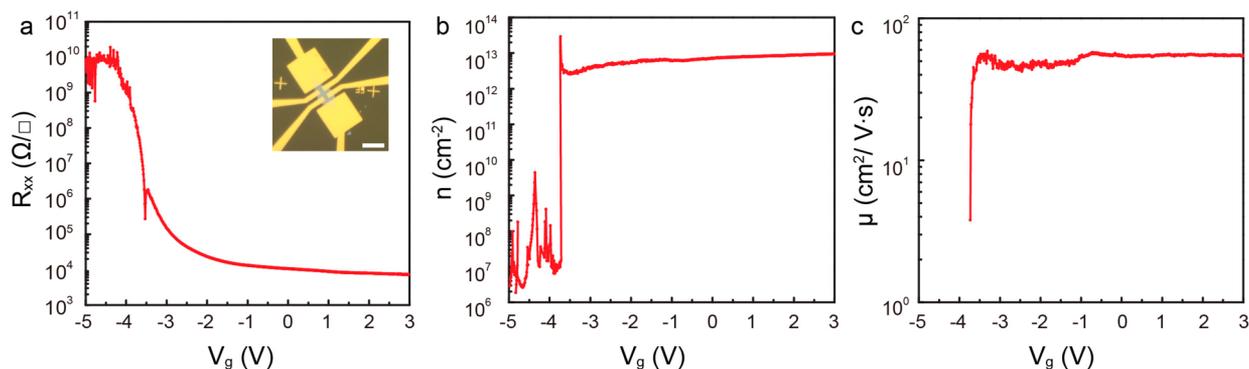
Figure 3. Electronic property modulation through fluorine ion gating. Gate bias-dependent (a) sheet resistance, (b) corresponding carrier density, and (c) mobility measured at 220 K. Inset: optical image of the device. (Scale bar: 10 μm.)

cm^{-2}, showing large carrier modulation capability. By tuning the carrier density under varying gate voltages, we are able to induce an insulator−metal transition in MoS_2. The device shows consistent transfer characteristics after cycles of cooling over a week of measurement, showing the chemical stability of LaF_3 gating. In addition, the direct access of the surface area of MoS_2 facilitates in situ Raman measurements, which can serve as an additional probe of carrier density modulation. The successful demonstration of crystalline LaF_3-based EDLT establishes LaF_3 as a new member of solid-state ionic gating dielectrics and provides a convenient option to achieve high carrier density.

Figure 1a shows the crystal structure of LaF_3 (space group $P6_3/mcm$),[20] which is a well-known fluoride ion conductor.[21,22] Because of the fluorine vacancies already existing in the crystal, fluoride ions (F^-) can transport by hopping throughout the crystal lattice while lanthanum ions stay immobile due to their large size and mass.[23] Due to the insulating behavior of LaF_3 (bandgap ∼4.9 eV) and its mechanical stability, LaF_3 can serve as both the substrate and gate dielectric, compatible with silicon-based device fabrication processes. Figure 1b shows the schematic illustration of a LaF_3 electric-double-layer capacitor (EDLC) in a parallel plate geometry. Once an external bias is applied, the charges accumulate on the two metal plates, creating an electric field across the electrolyte that drives the movement of F^-. While F^- move toward the plate that is positively charged, the negatively charged plate is left facing the side with an excess of fluorine vacancies which carry effective positive charges. At equilibrium, EDLs based on F^- accumulation and depletion form at the two opposite metal plates, respectively, creating nanoscale capacitors and a large electric field at the interface.

To briefly understand the charging mechanism of the LaF_3 system, electrochemical impedance spectroscopy is performed. Figure 1c shows the frequency-dependent capacitance for the Au/LaF_3/Au sandwich structure which bears resemblance to the back-gate geometry of a transistor. The frequency regime above 1 kHz, characterized by a small capacitance, represents the capacitance coupling (geometry capacitance) directly between the two metal plates across the total thickness of bulk LaF_3. As the frequency decreases from 1 kHz to 10 Hz, the capacitance rapidly increases. As the frequency decreases below 10 Hz, the capacitance slightly increases to the maximum value of about 4 μF/cm^2, which corresponds to the typical EDL polarization at the electrode surface. In this regime, two different nanogap capacitors form at two opposite electrodes due to the accumulation and depletion of F^-, respectively,

providing the EDL capacitance used in EDLTs. This frequency-dependent capacitive behavior of LaF_3 closely resembles that of ionic liquids which has been extensively demonstrated in the literature.[24] The important method of exploiting the pure electrostatic nature of EDL at lower temperatures, which is established from ionic liquids, is applied to our study and will be discussed later.

To exploit the EDL capacitance for transistor applications, MoS_2 is exfoliated onto LaF_3 as the semiconductor channel and Hall bar pattern is fabricated (Figure 2b inset) for the measurement of transfer characteristics. Figure 2b shows the transfer curve measured at 300 K. A clear n-type conduction with an on/off ratio of 10^5 at a small gate voltage of 2 V can be observed, indicating successful carrier density modulation. The corresponding gate current at $V_g = 2$ V is about 5 nA, which is 2 orders of magnitude lower than the source-drain current (I_{ds}). However, as V_g increases beyond 2 V, the gate current increases rapidly, eventually reaching tens of nA, but is still much smaller than the I_{ds}. To guarantee reliable operation of the device, the voltage window at room temperature is therefore limited to ±2 V. Carrier density modulation by LaF_3 is further confirmed with in situ gate-dependent Raman measurement (Supporting Information, Figure S2). With increasing gate bias, clear suppression of both A_{1g} and E_{2g} peaks can be observed at an excitation wavelength of 633 nm, consistent with previous reports.[25,26] The gradual disappearance of these two vibration modes indicates the electron filling of the K and K′ valleys, leading to Pauli blocking effect and reduced absorption of the incident laser.[27]

To explore the suitable operation temperature and voltage window of LaF_3-based EDLTs, temperature-dependent transfer curves are measured (Figure 2c). The goal of operating at a lower temperature is to achieve the same degree of channel modulation without inducing undesirable electrochemical reactions. A gate current of about 3−5 nA is thus used as the criterion to determine the suitable voltage window at each temperature. Current modulation can be achieved from room temperature down to 160 K and is completely suppressed at 100 K. To determine the suitable operation temperature, the magnitude of gate current at a channel resistance of ∼28 kΩ, which is the lowest resistance at room temperature on this device, is examined (Figure 2d). The gate current monotonically decreases from 3.5 nA at room temperature to below 0.1 nA at 240 K, reaching the minimum of 0.035 nA at 160 K. This decrease exhibits an exponential decay, reflecting the thermally activated vacancy hopping of F^-. Hysteresis can be observed to slightly increase with decreasing temperature due to the slower
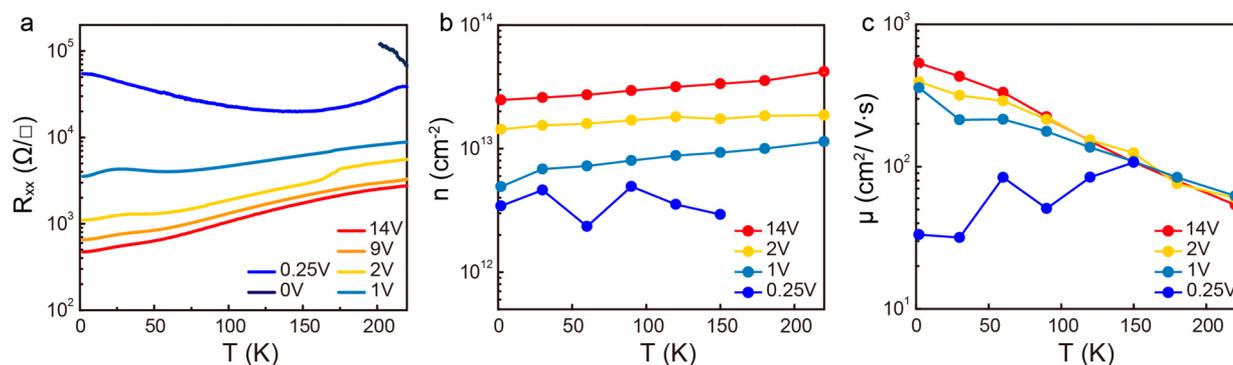
Figure 4. Low-temperature measurement on MoS_2/LaF_3 EDLT. (a) RT curves measured under different gate voltages showing gate-induced insulator−metal transition. Temperature-dependent (b) carrier density and (c) mobility measured under different gate bias.

ion movement at lower temperature, resulting in the delayed response of F^- when the scanning direction of V_g is reversed. However, the degree of this hysteresis also differs from device to device due to different amounts of trapped charges introduced. Note that the hysteresis is still smaller than that observed in ionic liquids at the same temperature for all the devices we measured. Considering all the above-mentioned factors, the temperature range for operation based on the minimization of gate leakage current lies in the range 220−240 K.

To examine the tunability of electronic properties on MoS_2 with LaF_3 gating, transfer characteristics and the corresponding sheet carrier density n_s and mobility are measured at 220 K. Within a gate voltage from −5 to 3 V, the channel resistance is tuned from more than 1 GΩ/□ to several kΩ/□ (Figure 3a), crossing the critical value of resistance for the insulator−metal transition in MoS_2. From Hall measurements, we may extract the carrier density and mobility at each gate bias condition, as shown in Figure 3b,c. In the high conductance regime from −2 to 2 V, the sheet carrier density n_s is on the order of $10^{12}-10^{13}$ cm^{-2}. Mobility in the more conductive regime is around 55−60 cm^2/(V s) and stays approximately constant within this voltage range, with a lower mobility at low gate voltage. This variation of mobility with V_g can be attributed to the formation of the two-dimensional electron gas owing to the surface band bending of MoS_2 near the interface.[28−30] At a higher V_g, the carriers start to be confined in the gradually formed potential well, resulting in enhanced mobility.

Low-temperature transport properties of the MoS_2 channel with charge carriers accumulated at 220 K are measured at multiple V_g values. As shown in the sheet resistance−temperature (RT; sheet resistance, R_s) curve in Figure 4a, a clear insulator−metal transition induced by gate electric field can be observed. At V_g = 0 V, R_s increases rapidly with decreasing temperature and exceeds the measurement limit. For V_g = 0.25 V, R_s first decreases at 220 K until around 150 K and then increases again as the temperature further decreases. As V_g increases from 0.25 to 1 V, R_s at 220 K decreases from 29 kΩ/□ to 8.8 Ω/□, crossing the quantum of resistance (25.6 kΩ/□). When V_g > 1 V, R_s always decreases with cooling despite some small bumps in the RT curves, which is the sign of metallic behavior and indicates the transition from an insulator to metal within a low gate voltage V_g = 0.25−1 V.

Temperature-dependent carrier density and mobility at the corresponding V_g are also extracted from Hall measurements and summarized in Figure 4b,c. At V_g < 1 V, the channel is in the insulating state with a high sheet resistance and a low carrier density. The mobility is observed to drop with decreasing temperature, from 107 cm^2/(V s) at 150 K to 33 cm^2/(V s) at 2 K, which can be attributed to the hopping transport of electrons (either variable-range hopping or thermally activated hopping mechanism depending on the temperature regime[31]). From V_g = 0.25 to 1 V, the carrier density increases over 1 order of magnitude, exceeding 1×10^{13} cm^{-2}, and is well-retained on the same order down to 2 K. For V_g > 1 V, the carrier density further increases and reaches a maximum of 4×10^{13} cm^{-2} at V_g = 14 V. In this regime ($V_g \geq 1$ V), the material exhibits metallic behavior and shows the typical bandlike electronic transport.[4,32,33] The mobility increases monotonically with decreasing temperature, eventually reaching a maximum of about 532 cm^2/(V s) at 2 K without any sign of saturation for the most conducting case. It is worth noting that the maximum mobility measured in our device is the highest mobility ever reported for EDL gated MoS_2, which can be attributed to a more uniform electric potential distribution at the EDL interface due to the crystalline LaF_3 lattice than the charged molecules in ionic liquids.

Compared with ionic liquids and lithium-based solid electrolytes, LaF_3 provides a lower areal capacitance, which results in the lower carrier density achieved in these LaF_3-based EDLTs. This lower capacitance may result from the following factors: (1) density of the mobile ions, which is related to the amount of charges that can be accumulated in the EDL, and thus, the carrier density; (2) mechanism of electron accumulation (even though the intercalation process depends on the range of applied voltage, it is much easier to have smaller Li^+ ion intercalation than larger F^- ions; therefore, it is more likely that Li-based electrolytes could have contribution from both electrostatic gating and electrochemical intercalation, leading to larger charge accumulation; however, further increasing the voltage may result in the decomposition of MoS_2, forming Li_2S); and (3) quality of the solid electrolyte/channel material interface. While liquids or gels can easily wet the surface of the channel and form good contact, a solid/solid interface is more problematic in terms of the quality of the contact at the interface. Factors such as surface roughness or trapped moisture or molecules during device fabrication may prevent the formation of uniform contact of ions with the entire channel material. Despite these issues, it is possible to enhance the gating performance by improving the fabrication process, annealing for better contact, or adjusting the density of mobile ions in LaF_3.

In summary, we present the solid-state anionic EDLT using a LaF_3 superionic conductor with mobile fluoride ions as the

charging media. The mechanical robustness of LaF$_3$ allows it to be used as a substrate that is compatible with current semiconductor technology. In addition, the large EDL capacitance and fast ion conduction enable the realization of solid-state devices exhibiting comparable performance to ionic-liquid- and electrolyte-based devices without the issues of strain, air-sensitivity, and electrochemical reactions/intercalation. With the powerful carrier modulation ability, we are able to induce a metal−insulator transition in layered MoS$_2$. Our results demonstrate that LaF$_3$ is a powerful material for ionic gating and can serve as the next generation EDLT that is compatible with *in situ* and surface characterizations, opening new possibilities for their study.

Method. *Impedance Measurement.* Shadow mask metal deposition is first performed on a LaF$_3$ crystal to define the electrodes on both sides for the impedance measurement. Electrochemical impedance spectroscopic measurements are conducted with a Biologic VSP potentiostat in the frequency range from 10 mHz to 1 MHz. To measure the impedance across the substrate, one electrode on each surface is connected to the potentiostat. To measure the in-plane impedance, two electrodes directly across from each other are connected.

Device Fabrication. Multilayer MoS$_2$ devices for transport measurements are made by mechanical exfoliation from bulk crystal directly onto LaF$_3$ substrates (commercially available from Crystran Ltd., doped with 0.3% mol Eu). On the other hand, monolayer MoS$_2$ devices for Raman measurements are made by PMMA-assisted transfer of CVD grown MoS$_2$ from SiO$_2$/Si substrates. After the channel material is transferred onto the substrate, standard electron beam lithography is performed to define the electrodes. Since the substrate is insulating, e-spacer is applied prior to the write. Metal deposition of Cr/Au (5/50 nm, for bonding pads) and Au (50 nm, for electrodes) is performed afterward, followed by acetone liftoff. The gate electrode is defined by either evaporation of Cr/Au (5/50 nm) or silver epoxy (as the back gate) that requires curing.

Transport Measurement. All transport measurements are performed in a physical property measurement system (PPMS, Quantum Design) equipped with a 9 T superconducting magnet. Transfer curves are measured at a scan rate of 10 mV/s using Keithley 2400 source meters as the voltage supply. Temperature-dependent characterizations of sheet resistance, carrier density, and mobility are conducted using the low-frequency AC technique with digital lock-in amplifiers (Stanford Research Systems SR830) in the current-driven configuration. A cooling rate of 3−5 K/min is used to avoid rapid thermal expansion/contraction. Hall measurements are performed within the magnetic field range from 9 T to −9 T to extract the carrier density and mobility. The four-point probe configuration is adopted throughout all measurements.

Raman Characterization. Raman spectra are collected under ambient condition with a Horiba Labram HR evolution Raman System using a laser excitation of 633 and 532 nm with 1800 lines/mm grating. Side-gate devices are used, and the bias is applied with a Keithley 2400 source meter.

■ ASSOCIATED CONTENT

ⓈSupporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nano-lett.7b05377.

Capacitance of LaF$_3$ in a side-gate geometry, gate-dependent Raman spectra, and transfer curves showing the chemical stability of LaF$_3$ gating (PDF)

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Notes
The authors declare no competing financial interest.

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