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24. This work was partly supported by Defense Advanced Research Projects Agency (DARPA/ARO) under contract number DAAD19-00-C-0096. We acknowledge useful discussions and help from K. Steeples, M. L. Peabody, A. Straub, K. Baldwin, A. Erbe, and R. Paiella. We thank R. Martini for lending the micro-bolometer camera. K. S. thanks the Hertz Foundation for financial support.

Supporting Online Material
www.sciencemag.org/cgi/content/full/1090561/DC1
Materials and Methods
SOM Text
Figs. S1 to S3
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18 August 2003; accepted 14 October 2003
Published online 30 October 2003;
10.1126/science.1090561
Include this information when citing this paper.

Nanowire Crossbar Arrays as Address Decoders for Integrated Nanosystems

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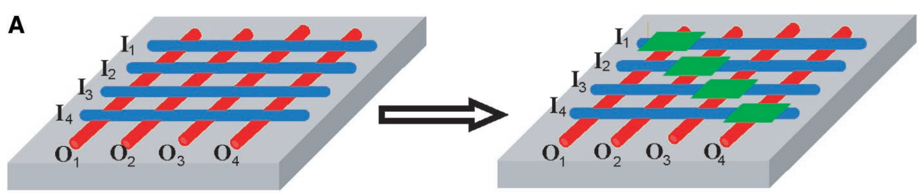
The development of strategies for addressing arrays of nanoscale devices is central to the implementation of integrated nanosystems such as biological sensor arrays and nanocomputers. We report a general approach for addressing based on molecular-level modification of crossed semiconductor nanowire field-effect transistor (cNW-FET) arrays, where selective chemical modification of cross points in the arrays enables NW inputs to turn specific FET array elements on and off. The chemically modified cNW-FET arrays function as decoder circuits, exhibit gain, and allow multiplexing and demultiplexing of information. These results provide a step toward the realization of addressable integrated nanosystems in which signals are restored at the nanoscale.

The past several decades have witnessed major advances in computing that have resulted from systematic reductions in feature sizes and the corresponding increases in integration densities achieved by the semiconductor industry (*1*). Recognition of possible barriers to the continuation of these trends has led to substantial work focused on exploring nanoscale device elements, including molecules (*2*, *3*), carbon nanotubes (NTs) (*4*–*7*), and semiconductor nanowires (NWs) (*8*–*10*), and on developing methods for the creation of organized and interconnected high-density arrays of these elements (*11*–*14*). Considerable progress has been made recently in both of these areas, although integrated architectures for nanocomputing will also require schemes for addressing elements within arrays at the nanoscale (*15*). The importance of being able to address nanoscale elements in arrays goes beyond the area of nanocomputing and will be critical to the realization of other integrated nanosystems such as chemical/biological sensors (*16*, *17*) and electrically driven nanophotonics (*9*, *18*).

We report an approach to this general problem based upon a scalable crossed-nanowire field-effect transistor (cNW-FET) architecture, in which molecular-level modification of specific cross points within arrays is used to define an address code that enables NW input lines to turn on and off specific output lines. This basic array structure functions as an address decoder, with signal restoration at the nanoscale because of the inherent gain of the cNW-FET elements. The underlying issue for addressing can be understood when we consider a regular cNW-FET array (Fig. 1A) that consists of *n*-input (I_1, I_2 . . . I_n) and *m*-output (O_1, O_2 . . . O_m) NWs, in which outputs are the active channels of FETs and the inputs function as gate electrodes that turn these output lines on and off (*10*). When a voltage is applied to I_n in a regular array, it will affect each of the output NWs in the same way, which precludes selective addressing of elements. We overcame this critical limitation by differentiating cross points such that inputs affected only specific output cross points in the array. In the simplest scenario in which one output NW is turned on or off by a single input, differentiation of diagonal elements of a square array (Fig. 1A)

A



B

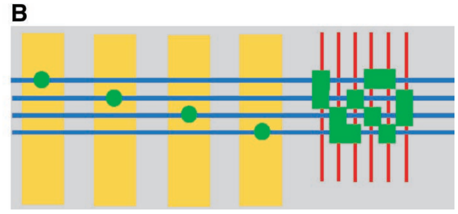


Fig. 1. Crossed NW array–based address decoders. (**A**) A 4 by 4 cNW-FET array with four horizontal NWs (I_1 to I_4) as inputs and four vertical NWs (O_1 to O_4) as signal outputs. The four diagonal cross points in the 4 by 4 cNW-FET array were chemically modified (green rectangles) to differentiate their responses to the input gate lines. This produced a 1-hot code in which I_n turns O_n on or off. (**B**) Bridging between microscale metal wires (yellow) and denser nanoscale NWs is achieved with a 2-hot code (green rectangles), whereby two inputs (blue NWs) are required to address each output (red NWs). The input NWs can be turned on or off by specific microscale wires with a simple 1-hot code.

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produces a code where $I_1, I_2 \ldots I_n$ address $O_1, O_2 \ldots O_n$, respectively. This idea can be generalized to enable a small number of input NWs to address a larger number of output NWs if two or more inputs are used to turn on or off a given output (*15*), or similarly, a small number of lithographically defined wires could address a much denser array of NWs (Fig. 1B), as required to bridge between micro- and nanoscale features.

The cNW-FET devices and arrays in these studies were assembled from silicon NW building blocks with fluid-directed assembly (*11*). NWs were prepared as core/shell Si/SiO_2 structures (*19*, *20*) in which the oxide shell serves as an integral, controlled-thickness gate dielectric that can be further manipulated with surface chemistry (*21*). Representative electrical transport data (Fig. 2A) recorded on a single cNW-FET before and after surface modification (*22*) demonstrate the substantial effect that the modification had on the gate response. In general, we modified the surface of the array by lithographically defining an opening around desired cNW junctions and then treating the junctions with an aqueous or ethanol solution of tetraethylammonium chloride (*22*). Before modification, the depletion mode device exhibited a threshold voltage of ~5 V, and after modification, this threshold shifted to ~1.5 V (*23*). Measurements made on more than 30 individual cNW-FET devices show that this large threshold voltage shift is reproducible. Specifically, a histogram (Fig. 2B) summarizing threshold voltages before and after modification yielded average ± 1 standard deviation values of 5.4 ± 0.8 and 1.5 ± 0.4 V, respectively. In addition, the threshold shift was stable. We found that modified cNW-FET devices could be turned on and off at least hundreds of times, and that the threshold shift was stable for at least a week.

The substantial and reproducible shift in threshold voltage observed for individual cNW-FETs strongly suggests that surface modification could be used to differentiate specific cNW-FET elements in an array to produce an address decoder circuit. We tested this idea first in a 2 by 2 cNW-FET array (Fig. 3A). Conductance versus applied NW input gate voltage data (Fig. 3B) shows that, before modification, each of the four cNW-FET elements remained on for voltages greater than 2 V. After specific modification of the I_1/O_1 and I_2/O_2 elements, these devices could be turned off with a gate voltage of ~1 V, whereas the off-diagonal elements remained unaffected for the same input voltage. Hence, when I_1 was set to 1 V and I_2 was set to 0 V, only O_2 was active, with an output of 2 V, and O_1 was off with an output of 0 V (Fig. 3C). O_1 could be selected as well when I_1 was set to 0 V and I_2 was set to 1 V, yielding an output of 2 V. The 2 by 2 array thus functioned as an address decoder circuit for multiplexing and demultiplexing signals. In addition, these results show that our FET-based NW decoder had a large-signal gain of 2; that is, an input of 1 V yielded an output of 2 V. The specific value of large-signal gain depends on the measurement parameters. However, small-signal gain characterization of individual devices yielded values of at least 5, and optimization of the FET channels (*21*) could lead to an increase in transconductance, which would further enhance small-signal gains. The gain observed in these devices was distinct from results obtained with molecular diode switches (*13*, *24*) and suggests that it will be possible to achieve signal restoration with our cNW-FET decoder without external transistor devices for signal amplification.

We investigated the potential to scale the cNW decoder concept to larger circuits by assembling and characterizing a substantially larger 4 by 4 array (Fig. 3D). Measurements of conductance versus applied NW input voltage (fig. S1) show that, before surface modification, all of the 16 cNW-FET elements remained on for voltages greater than 3 V. However, after specific modification of the four diagonal I_n/O_n elements, these FETs could be selectively turned off by their respective inputs. Hence, by variation of the NW input voltages (Fig. 3E), it is possible to address selectively each of the four

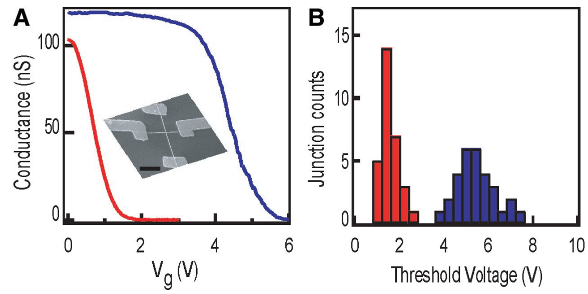

Fig. 2. Molecular-level modification of cNW-FETs. (**A**) Conductance versus gate voltage of a single cNW-FET before (blue) and after (red) treatment with TEA aqueous solution. Inset: An SEM image of a cNW-FET device. Scale bar, 1 μm. (**B**) Histogram of the threshold voltages for 30 cNW-FETs before (blue) and after (red) chemical modification.

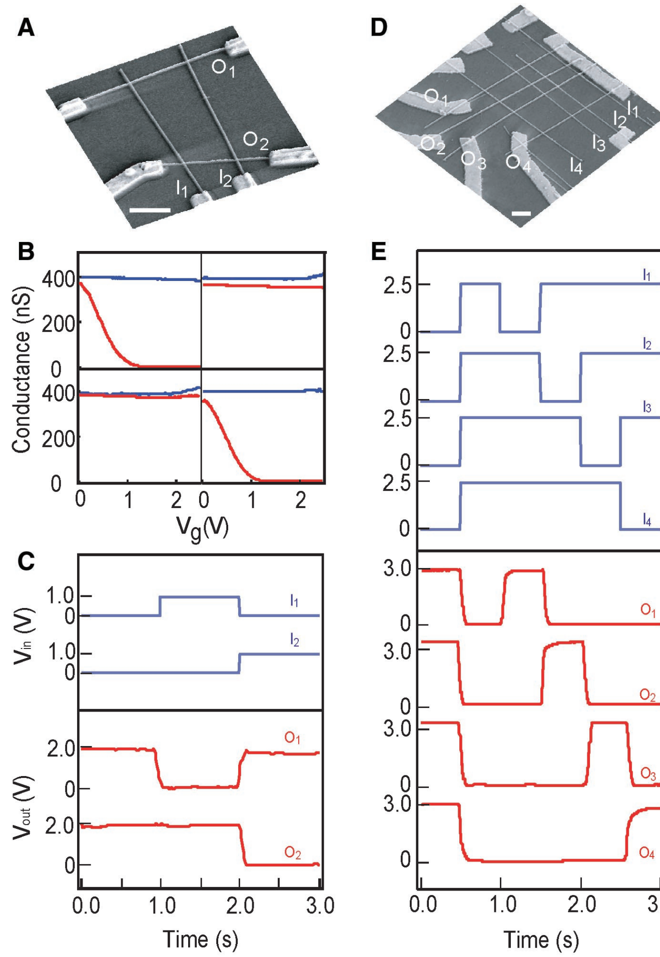

Fig. 3. Crossed NW FET decoders. (**A**) An SEM image of a 2 by 2 cNW-FET decoder. The two diagonal cross points were chemically modified. Scale bar, 1 μm. (**B**) Conductance versus gate voltage for each cross point in the 2 by 2 cNW-FET array before (blue) and after (red) chemical modification. Starting clockwise from the top left quadrant, data are from junctions I_1/O_1; I_2/O_1, I_2/O_2, and I_1/O_2, respectively. (**C**) Real-time monitoring of the gate voltage inputs (blue, V_{in}) and signal outputs (red, V_{out}) for the 2 by 2 decoder. Supply voltage is 3 V, and the load resistance is 10 MΩ. (**D**) An SEM image of a 4 by 4 cNW-FET decoder. The four diagonal cross points were chemically modified. Scale bar, 1 μm. (**E**) Real-time monitoring of the gate voltage inputs (blue) and signal outputs (red) for the 4 by 4 decoder. Supply voltage is 3.5 V, and the load resistance is 40 MΩ. The NW array–based decoder was interfaced to a commercial switching system (a Keithley 7002 switching system with a 7011-S Quad 1 by 10 multiplexer card), and the voltage signals from the decoder output channels were measured sequentially.

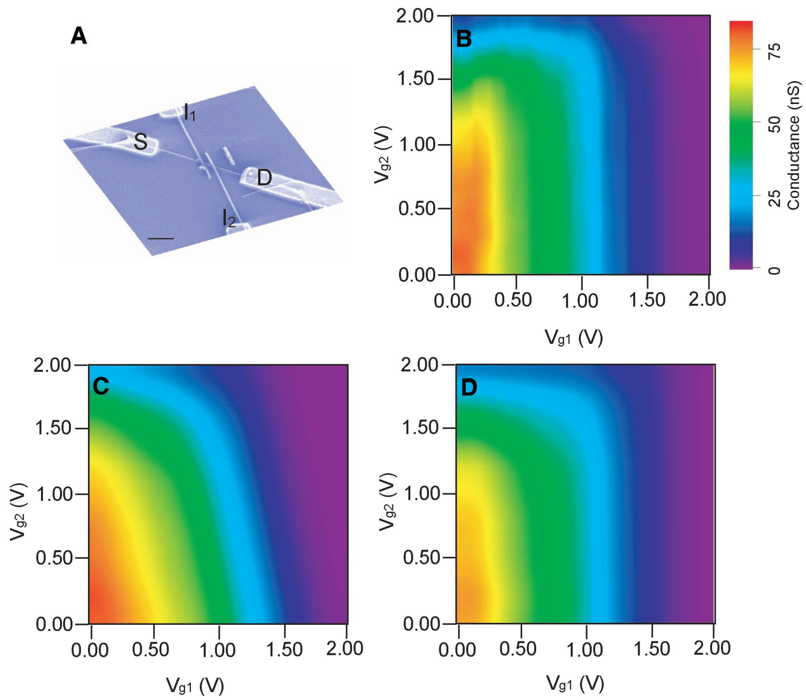

Fig. 4. Investigations of decoder input coupling. (**A**) An SEM image of a cNW-FET with two adjacent input gates, I_1 and I_2. S, source electrode; D, drain electrode. Scale bar, 500 nm. (**B**) Conductance versus gate voltage applied to I_1 (V_{g1}) and I_2 (V_{g2}). (**C** and **D**) Simulations of the conductance versus V_{g1} and V_{g2} (*26*) for the cases in which (C) I_1 and I_2 have 20% coupling ($\alpha = \beta = 0.2$) and (D) I_1 and I_2 are independent ($\alpha = \beta = 0$).

output lines, as required for multiplexing and demultiplexing signals. The output signals can also exhibit finite rise-time (e.g., O_4) that could limit the speed of these circuits. The origin of the observed rise-time can be traced to absorbed water that led to hysteresis in conductance versus input gate voltage curves; reduction of the hysteresis in vacuum suggests that passivation of these structures could effectively eliminate this issue. In addition, the address codes in these arrays were defined with electron-beam lithography, which would not be scalable for large systems; however, methods such as nanoimprint lithography (*13*, *25*) could produce the needed codes in a scalable manner to very high densities.

We also investigated the potential scaling of the cNW-FET decoder concept to higher densities by characterizing the output response to two adjacent input gates with separations an order of magnitude smaller than in the previous arrays (Fig. 4A). A two-dimensional plot (Fig. 4B) summarizing the channel conductance as a function of input voltages I_1 (x axis) and I_2 (y axis) shows several important features. First, each input can independently turn off the FET when the other is set to zero. Second, the two-dimensional conductance plot exhibited a rectangular shape with edges parallel to the x and y axes, which suggests that there is little coupling of the responses due to I_1 and I_2. To confirm this latter point, we simulated (*26*) the responses expected for a two-input cNW-FET when there is 20% coupling between the inputs (Fig. 4C), which would be a conservative limit that still allows a functioning decoder structure, and when the inputs are independent (Fig. 4D). These results show that coupling leads to a pronounced curvature that was not observed in our experimental data; thus, the two inputs act independently on the 250-nm-length scale of this test device. The limits in separation to which this approach can be pushed are not yet known, although by incorporating NWs with axial modulation doping (*27*), it should be possible to achieve working decoders with input separations substantially below 100 nm.

Our studies have shown that molecular-level modification of specific cross points within cNW-FET arrays defines an address decoder architecture that is scalable and exhibits signal restoration at the nanoscale. The cNW-FET decoder could serve as an approach for bridging between microscale wires and dense nanoscale arrays (Fig. 1B). Bridging length scales requires that a limited number of microscale wires address a much larger number of dense nanoscale wires, which can be achieved when more than one input is used to turn each output on or off. For example, a two-input code structure (Fig. 1B) requires only $O(\sqrt{N})$ inputs to address N outputs and is still defect-tolerant (*15*). Extending the present studies in these directions could enable addressing and micro-to-nanoscale integration in a wide range of nanoelectronic and nanophotonic systems.

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23. The large threshold shift is believed to be due to passivation of compensating defects at the surface of the SiO_2 gate dielectric (*21*). This suggestion is supported by studies of silicon NW FETs that exhibit similar threshold shifts after chemical modification with 4-nitrophenyl octadecanoate, which reacts to form covalent C–O(Si) bonds that passivate defects on the SiO_2 surface.
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$$\frac{1}{G_{total}} = \frac{1}{G_1(V_{g1} + \alpha V_{g2})} + \frac{1}{G_2(V_{g2} + \beta V_{g1})} + \frac{1}{G_s}$$
where V_{g1} and V_{g2} are the two input gate voltages, respectively, and α and β correspond to the coupling factors ($0 \le \alpha, \beta \le 1$).
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28. We thank H. Park and A. DeHon for discussion. Supported by the Defense Advanced Research Projects Agency (C.M.L.).

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Fig. S1

28 August 2003; accepted 21 October 2003