Pump–Probe Measurements of CMOS Detector Rise Time in the Blue

Aparna Bhatnagar, *Student Member, IEEE*, Salman Latif, *Student Member, IEEE*, Christof Debaes, *Student Member, IEEE*, and David A. B. Miller, *Fellow, IEEE, Fellow, OSA*

***Abstract*—This paper proposes the use of shorter wavelengths and monolithic integration for chip-to-chip and on-chip optical communication. The promise of monolithic detectors for high-speed interconnection is demonstrated through experimental measurements and matching simulations. Responsivities >0.06 A/W and transit-time-limited response can be expected in the blue from planar p-i-n silicon-on-insulator (SOI) detectors.**

***Index Terms*—Complementary metal–oxide–semiconductor (CMOS) photodetectors, optical clocking, optical interconnects, silicon-on-insulator (SOI).**

I. Introduction

SILICON is ubiquitous in electronics, and it is a good material for photodetection especially at visible wavelengths. The pn-junctions available in standard complementary metal–oxide–semiconductor (CMOS) processes are used for visible light detection in commercial image sensors. CMOS process constraints limit detector performance, but the process is very cost effective and robust with high yield and uniformity. Short-haul optical interconnects are targeted at providing communication between CMOS chips and for timing signals within chips. For these applications, having detectors and circuits closely integrated on the same substrate has density benefits in addition to manufacturability.

Because its bandgap is $\sim$1.1 eV, silicon is transparent at telecommunications wavelengths and has a fairly long absorption depth of $\sim$ 14 μm at 850 nm. One constraint of the CMOS process is the relatively short depletion width of the available pn-junctions. Only carriers generated near a depletion region experience an electric field and get collected quickly. For a 0.25-μm CMOS process, depletion widths are $\sim$ 0.1 μm, while junction depths are typically < 1 μm. Thus, at 850 nm, very few carriers are generated near the junction and collected quickly. Most carriers are generated in the substrate and collected slowly through diffusion. This makes the detector slow. Conversely, the detectors can be made fast at the expense of carrier collection efficiency. For example, clever use of buried junctions in bulk CMOS achieved 1-Gb/s 850-nm detectors while accepting the resulting responsivity decrease [1]. Similarly, silicon-on-insulator (SOI) CMOS processes achieve high-speed 850-nm detectors by eliminating the slow carriers. The responsivity of these detectors suffers due to the uncollected carriers.

The promise of monolithic integration in CMOS for interconnects has inspired many novel detector structures to mitigate the responsivity–speed tradeoff at 850 nm. Among these are resonant cavity enhancement (RCE) detectors using distributed Bragg reflectors (DBRs) [2], transit-time-limited metal–semiconductor–metal (MSM) detectors on SOI [3], roughened membrane MSMs [4], and grating-coupled SOI waveguide detectors [5]. The fabrication of these detectors is compatible with CMOS but requires additional processing and integration. Within standard SOI processes, avalanche-gain-based detectors have been reported, which require no additional steps but may need voltages beyond CMOS supply levels [6]. Trench p-i-n detectors [7] and thicker SOI materials [8] have also been reported. These optimize the balance between speed and responsivity by maximizing the amount of silicon available for absorption at a given speed. For optical interconnects, detector capacitance is another important parameter because it directly impacts receiver bandwidth, voltage swing, and noise. Planar p-i-n detectors in SOI have smaller capacitance than deep trench or bulk detectors of similar active size.

One way to circumvent the responsivity–speed tradeoff is not to use 850-nm light but instead to communicate using shorter wavelengths. Short-distance optical interconnects such as those within a computer may well be free space rather than fiber based; thus, fiber loss is not a consideration in the choice of wavelength. 850 nm has been a popular wavelength for short-haul optical links because of the availability of low-cost transmitters. A particularly attractive shorter wavelength for interconnects may be 425 nm, obtained by frequency doubling traditional 850-nm sources. Arrays of frequency-doubled extended-cavity surface-emitting lasers in the blue are commercially available and targeted at low-cost markets [9]. Practical high-power transmitters for such short wavelengths may still present a challenge, but for clock injection, short-pulse sources would appear to be viable, for example, by frequency doubling known infrared sources. The ultrashallow junctions available in CMOS are ideal for detecting blue and ultraviolet (UV) [10]. Silicon has an absorption depth of $\sim$100 nm in the blue ($\lambda = 400$ nm). Therefore, at this wavelength, most of the photogeneration would occur within the depletion region, making CMOS detectors potentially fast and efficient in the blue.

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The efficiency of SOI and bulk CMOS in the visible has been researched for image sensor applications [11], [12]. Optical interconnects require much greater detector speeds than these applications. Optical clock injection further requires fast rise times. To the authors' knowledge, no research has investigated the viability of using blue wavelengths and CMOS photodetectors for high-speed interconnects. This paper presents experimental measurements of the rise time of monolithic CMOS detectors in an ultrathin SOI process with blue light. Using a pump–probe measurement, the temporal response of the planar p-i-n detectors is resolved with subpicosecond accuracy. The detectors are found to be transit time limited and scalable. The detector rise times are measured to be ∼100 ps, and the simulations of smaller spacing detectors show ∼20-ps rise times are possible in this technology.

II. Device Structure

The SOI CMOS photodetectors studied in this paper were fabricated by Peregrine Semiconductor in their commercial 0.5-μm silicon-on-sapphire process. The silicon in this process is 100 nm thick and is deposited on top of a sapphire substrate. An intrinsic silicon layer is available allowing fabrication of multifingered lateral p-i-n structures simply by laying out any length of intrinsic silicon between heavily doped N and P regions as shown in Fig. 1. Here, we report on a detector with 6-μm finger spacing with an overall size of 20×20 μm. The calculated capacitance of this photodetector is ∼3 fF. The measured responsivity of the photodetectors is 0.066 A/W at 425 nm, and <0.001 A/W at 850 nm. Because the energy per photon is higher at 425 nm than at 850 nm, the maximum possible responsivity at 425 nm is lower ∼0.34 A/W. The measured value of 0.066 A/W corresponds to 20% efficiency. This is reasonable in the context of the specific CMOS process used here for three reasons. First, the silicon thickness in this process is only 100 nm, whereas the absorption depth of 425-nm light in silicon is 180 nm [13]. Thus, only ∼43% of the incident light is absorbed. Second, the silicon–sapphire interface contains carrier recombination sites or traps that lower the carrier lifetime and further reduce the number of carriers collected. Third, since no antireflection (AR) coating is used on the chip, ∼20% of the light is expected to be lost to the first surface reflection. With thicker SOI processes, with, for example, 600-nm-thick silicon, a better responsivity can be expected. The measured responsivity of 0.066 A/W is reasonable for this process and demonstrates the improved efficiency of CMOS detectors in the blue relative to 850 nm. Further improvement can be shown by using an SOI process where the interface trap density is low, which is the case when the insulator is silicon dioxide, for example, and by using an AR coating.

For comparison, Fig. 2 shows the structure of a silicon detector in a standard 0.25-μm bulk CMOS process. The process is twin-well, and the available pn-junctions are shown in gray. Detectors in the bulk process have greater capacitance than SOI detectors because, in the SOI case, the junction edge toward the substrate is absent. Further, the availability of intrinsic silicon in SOI allows lower capacitance lateral p-i-n structures, whereas only pn-junctions are available in the bulk process. Another difference between bulk and SOI is the deeper and wider well–epi junction available in bulk. Depletion widths for the surface and well junctions are $\sim$ 0.1 μm and $\sim$ 0.4 μm respectively. The low-doped epi layer is not available in all bulk processes.

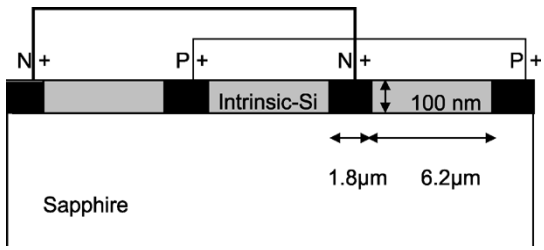

Fig. 1. Schematic cross section of a two-finger lateral p-i-n SOI photodetector.

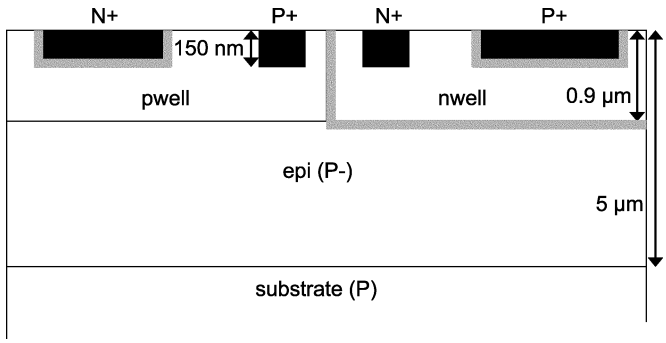

Fig. 2. Schematic cross section of photodetectors in a bulk CMOS process. Junction areas are shown in gray.

III. Pump–Probe Experiment on SOI

The speed of the SOI detectors was characterized in a pump–probe experiment. A blue light pulse train (pump beam) was generated by frequency doubling a 160-fs-pulsewidth mode-locked Ti–Sapphire laser centered at 845 nm in a 1-mm-thick beta–Barium–borate (beta–BaB204 or BBO) crystal. A total of 20 mW of average blue power was available for experiments. The laser pulse repetition period was 12 ns. A dichroic beamsplitter separated the two wavelengths after the conversion. The blue pulse train (pump beam) was focused onto the SOI CMOS photodetector. Part of the remaining unconverted 850-nm pulse train was used as the probe beam for modulators that measured the electrical response of the circuit.

We integrated the SOI CMOS chips with electroabsorption modulators via flip-chip bonding so that we could optically characterize the temporal response of the silicon detectors to blue light. Fig. 3(a) is a top-view microscope picture of the integrated modulators and CMOS detectors. The modulators are molecular-beam-epitaxy-grown GaAs–AlGaAs multiple-quantum-well (MQW) p-i-n diodes based on the quantum-confined Stark effect (QCSE) [14]. The QCSE leads to the absorption of this device being voltage dependent. For example, if we shine a beam of wavelength 845 nm on the specific modulators we used, it will absorb progressively less of the beam as the voltage across the modulator increases.

The modulators are connected to the CMOS detectors as shown in Fig. 3(b). By fixing the voltage on the p-side of the modulator and measuring the intensity of the reflected light from it, we have a signal that is proportional to the voltage

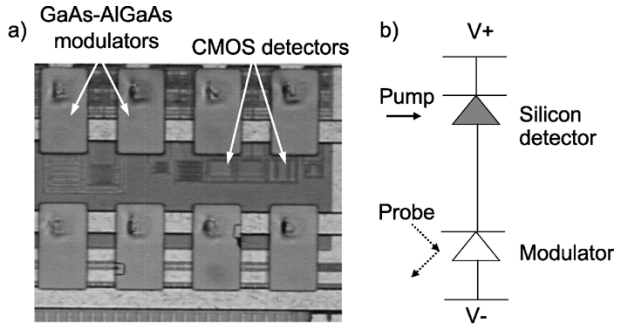

Fig. 3. (a) Flip-chip-bonded GaAs–AlGaAs MQW devices with monolithic CMOS detectors. (b) Schematic of dectector–modulator connection.

on the n-side, which is connected to the CMOS detector. As shown in Fig. 3(b), the 425-nm pulse train (pump) on the silicon photodetector raises the voltage on the modulator. The pulse train on the modulator (probe beam) is delayed relative to the pump using a corner-cube reflector on a computer-controlled delay stage. As the delay of the probe pulse train is swept, the voltage rise caused by the CMOS detector is mapped out via the QCSE. Using a polarizing beamsplitter and a quarter-wave plate, reflected probe light from the modulator is deflected to a fiber-coupled photodetector and measured on a lock-in amplifier. A chopper in the path of the pump pulse train modulates the beam at the frequency to which the lock-in amplifier locks. The experimental setup is shown in Fig. 4.

Fig. 5 is a plot of the reading from the lock-in as a function of relative delay between pump and probe. At ∼0 ps, the pump pulse arrives. As the voltage on the modulator rises, its absorption decreases, leading to a rise in the lock-in signal. Sweeping the arrival time of the probe with respect to the pump maps the voltage rise caused by the CMOS photodetector with picosecond precision. Fig. 5 shows the signal for three different biases. This voltage remains high until sufficient pull-down current from the modulator can sweep out the charge and restore the node to the negative supply. The pump and probe beam powers are constant across the three curves. The signal swing can be seen to increase with voltage. The increase is not expected to be exactly proportional to the voltage as the modulators are not exactly linear over all voltage ranges. Independent modulator contrast ratio measurements indicate that the total signal swing in Fig. 5 corresponds to a ∼4-V rise in the voltage. Focusing an additional pull-down continuous-wave beam on the modulator for additional pull-down did not decrease the reset voltage, indicating the node was swinging fully to the negative supply.

The 10%–90% rise times for the three curves are 104, 107 and 113 ps, respectively, for the 4-, 4.5-, and 5-V biases. The detector finger spacing is 6 μm; thus, for a 4.5- V bias, the corresponding field is 0.75 V/μm. The drift velocity of holes in silicon at 0.75 V/μm is $\sim 2.5 \times 10^6$ cm/s while that of electrons is $\sim 7.5 \times 10^6$ cm/s [15]. Thus, the expected full-swing rise time for a transit-time-limited detector is between 80 and 250 ps, with the 10%–90% rise time being slightly less. We see that the data agree reasonably well with this estimate. Transit-time-limited transport is encouraging because it indicates the detector rise time can be decreased by simply decreasing the finger spacing. Spacings down to 1.2 μm are possible in this SOI process without design rule violation. A simple proportional scaling leads us to expect detectors with this spacing would have <20-ps rise time.

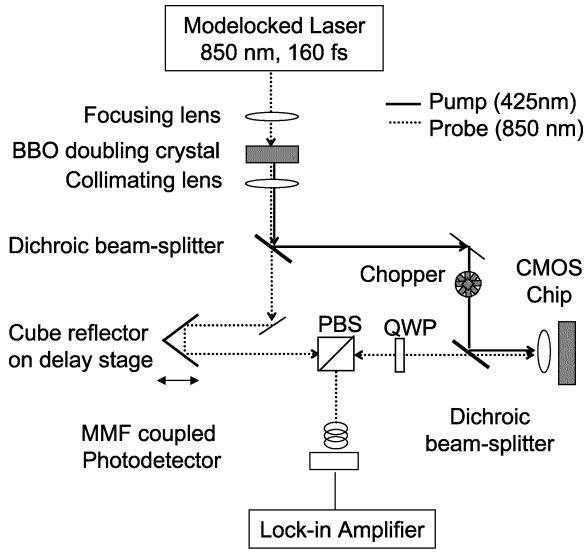

Fig. 4. Experimental setup for pump–probe measurement.

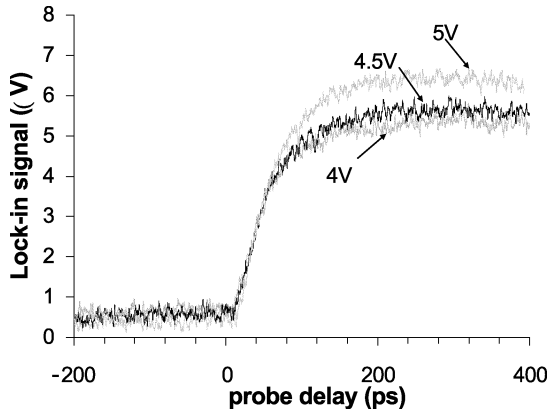

Fig. 5. Pump–probe measurements of the rise time of a 6-μm finger-spacing planar p-i-n SOI detector for 4-, 4.5-, and 5-V bias.

Fig. 6 shows device simulation results for the rise time of SOI detectors with 5-V bias. The device structure in Fig. 1 was simulated in MEDICI with a short-pulse optical input impinging on the detector at time zero. The integrated photocurrent or, equivalently, the total charge collected at the detector terminal is plotted as a function of time for 6- and 1.2- μm finger-spacing p-i-n SOI detectors. The simulation shows a 10%–90% rise time of 120 ps for the 6-μm detector, validating our experimental measurement. MEDICI calculates a rise time of 15 ps for the 1.2-μm detector.

IV. Electrical Sampling of Bulk CMOS Detectors

To characterize the temporal response of CMOS detectors in the 0.25-μm bulk process, we designed high-impedance electrical samplers with 5-GHz bandwidth on the CMOS chip. (This chip was not configured for modulators attached directly beside the detectors as in the previous SOI case.) A simplified graphic of the sampling circuit is shown in Fig. 7. An optical

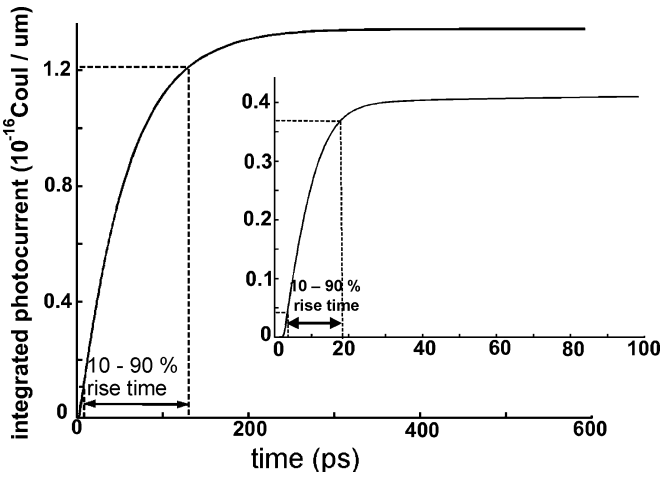

Fig. 6. MEDICI simulations of the integrated photocurrent versus time for planar p-i-n SOI detectors with 5-V bias for 6-μm and, in the inset, 1.2-μm finger spacing.

pulse train from the Ti–Sapphire mode-locked laser is focused onto the CMOS detector. The laser produces 160-fs pulses at a repetition period of 12 ns. Every 12 ns, the voltage across the detector is reset to the supply and then released, allowing the photocurrent in the CMOS detector to discharge the voltage. The sample clock is an electrical signal also synchronized to the repetition period of the laser. The delay of the sample clock is swept through the arrival time of an optical pulse to capture the time evolution of the voltage on the detector. The sampled voltage is recorded on the oscilloscope following an inverting buffer stage, as shown. The detector studied here is the N + p-well junction, which has a depletion width of $\sim$100 nm at a depth of $\sim$100 nm from the chip surface. The response of this detector to both 850- and 425-nm light was measured. The capacitance of this 10 $\times$ 10-μm detector was 100 fF.

The results for both wavelengths are shown in Fig. 8. The plot shows a sharp rise ($\sim$100 ps) followed by a slower tail. In the 850-nm case, the sharp rise comprises a small fraction of the total swing, whereas in the 425-nm case, the sharp rise achieves most of the swing. The sharp rise corresponds to the carriers generated near the depletion region, which are collected due to drift. The slow tail corresponds to carriers generated outside the depletion area, which slowly diffuse into it, contributing eventually to the voltage rise. Since the absorption length at 850 nm is $\sim$ 14 μm, a very small number of carriers are generated near the depletion region. In contrast, at 425, where the absorption depth is $\sim$180 nm, the majority of carriers are generated at or near the depletion within the first 100 ps. Note that the 100-ps rise time in the fast regime indicates that these bulk detectors are *RC* limited, since the transit time for the 100-nm depletion width would be much shorter. Given the relatively large (100 fF) capacitance of the bulk detectors, *RC*-limited behavior can be expected.

These results confirm our intuition about the behavior of bulk CMOS detectors in the blue and at 850 nm. In addition, we note that, even in the blue, there is still a diffusion tail and thus a slow component to the charge collection. Because the sampling space is limited to 12 ns, this experiment does not allow quantitative determination of what fraction of the total charge is collected

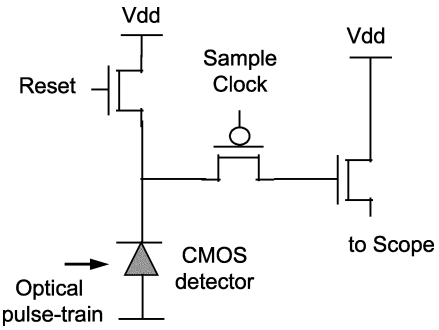

Fig. 7. Simplified schematic of sampler circuitry for measuring the temporal response of bulk CMOS detectors at 850 and 425 nm.

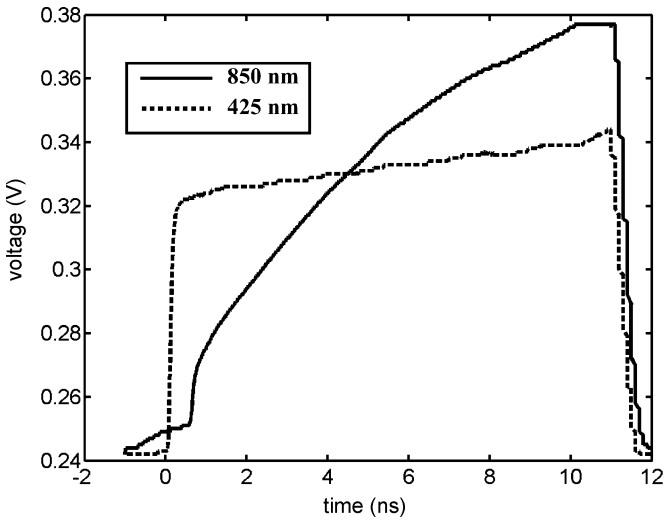

Fig. 8. Electrically sampled measurement of the temporal response of a bulk CMOS detector at 850 and 425 nm.

in the fast regime. MEDICI simulations of this bulk CMOS detector correspond to the experimental data in the first 12 ns and are used to estimate the evolution at longer times. These simulations confirm that $\sim$88% of the carriers are collected in the fast regime at 425 nm, compared with $\sim$6% at 850 nm. This type of response could be viable if used with clamping circuitry or in an integrating application.

V. Conclusion

This paper experimentally explored the feasibility of using blue light for enhancing the performance of bulk and SOI CMOS detectors for high-speed applications. It was found that in bulk CMOS, the slow carrier collection tail is greatly reduced by using blue light, making these detectors viable for use in some high-speed applications. However, the relatively large capacitance of bulk CMOS detectors could limit their speed regardless of wavelength. A pump–probe technique was used to verify transit-time-limited response from SOI detectors. A responsivity of 0.066 A/W and $\sim$100-ps rise times were measured in the blue. Thus, even with 6-μm finger spacing, the SOI detectors have a $\sim$3.5-GHz bandwidth and are therefore suitable for $\sim$5-Gb/s data speeds with blue light input. Hand calculations and MEDICI simulations show that 1.2-μm detectors, which are available in this technology, would be suitable

for >10 Gb/s applications. Although high-speed low-power blue light signals may not yet be conveniently generated or modulated for interconnect applications, the idea of generating blue light for optical clock injection is relatively more viable even with present optical short-pulse technology, and this paper demonstrates that blue-light clock injection directly into silicon circuits may well be quite feasible in the near future.

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REFERENCES

[1] T. K. Woodward and A. V. Krishnamoorthy, "1 Gbit/s CMOS photoreceiver with integrated detector operating at 850 nm," *Electron. Lett.*, vol. 34, no. 12, pp. 1252–1253, June 1998.

[2] M. K. Emsley, O. Dosunmu, and M. S. Unlu, "High-speed resonant-cavity-enhanced silicon photodetectors on reflecting silicon-on-insulator substrates," *IEEE Photon. Technol. Lett.*, vol. 14, pp. 519–521, Apr. 2002.

[3] M. Y. Liu, E. Chen, and S. Y. Chou, "140 GHz metal–semiconductor–metal photodetectors on silicon-on-insulator substrate with a scaled active layer," *Appl. Phys. Lett.*, vol. 65, no. 7, pp. 887–888, 1994.

[4] B. F. Levine, J. D. Whynn, F. P. Klemens, and G. Sarusi, "1 Gb/s Si high quantum efficiency monolithically integrable $\lambda = 0.88\ \mu$m detector," *Appl. Phys. Lett.*, vol. 66, no. 22, pp. 2984–2986, 1995.

[5] S. M. Csutak, S. Dakshina-Murthy, and J. C. Campbell, "CMOS-compatible planar silicon waveguide-grating-coupler photodetectors fabricated on Silicon-on-Insulator (SOI) substrates," *IEEE J. Quantum Electron.*, vol. 38, pp. 477–480, May 2002.

[6] B. Yang, J. D. Schaub, S. M. Csutak, D. L. Rogers, and J. C. Campbell, "10-Gb/s all-silicon optical receiver," *IEEE Photon. Tech. Lett.*, vol. 15, pp. 745–747, May 2003.

[7] M. Yang *et al.*, "A high-speed, high-sensitivity silicon lateral trench photodetector," *IEEE Electron Device Lett.*, vol. 23, pp. 395–397, July 2002.

[8] Q. Ouyang and J. D. Schaub, "High speed lateral trench detectors with a junction substrate," in *Proc. Device Research Conf.*, June 23–25, 2003, pp. 73–74.

[9] Frequency Doubled NCSEL Lasers. [Online]. Available: http://www.novalux.com/products/

[10] A. Rochas, A. R. Pauchard, P. A. Besse, D. Pantic, Z. Prijic, and R. S. Popovic, "Low-noise silicon avalanche photodiodes fabricated in conventional CMOS technologies," *IEEE Trans. Electron Devices*, vol. 49, pp. 387–395, Mar. 2002.

[11] P. Catrysse, B. Wandell, and A. El Gamal, "An integrated color pixel in 0.18 μm CMOS technology," in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, Dec. 2–4, 2001, pp. 24.4.1–24.4.4.

[12] X. Zheng, C. Wrigley, G. Yang, and B. Pain, "High responsivity CMOS imager pixel implemented in SOI technology," in *IEEE Int. SOI Conf.*, Oct. 2–5, 2000, pp. 138–139.

[13] S. Adachi, *Optical Constants of Crystalline and Amorphous Semiconductors*. Norwell, MA: Kluwer, Aug. 1999.

[14] D. A. B. Miller, D. S. Chemla, T. C. Damen, A. C. Gossard, W. Wiegmann, T. H. Wood, and C. A. Burrus, "Electric field dependence of optical absorption near the bandgap of quantum well structures," *Phys. Rev. B, Condens. Matter*, vol. 32, pp. 1043–1060, 1985.

[15] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1969, ch. 2, p. 59.

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