Thin Dielectric Spacer for the Monolithic Integration of Bulk Germanium or Germanium Quantum Wells With Silicon-on-Insulator Waveguides

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Abstract: We propose an approach to monolithically integrate bulk germanium (Ge) or Ge quantum wells with silicon-on-insulator (SOI) waveguides through selective epitaxy and direct butt coupling. To prevent lateral epitaxial growth during the selective epitaxy, a dielectric insulating spacer layer is deposited on the sidewall facet of the SOI waveguide. With an SiO_2 spacer that is 20 nm thick, the additional insertion loss penalty can be as low as 0.13 dB. We also propose and demonstrate a robust, reliable, and complementary metal–oxide–semiconductor (CMOS)-compatible fabrication process to realize sub-30-nm spacers.

Index Terms: Integrated optoelectronics, germanium, quantum wells, electrooptic modulators.

1. Introduction

Optical interconnections for integrated-circuit inter- and intra-chip communication links have been extensively investigated recently as a possible solution to the electrical interconnect bottleneck in the current electronic technology [1]–[4]. In particular, silicon (Si)-based photonics, which are compatible with the existing complementary metal–oxide–semiconductor (CMOS) technology, are one of the most promising candidates for low-cost, high-density, and large-scale implementation [5]–[8]. Optical interconnect systems involve the generation, modulation, propagation, and detection of photons [7]. With a band gap energy of 1.12 eV, silicon is transparent in the telecommunication C-band (1530–1565 nm) and, hence, is an ideal material for optical propagation. Ridge and rib waveguides built on the silicon-on-insulator (SOI) platform have demonstrated very low loss, sharp bending radius, and small footprint [9], [10].

Germanium (Ge), another Group IV material which is already widely adopted in the advanced CMOS technology, has its lowest energy band gap at 0.66 eV and, hence, can be efficient at photon

detection in the telecommunication bands. Various surface normal [11], [12], as well as waveguide-based [13]–[15], Ge photodetectors on Si substrates have already been demonstrated by several groups, showing high responsivity, low dark current, and high speed operation. Moreover, the Franz–Keldysh effect in bulk GeSi alloy has already been used to demonstrate an electroabsorption waveguide modulator [16]. Some of these devices [13]–[16] are monolithically integrated with SOI waveguides, making them very attractive for optical interconnect applications.

Recently the quantum-confined Stark effect (QCSE) [17], a physical mechanism related to the Franz–Keldysh effect but potentially much stronger because of its more abrupt absorption edges and excitonic effects [18], was demonstrated in Ge/SiGe quantum wells grown on Si substrates [19], [20]. It opens a new approach to build CMOS-compatible optical modulators with low voltage drive, large bandwidth, and potentially very-low-energy consumptions. Several standalone QCSE electroabsorption modulators employing this physical mechanism have already been demonstrated [21], [22]. Monolithically integrating these QCSE modulators with the SOI waveguides can further reduce the device footprint, capacitance, and, even more importantly, power consumption. An additional benefit is that the same epitaxy and device structure can also function as a photodetector [23]. Therefore, by monolithically integrating Ge/SiGe quantum well structures with SOI waveguides, we can simultaneously realize optical modulation, propagation, and detection.

In this paper, we present a novel approach to integrate bulk Ge or Ge/SiGe quantum well active sections with SOI waveguides through butt-coupling. In particular, we propose and demonstrate a thin dielectric spacer for this monolithic integration. The rest of the paper is organized as follows. First, we give an overview of the integration scheme and motivate the necessity for the thin spacer layer. Then, numerical analysis will be carried out to evaluate the impact of this spacer layer on the device performance. After that, a dual-layer fabrication process is proposed and demonstrated to build this thin spacer layer with precise thickness control. Finally, we will discuss the further applications for this spacer and draw conclusions.

2. Motivation

The incorporation of Ge into SOI waveguides is typically realized through selective epitaxial growth from the underlying crystalline Si. The coupling between the Ge active section and the passive waveguide can be realized by two different approaches. In the first approach, a Ge layer is grown directly from the top crystalline Si layer of the SOI substrate [13], [16]. In this scheme, coupling is realized evanescently using adiabatic tapers. These adiabatic tapers are at least tens of micrometers long. So devices in this category have a large footprint. Furthermore, if the taper is realized in the Ge active section, the devices unavoidably have a large capacitance. In the second approach, a recess is defined in the top Si layer, and Ge is selectively grown from the remaining crystalline Si inside the recess [14], [15]. In this scheme, the Ge active section and the SOI waveguide are at the same vertical level. The coupling between the two is realized through direct butt coupling. The devices in this category can be very compact and wavelength insensitive since adiabatic tapering is not needed. The sacrifices here are the additional insertion loss and back reflection due to the refractive index mismatch. For short distance interchip and intrachip interconnect applications, where a small device footprint is necessary and some insertion loss can be afforded, this second approach and direct-butt coupling is arguably preferable to the evanescent coupling approach. In this paper, we choose to integrate the active section with the SOI waveguide through direct-butt coupling.

The selective epitaxial growth for the second approach is illustrated in Fig. 1(a). As indicated by the black arrows in the figure, the epitaxial growth will occur from the exposed crystalline Si, both vertically from the bottom of the recess and laterally from the exposed Si facets. More seriously, if the two exposed vertical facets are (100) growth planes, the lateral and vertical growth rates may be the same. This lateral growth is unwanted, and imposes two major limitations. First of all, depending on the relative rates of the vertical and lateral growth, the grown epitaxy may be of an irregular shape and difficult to predict. At the location where the vertical growth joins the lateral growth, misfit dislocations and voids can form, resulting in poor epitaxy quality and device performance [24]. The

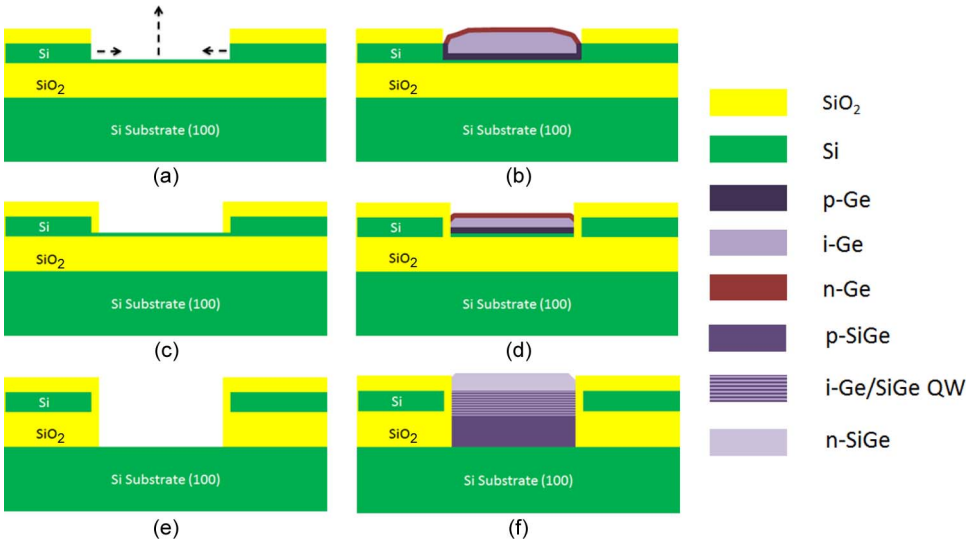

Fig. 1. Schematics of the different growth templates (on the left) and the corresponding p-i-n epitaxy (on the right). (a) The commonly used template with a silicon recess and without the spacer. Black dashed arrows indicate the directions of the selective growth. (b) The shape of the grown film is unpredictable due to the simultaneous lateral and vertical growth. With *in situ* doping, the intrinsic region will be electrical shorted. (c) The growth template with the silicon recess and dielectric spacers on the vertical facets. (d) The corresponding grown epitaxy. Note that some faceted growth may occur at the boundary of the growth window depending on the growth conditions, but this faceting region is narrow and relatively predictable. (e) The growth template with BOX removed and with the spacer. (f) The epitaxy of a p-i-n SiGe diode with Ge quantum wells in the intrinsic region.

lateral growth also makes it impossible to grow planar heterostructures, such as quantum wells. Furthermore, even for bulk Ge growth, a chemical-mechanical polishing (CMP) step is needed after the selective epitaxy to planarize the structure. Second, for many applications, such as photodetectors and modulators, a vertical p-i-n structure is needed. If *in situ* doping is used, the lateral growth of the doped layer will electrically short the intrinsic region. Fig. 1(b) illustrates the case if *in situ* doping were added during the selective epitaxy. The common work-around is to dope the starting thin Si through ion implantation and rapid thermal annealing (RTA) instead [13]–[15]. However, ion-implantation can generate crystalline defects in the growth template, which will degrade the quality of the subsequent growth. High-temperature RTA imposes additional thermal budget constraints on the fabrication of the CMOS circuitry if it is to be integrated together with the optical interconnects. Furthermore, recent work [25] shows that a higher activated doping level and a sharper transition boundary between the doped and intrinsic regions can be achieved in *in situ* doped Ge, which will be of great importance for high speed devices. Recently, we have already demonstrated that high quality Ge/SiGe quantum well structures can be selectively grown on patterned Si substrates with SiO_2 as the growth mask [26].

To avoid the unwanted lateral growth, we propose inserting a dielectric insulating spacer layer at the sidewall of the growth window. The most commonly used insulating dielectric in CMOS technology is SiO_2. Fig. 1(c) illustrates the growth template with the spacers on both sides of the exposed crystalline Si waveguide. With the spacer in place, the lateral growth will not initiate. This makes it possible to achieve *in situ* doping for bulk Ge active sections, as in Fig. 1(d) and, more importantly, to grow planar Ge quantum well heterostructures in the active section.

One subtle difference between growing bulk Ge and Ge/SiGe quantum wells is that the active Ge/SiGe quantum wells need to be grown on a relaxed buffer at least several hundred nanometers thick so that there is no net built-in strain. On the other hand, the top Si layer for most SOI waveguides is only around 300 nm thick. To accommodate this relaxed buffer, the buried oxide (BOX) layer in the growth window can be removed before the selective growth, as shown in Fig. 1(e). The growth will start from the top surface of the handle substrate of the SOI wafer. There is an additional benefit using this

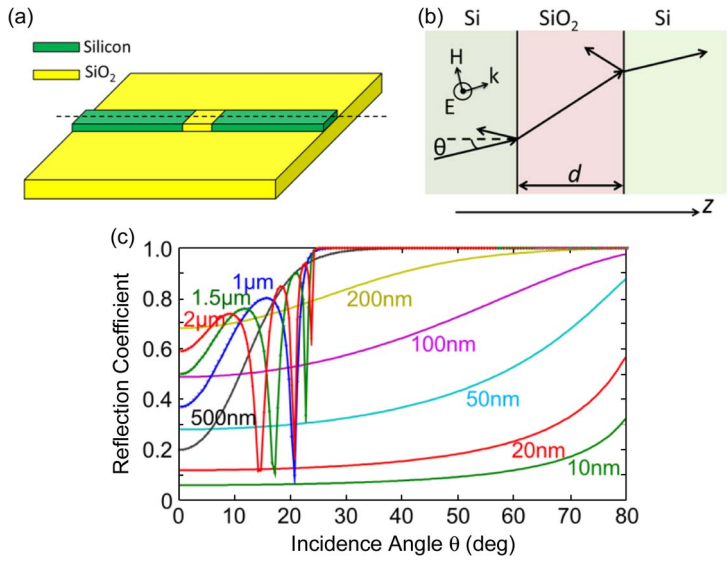

Fig. 2. (a) Schematic of the problem setup. Propagation through two SOI waveguide sections with a SiO_2 spacer in between. (b) Simplified 1-D model for a plane wave component with incidence angle θ. (c) Electric field reflection coefficient evaluated for various angles with different spacer thicknesses.

approach. While the majority of the BOX can be removed by reactive ion etching (RIE) to maintain a vertical sidewall, wet hydrofluoric acid (HF) can be used to remove the lower portion of the oxide layer immediately above the handle substrate. This avoids any dry-etching induced damage on the growth surface, preserves the crystal quality of the underlying crystalline silicon, and hence improves the epitaxial quality of the grown film. Some Si or low percentage SiGe alloy can be selectively grown first to fill part of the BOX region and act as the bottom cladding in the active section.

3. Numerical Analysis

There is a large difference in refractive index between Si (3.52) and SiO_2 (1.455) in the near infrared region. The introduction of such a SiO_2 spacer layer into the structure will inevitably cause some insertion loss. In this section, we will study this insertion loss in detail. To evaluate the insertion loss due to the spacer only, i.e., not that from the index difference between the SOI waveguide and the active Ge section, we will evaluate the coupling from the entrance SOI waveguide to the spacer, and then to the exit SOI waveguide, as illustrated in Fig. 2(a). First, we give a 1-D analytical model using the transfer matrix method to gain some physical intuition. Then, a 3-D finite-difference time-domain method (3D-FDTD) will be used to quantify the insertion loss numerically.

In the ray-optics picture, modes in an optical waveguide can be considered as the superposition of plane waves incident at various different angles. These plane wave components experience total internal reflection (TIR) when hitting the boundaries between the core and the cladding of the waveguide. Neglecting the Goos–Hänchen shift associated with the TIR, the propagation of each plane wave component can be treated as that in a uniform medium with a refractive index of the waveguide core. For each plane wave component, as shown in Fig. 2(b), the problem of transmission through the SiO_2 spacer can be treated by the well-known transfer matrix method [27]. In particular, for the simple 3-layer problem, the reflection coefficient can be evaluated analytically as

$$\mathrm{r} = -\frac{e^{-i2k_{z1}d}(k_{z2}-k_{z1})(k_{z1}+k_{z0})+(k_{z2}+k_{z1})(k_{z1}-k_{z0})}{e^{-i2k_{z1}d}(k_{z2}-k_{z1})(k_{z1}-k_{z0})+(k_{z2}+k_{z1})(k_{z1}+k_{z0})} \tag{1}$$

where k_{z0}, k_{z1}, and k_{z2} are the z-components of the complex wave vectors in Si, SiO_2, and Si, respectively, and d is the thickness of the SiO_2 spacer layer. We evaluate the behavior at $\lambda = 1.55\ \mu$m. In the calculations, the refractive indices for Si and SiO_2 are assumed to be 3.52 and

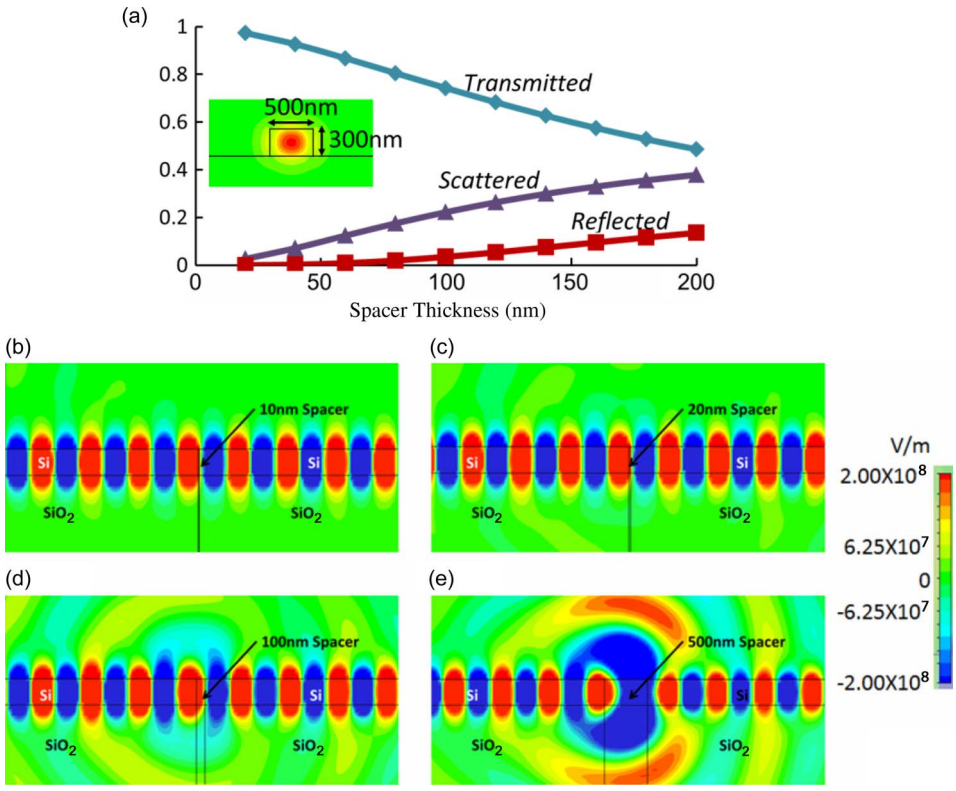

Fig. 3. (a) Percentages of transmitted, scattered, and reflected optical power for different spacer thicknesses. (Inset) Mode profile of the fundamental quasi-TE mode for a 500-nm-wide and 300-nm-thick SOI waveguide. (b)–(e) Electric field distribution for different spacer thicknesses in the cross sectional plane along the dashed line in Fig. 2(a).

1.455, respectively. Using (1), we plot the reflection coefficient for different incidence angles with different spacer layer thicknesses in Fig. 2(c). For thicknesses below 200 nm, the reflection coefficient increases monotonically with increasing incidence angle and increasing spacer layer thickness. We should note that the TIR angle between Si and SiO_2 is $\varphi_c = 24.3^\circ$. If the plane wave component experiences TIR vertically between the Si core and the SiO_2 cladding, the relevant incidence angles at the interface between the Si core and the SiO_2 spacer are $\theta < 90 - \varphi_c = 65.7^\circ$. For spacer layer thicknesses below 20 nm, the field reflection coefficient in this range is less than 0.3, corresponding to less than 10% reflected optical power. For $24.3^\circ < \theta < 65.7^\circ$, frustrated TIR takes place for thicknesses less than $\sim$200 nm, allowing some transmission, while for thicknesses larger than 500 nm the TIR is essentially complete in this angular range. For thick spacers, there are reflection minima due to interference for angles $< 24.3^\circ$, but these occur only for a very narrow incidence angle range. Based on this simple model, we do expect that there is substantial variation in the reflection of the different angular components of the beam: A simple "normal incidence" reflection model is obviously not valid. This model also shows that, for thin spacers (e.g., 20 nm or less), we can expect relatively low reflection resulting from this layer, even over a broad range of angles.

Of course, the above 1-D model in the ray optics picture is somewhat naïve. Specifically, though it can model a beam of a finite size, like the waveguide mode, it does not properly include the effects of the reflections at the (horizontal) core-cladding interfaces. To quantitatively evaluate the insertion loss, the full-wave 3-D FDTD method is used [28]. In the analysis, the fundamental quasi-TE mode of a 500 nm wide and 300 nm high SOI waveguide at 1.55 μm is considered, the mode profile of which is shown in the inset of Fig. 3(a). This mode is launched from the entrance SOI waveguide [left-hand side in Fig. 3(b)–(e)], transmitted through the SiO_2 spacer, and then into the exit SOI waveguide [see the right-hand side in Fig. 3(b)–(e)]. The grid size in the propagation direction is

chosen to be 1 nm, which is fine enough for the thinnest spacer of 10 nm. Transmitted, scattered, and reflected optical powers are normalized to the incident optical power, and calculated numerically, with the results shown in Fig. 3(a). The corresponding electric field distributions in the middle plane cross section of the SOI waveguide for different spacer thicknesses are shown in Fig. 3(b)–(e). We can see that the transmission for a 20-nm spacer is more than 97%, which is equivalent to an insertion loss of 0.13 dB. More than 90% of optical power can be transmitted for spacers thinner than 50 nm (less than 0.46 dB insertion loss). This high transmitted optical power corresponds to almost perfect transmission, as shown in Fig. 3(b) and (c). As the spacer thickness increases, the scattered and reflected optical powers increase, while the transmitted optical power decreases. This can also be seen in Fig. 3(d) and (e), where the transmission is substantially perturbed, and a significant amount of the optical power is reflected and scattered.

4. Fabrication Process

As our numerical analysis in the previous section shows, the thickness of the spacer layer is a critical parameter. First, the thinner the spacer layer is, the lower the insertion loss is. Second, variations in the spacer thickness directly translate to variations of the insertion loss of the devices. So, reliably and uniformly fabricating this very thin spacer is crucial. Since epitaxial growth will be carried out afterward, the very thin spacer has to be formed on and only on the vertical facet sidewall—not on top of the growth window. Furthermore, it is highly desirable that no additional damage is done to the growth window due to the fabrication of the spacer. In this section, we will demonstrate such a process to realize a very thin, sub-30-nm-thick spacer with precise thickness and uniformity control.

Fig. 4(a) shows the detailed process flow. Starting with a SOI substrate [see Fig. 4(a)(1)], we first etch the top Si layer and the majority of the thickness of the BOX using RIE [see Fig. 4(a)(2)]. Then, a wet HF etch is used to remove the small remaining thickness of the BOX, reaching the handle Si substrate [see Fig. 4(a)(3)]. A conformal SiO_2 layer is then deposited by low-pressure chemical vapor deposition (LPCVD) and densified. The thickness of this SiO_2 layer can be accurately controlled by the deposition time and determines the final thickness of the SiO_2 sidewall spacer. Next, a conformal stoichiometric silicon nitride (Si_3N_4) layer is deposited, also by LPCVD. A highly anisotropic RIE, using CHF_3, CF_4, and O_2, is then used to etch the nitride on the top surface of the growth window, stopping on the underlying deposited SiO_2. Due to the etching anisotropy, a Si_3N_4 spacer remains on the sidewall. A HF wet etch then removes the deposited SiO_2 on the growth window. During this step, the Si_3N_4 spacer protects the SiO_2 layer on the sidewall of the growth trench from being removed. Finally, a selective wet etch (hot phosphoric acid) removes the Si_3N_4 spacer.

SiO_2 spacer can, in principle, be fabricated without the sacrificial Si_3N_4 layer by using a highly anisotropic SiO_2 RIE. However, typically the etching rate of RIE varies from the center to the edges of a wafer. Thanks to the sacrificial Si_3N_4, the spacer thickness can be precisely controlled. And more importantly, very good uniformity can be achieved across the entire wafer without fine tuning of the dry etching process. Moreover, we have designed the process so that no direct etching plasma hits the surface of the crystalline Si in the growth window, hence avoiding additional damage due to the fabrication of this spacer. Note that in the process flow of Fig. 4(a), we removed the BOX layer. Using this process, we fabricated a 22-nm SiO_2 spacer on a sloped Si sidewall of approximately 80°, as shown in Fig. 4(b). This also shows that a perfect 90° sidewall facet is not essential to the fabrication of this thin spacer. For applications where an Si recess in the top Si layer is used to nucleate the epitaxial growth, only Steps 4–8 are needed.

5. Discussions and Conclusion

Our motivation for the spacer is the integration of p-i-n bulk Ge or Ge/SiGe quantum wells with a SOI waveguides. However, the use of this spacer is by no means limited to these applications. Monolithic integration in III–V material systems has, for a long time, attracted much research interest. Various approaches, such as selective epitaxial growth/regrowth, offset quantum well growth, and quantum well intermixing, have been successfully demonstrated [29]. This thin spacer

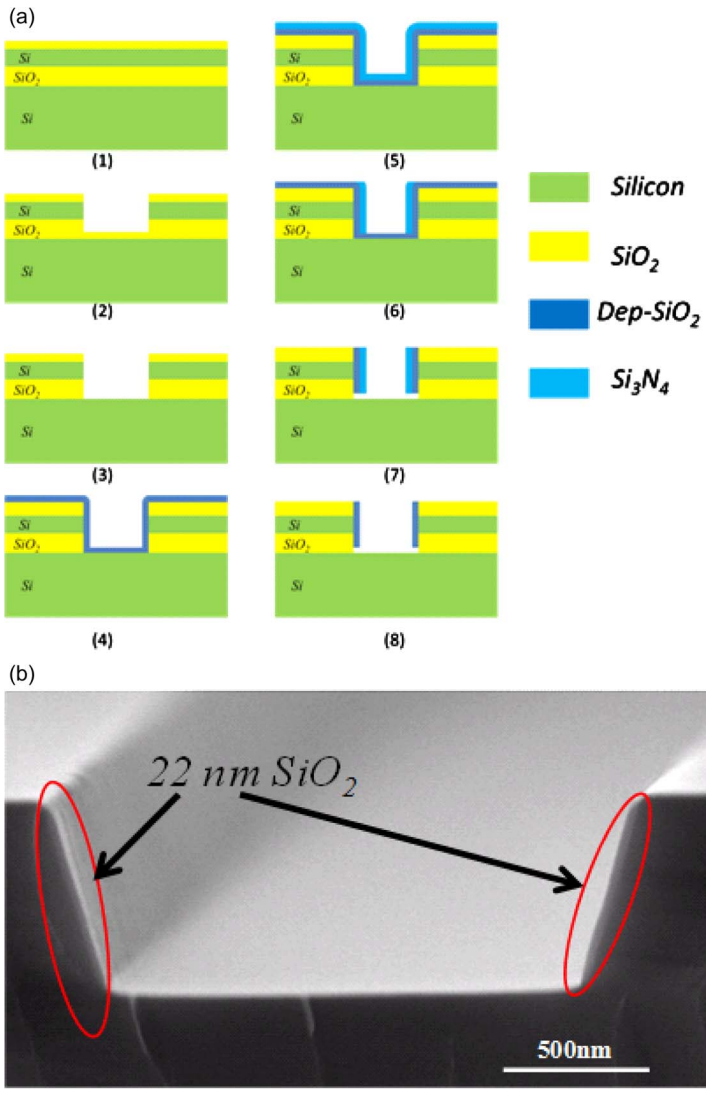

Fig. 4. (a) Process flow for the thin spacer fabrication process. (b) Fabrication results: 22 nm SiO_2 on sidewalls with 80° slope of a growth window trench.

with selective epitaxial growth adds yet another technique to the existing toolkit. For example, this thin spacer layer can replace proton implantation to provide electrical isolation and current confinement for III–V edge emitting lasers coupled to passive waveguides. Although our numerical analysis is done for the coupling between two SOI waveguides with a SiO_2 spacer in between, we expect similar conclusions in other types of waveguide systems. Furthermore, in our fabrication approach, we chose SiO_2 as the spacer material and Si_3N_4 as the sacrificial material, since these two materials are commonly used in CMOS technology. However, this dual-layer spacer fabrication approach is quite general, and should also apply to other dielectric materials. For example, Ge oxynitride or Ge oxide might be preferred as the spacer material to provide better passivation for the subsequently grown Ge epitaxy [30], [31]. Moreover, recent progress on atomic layer deposition techniques for dielectric materials can lead to even more precise control of the spacer thickness.

In conclusion, we discussed various approaches to integrate p-i-n bulk Ge or Ge/SiGe quantum wells with SOI waveguides. We proposed an insulating dielectric spacer to be inserted at the sidewall facet of the SOI waveguide to prevent unwanted lateral growth. Through numerical calculation, we

show that the addition insertion loss can be lower than 0.13 dB for spacers thinner than 20 nm. A robust fabrication process using a sacrificial nitride layer is proposed and demonstrated to realize such thin spacer layers with precise thickness control and excellent uniformity.

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