Surface-Normal Ge/SiGe Asymmetric Fabry–Perot Optical Modulators Fabricated on Silicon Substrates

Ross M. Audet, Elizabeth H. Edwards, Krishna C. Balram, Stephanie A. Claussen, Rebecca K. Schaevitz, Emel Tasyurek, Yiwen Rong, Edward I. Fei, Theodore I. Kamins, James S. Harris, and David A. B. Miller

***Abstract*—We demonstrate the first vertical-incidence Ge/SiGe quantum well reflection modulators fabricated entirely on standard silicon substrates. These modulators could help enable massively parallel, free-space optical interconnects to silicon chips. An asymmetric Fabry–Perot resonant cavity is formed around the quantum well region by alkaline etching the backside of the Si substrate to leave suspended SiGe membranes, upon which high-index-contrast Bragg mirrors are deposited. Electroabsorption and electrorefraction both contribute to the reflectance modulation. The devices exhibit greater than 10 dB extinction ratio with low insertion loss of 1.3 dB. High-speed modulation with a 3 dB bandwidth of 4 GHz is demonstrated. The moderate-Q cavity ($Q \sim 600$) yields an operating bandwidth of more than 1 nm and permits operation without active thermal stabilization.**

***Index Terms*—Integrated optoelectronics, optical interconnections, optical modulation.**

I. Introduction

FUTURE chip-to-chip interconnects, such as those between multiple processors or between processors and memory, will require extremely high-communication bandwidth densities and low energy consumption [1]. Optical interconnects show promise for meeting these bandwidth and energy targets, provided the optical devices and silicon circuitry are tightly integrated [2]. As such, there has been great interest in making silicon-compatible optical components that can be integrated with complementary metal–oxide—semiconductor (CMOS) circuitry. In particular, much progress has been made to date on creating effective Si-compatible modulators based on both electrooptic and electroabsorption effects [3], [4].

While simple waveguided optical links may prove sufficient in the short term, to achieve ultimate scaling of interconnect bandwidth, dense wavelength division multiplexing will likely eventually be required for waveguided devices because of the limited chip perimeter available for waveguide coupling [2]. An alternative approach that can achieve the extreme bandwidths that will be required by future computing systems is to use optical modulators employed in a surface-normal geometry, in which both the incident and modulated reflected beams are oriented perpendicular or near-perpendicular to the chip surface. These modulators can be employed in links based on hybrid integration with waveguides [5], or in systems based on free-space optics.

Because surface-normal modulators can be integrated into dense 2-D arrays, they can enable spatially multiplexed free-space optical links with thousands of channels. They can thus provide the continued scaling of interchip interconnect bandwidths that will be necessary to meet projected bandwidth demands for future computing systems, using only a modest fraction of a chips surface area [2]. Furthermore, they can avoid the complexity of wavelength division multiplexing schemes, which would be necessary for waveguide approaches.

In one possible implementation of a free-space chip-to-chip interconnect using surface-normal devices, light is generated off-chip by an efficient III–V semiconductor laser. A regularly spaced grid of spots is generated from the collimated laser beam by means of a diffractive element, and is imaged onto an array of modulators using one or more intermediate layers of optics. The modulated reflected light is then directed to photodetectors on a neighboring chip.

There has been the substantial consideration of optical system design and corresponding alignment tolerances for these free-space interconnects [6]–[9], and several demonstrations to date of highly parallelized free-space optical links consisting of hundreds or thousands of beams [10]–[13], some using vertical cavity surface-emitting laser (VCSEL) arrays, and others using optical modulators. Large, parallel, optically connected

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R. M. Audet, K. C. Balram, E. Tasyurek, and D. A. B. Miller are with the Edward L. Ginzton Laboratory, Stanford University, Stanford, CA 94305 USA (e-mail: ross.audet@post.harvard.edu; kcbalram@stanford.edu; tasyurek@stanford.edu; dabm@ee.stanford.edu).

E. I. Fei, T. I. Kamins, and J. S. Harris are with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305 USA (e-mail: edfei@stanford.edu; kamins@stanford.edu; harris@snow.stanford.edu).

E. H. Edwards was with the Edward L. Ginzton Laboratory, Stanford, CA 94305-4090 USA and is now with the Teramat, Inc., Palo Alto, CA 94301 USA (e-mail: ehe@alumni.stanford.edu).

S. A. Claussen was with the Edward L. Ginzton Laboratory, CA 94305-4090 USA and is now with the Colorado School Of Mines, Golden, CO 80401 USA (e-mail: sclausse@mines.edu).

R. K. Schaevitz was with the Edward L. Ginzton Laboratory, CA 94305-4090 USA and is now with Corning West Technology Center, Palo Alto, CA 94304 USA (e-mail: rebecca.schaevitz@gmail.com).

Y. Rong was with the Stanford Department of Electrical Engineering, Stanford, CA 94305-9505 USA and is now with the Philips LumiLEDs, San Jose, CA 95131 USA (e-mail: rywryw@gmail.com).

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logic systems based on III–V devices have been successfully demonstrated with over 60 000 light beams [14].

Despite the potential advantages of free-space interconnects based on surface-normal modulators, there has not yet been a demonstration of an efficient, vertical-incidence modulator that can be monolithically integrated with CMOS circuitry, as would be desired for high-bandwidth links to silicon chips.

The surface-normal device configuration presents several challenges. Most significantly, the optical interaction length between the incident beam and the semiconductor material is limited, and as such, a strong electrooptic or electroabsorptive effect must be employed in conjunction with a resonant cavity to achieve sufficient contrast. This has successfully been demonstrated in III–V semiconductor devices, where modulation has been achieved using the quantum-confined Stark effect (QCSE) in asymmetric Fabry–Perot (AFP) resonant cavities formed by epitaxial distributed Bragg reflectors (DBRs) [15]–[17].

Following the demonstration of strong quantum-confined Stark effect (QCSE) in Ge/SiGe quantum wells (QWs) [18]–[21], our group has recently made significant progress toward a silicon-compatible surface-normal modulator by demonstrating a device based on QCSE in Ge/SiGe QWs situated inside a moderate-Q AFP resonant cavity [22]. The Ge/SiGe QW structures in Ref. [22] are grown by chemical vapor deposition (CVD) on silicon substrates. However, because of the lack of an effective epitaxial DBR in the SiGe material system, a layer-transfer process involving anodic bonding to a Pyrex handle wafer was employed in order to form the resonant cavity, meaning that the fabricated modulators were not monolithically integrable with CMOS circuitry. Furthermore, the demonstrated extinction ratio was low, possibly due to surface roughness at the SiGe/Pyrex bonding interface.

In this study, we present the first Ge/SiGe QW asymmetric Fabry–Perot modulators (AFPMs) fabricated entirely on standard silicon substrates. These devices utilize a backside etch process that enables fabrication of the resonant cavity following the epitaxial growth. As such, the modulators could be suitable for integration with silicon circuitry. We attain high extinction ratios ($>$ 10 dB) with low insertion loss (1.3 dB) and drive voltage swings of 3 V or less, with nearly 7 dB extinction ratio for a 1 V drive swing.

II. Concept

The operational principle behind these AFPMs has been outlined previously [22]. We summarize the most important aspects of the theory here. The Ge/SiGe QW active region, in which the absorption can be modulated by application of an electric field via the QCSE [23], is located inside an AFP resonant cavity, consisting of a high reflectance back mirror (ideally 100% reflective), and a front mirror with slightly lower reflectance, with the precise value chosen to match the absorption properties of the QW active region. It is possible to reach a "critical coupling" condition (analogous to that for waveguide-coupled microring modulators [24]) with zero reflectance when the front mirror reflectance matches the effective (reflectance minus absorption in the cavity) back mirror reflectance. Thus, the AFP cavity allows a small change in the material absorption to be translated into a large change in the overall reflectance, with nearly zero reflectance in the off state, such that high extinction ratios are achieved despite the limited interaction length afforded by the vertical-incidence geometry.

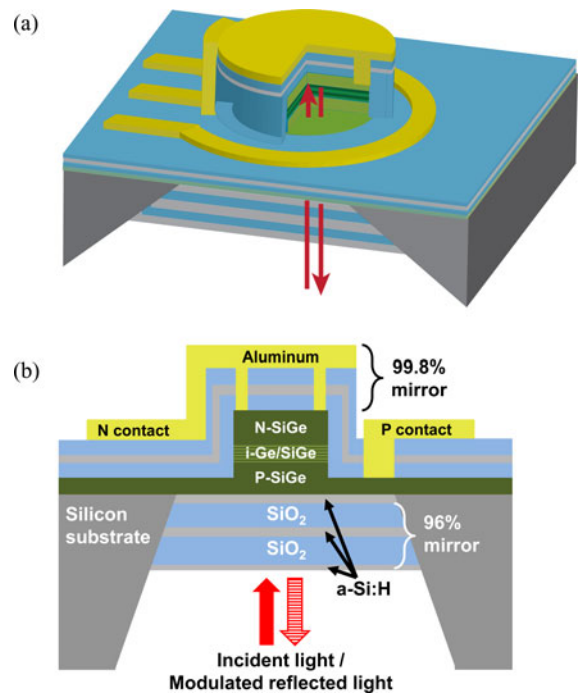


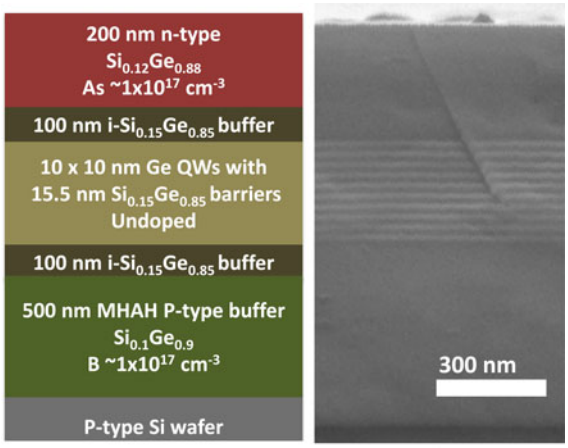
Fig. 1. Schematic illustration of the Ge/SiGe quantum well asymmetric Fabry–Perot reflection modulator. (a) Perspective view and (b) side view.

The challenge in creating such an AFP cavity in the Ge/SiGe material system is the inability to fabricate an epitaxial DBR mirror with sufficient index contrast beneath the QW active region. Because of this, it is necessary to form the front and back mirrors in a separate process following the epitaxial growth of the SiGe active region. In this study, we utilize a masked alkaline wet etch to remove the silicon substrate directly underneath the modulators. The etch terminates upon reaching the SiGe layer, leaving a thin suspended SiGe membrane. Thus, we have access to both the front and back side of the SiGe active region, enabling deposition of the appropriate distributed Bragg reflector mirrors to form the asymmetric Fabry–Perot resonant cavity. The overall device concept is depicted in Fig. 1(a) and (b).

A related substrate removal technique utilizing silicon-on-insulator (SOI) substrates has been previously demonstrated for a Si microcavity [25]. In the Ge material system, substrate and sacrificial layer removal techniques have been used to create tensile-strained Ge films in order to decrease the direct bandgap energy relative to the indirect gap [26], [27], and a strained Ge membrane structure has been proposed as a means of making an electrically injected Ge-VCSEL [28].

III. Epitaxy

The Ge/SiGe QW epitaxial structure used in the modulator is grown on a p-type Si wafer using an Applied Materials Centura Epi reduced pressure chemical vapor deposition (RPCVD)



(a) (b)

Fig. 2. (a) Epitaxial layer structure design showing the SiGe p-i-n diode structure with a multiple-hydrogen-annealing-for-heteroepitaxy (MHAH) relaxed SiGe buffer on a Si substrate and (b) scanning electron microscope image of the epitaxial structure.

system, operated at a chamber pressure of 40 torr and a growth temperature of 400 °C. The layer structure is shown in Fig. 2. The QW active region is inside the intrinsic region of a p-i-n diode. A fully relaxed multiple-hydrogen-annealing for heteroepitaxy (MHAH) $\mathrm{Si}_{0.1}\mathrm{Ge}_{0.9}$ p-type (boron, $1 \times 10^{17}\ \mathrm{cm}^{-3}$) buffer layer limits the propagation of crystal defects arising from the 4% lattice mismatch between Si and Ge [29]. The active region above this consists of a 100 nm intrinsic spacer region to limit dopant diffusion into the quantum wells, followed by ten 10 nm-thick Ge QWs with 15.5 nm $\mathrm{Si}_{0.15}\mathrm{Ge}_{0.85}$ barriers, and another 100 nm intrinsic spacer. At the top of the structure is a moderately arsenic-doped ($1 \times 10^{17}\ \mathrm{cm}^{-3}$) n-type $\mathrm{Si}_{0.1}\mathrm{Ge}_{0.9}$ layer.

The absorption properties of the epitaxy are measured by fabricating p-i-n photodiodes on samples without a resonant cavity. The devices are illuminated using a fiber probe with light from a tunable laser. A reverse bias is applied to a device, and photocurrent is measured using a lock-in amplifier, with values calibrated by comparison at several wavelengths to readings from a semiconductor parameter analyzer. Because the Ge QWs sit within the intrinsic region of the p-i-n diode, nearly all the generated photocarriers will be collected as photocurrent when a bias is applied, and hence the photocurrent provides a measure of the optical absorption inside the QW active region. Strong QCSE is evident in the absorption spectra, shown in Fig. 3. The fraction of light absorbed per pass in the material is normalized to the thickness of the QW active region (including both wells and barriers) in order to express the absorption in inverse centimeters.

Because the applied field strongly alters the the QW transition energies and absorption strengths, there is a corresponding change in refractive index as governed by the Kramers–Kronig relations [30], [31]. Although measurements of the absorption must be taken over a wide range of photon energies in order to determine the full refractive index profile, the relative change Δn of the refractive index can be calculated from photocurrent measurements over the smaller range of wavelengths in which

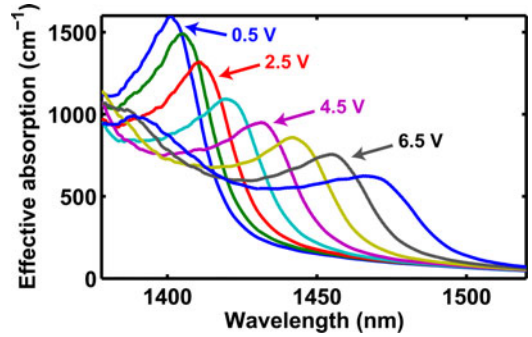


Fig. 3. Absorption spectra of the Ge/SiGe quantum well epitaxy for reverse bias voltages ranging from 0.5 to 7.5 V, in 1 V increments.

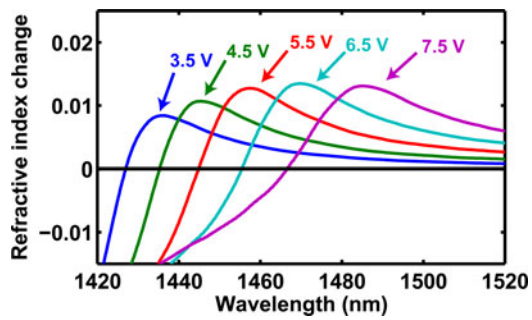


Fig. 4. Calculated refractive index change for several reverse bias voltages, relative to the refractive index profile at 0.5 V reverse bias.

the applied field substantially alters the absorption. Using the experimentally measured differential absorption between high bias states and a low bias (0.5 V) state, we compute Δn versus wavelength for several applied bias voltages. The results are shown in Fig. 4. Due to the strong band edge electroabsorption, the effective refractive index change in the quantum well active region is extremely large (0.013 at 6.5 V bias, 1470 nm). For a 3 V swing (3.5 to 6.5 V, electric field of 75 to 140 kV/cm), we expect $\Delta n = 0.011$ in the QW active region. This value is about 8.5 times larger than the refractive index shift reported in Ref. [31]; however, the present device is deliberately operated closer to the exciton peak in the region where absorption is not negligible. In similar conditions as those in Ref. [31] (90 kV/cm applied field, photon energy 50 meV below the zero-field exciton peak, the calculated refractive index change is 0.004, approximately three times larger than the value reported in Ref. [31].

IV. Device Design

To limit the effects of background absorption arising from indirect gap absorption in the Ge and SiGe layers [32], we choose to operate at a wavelength of around 1470 nm, by applying several volts to redshift the absorption edge into this wavelength range.

From the photocurrent measurements (shown in Fig. 3), at the design wavelength of 1470 nm, at a bias of 6.5 V, the absorption is 380 cm^{-1} (1.02% absorption per pass) and at a bias of 4.5 V, the absorption is 120 cm^{-1} (0.38% absorption per pass).

Now, we consider the resonant cavity design. For an AFP cavity, at normal incidence, the fraction of reflected optical power

TABLE I
CAVITY DESIGN FOR OPERATION AT 1470 NM

High absorption state (6.5 V)	380 cm^{-1}
Low absorption state (4.5 V)	120 cm^{-1}
Absorption contrast	5 dB
Top mirror	$> 99.9\%$
Bottom mirror	96 %
Q (low absorption state)	600

on resonance, R_T, is

$$R_T = \frac{\left|\sqrt{R_f} - \sqrt{R_{b,\mathrm{eff}}}\right|^2}{\left|1 - \sqrt{R_f R_{b,\mathrm{eff}}}\right|^2} \quad (1)$$

where R_f is the front mirror reflectance, and the effective back mirror reflectance $R_{b,\mathrm{eff}}$ is given by $R_{b,\mathrm{eff}} = R_b \exp(-2\alpha L)$ [16]. Here, R_b is the reflectance of the back mirror (ideally near unity), α is the effective power absorption coefficient inside the cavity, and L is the cavity length.

Based upon the epitaxy absorption parameters, a front mirror reflectance of approximately 98% would enable the device to approach the zero-reflectance critical coupling condition in the high absorption state and thus help maximize the modulator extinction ratio [16]. The mirror reflectance in the present design was chosen to be slightly lower than this (96%), in order to yield a smaller insertion loss while still achieving a sufficiently high extinction ratio.

The high-reflectance mirror is formed by a three-layer $\lambda/4$ DBR stack consisting of 250 nm $\mathrm{SiO_2}$, 100 nm hydrogenated amorphous silicon (a-Si:H), and 250 nm $\mathrm{SiO_2}$. The high index contrast between the $\mathrm{SiO_2}$ and a-Si:H layers allows fabrication of a mirror with very few layer pairs in a CMOS-compatible materials system. The high-reflectance mirror is further enhanced by an aluminum layer on top of the DBR stack to yield an overall reflectance of 99.8%.

The 96% reflective mirror is located underneath the QW region in the back-illuminated configuration depicted in Fig. 1. It consists of a $\lambda/4$ DBR stack of $\mathrm{SiO_2}$/a-Si:H/$\mathrm{SiO_2}$/aSi:H with thicknesses of 250/100/250/42 nm, respectively. The 42-nm thick layer, which is significantly less than the nominal 100 nm $\lambda/4$ thickness, is chosen in order to achieve a mirror reflectance with the desired value of 96%, which is lower than the 99% reflectance in the case of a 100 nm final a-Si:H. The phase shift as a result of the deviation from the $\lambda/4$ thickness does not alter the wavelength of the cavity resonance appreciably.

Given the resonant cavity design (summarized in Table I) and the known properties of the Ge/SiGe epitaxy, we simulate the expected device performance based on plane wave illumination using a transfer matrix technique [33]. The zero-bias refractive index parameters are taken from spectroscopic ellipsometry of the individual films. The absorption spectra (shown in Fig. 3) and the calculated refractive index change (see Fig. 4), are incorporated into the simulation in order to determine the voltage-dependent response. The resulting simulated reflection spectra are shown in Fig. 5.

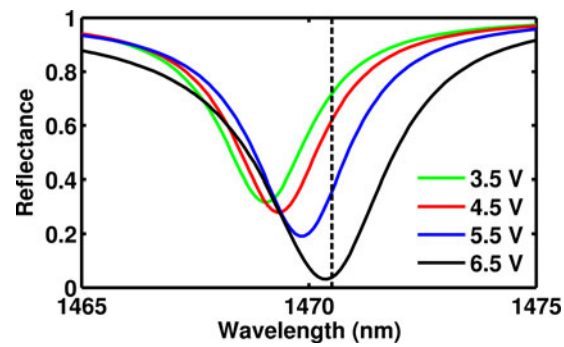


Fig. 5. Simulated modulator performance based on the resonant cavity design given in Table I. The wavelength corresponding to the highest extinction ratio is indicated with a dotted line. The voltage-dependent absorption and refractive index of the QW active region are taken from measurements of the bare epitaxy (Figs. 3 and 4).

The simulation shows a decrease in the minimum reflectance as the bias voltage is increased, and near zero reflectance as the asymmetric Fabry–Perot critical coupling condition is approached at 6.5 V bias. Additionally, the substantial refractive shift plays a large role in improving the extinction ratio and insertion loss by increasing the on-state reflectance at the operating wavelength. It should be noted that the refractive shift has typically been ignored in III–V semiconductor AFPMs due to the use of lower reflectance top mirrors. In one of the few previous reports considering the refractive shift, voltage swings up to 30 V were required to see a significant effect [34].

V. DEVICE FABRICATION

The fabrication of the devices begins by reactive ion etching the SiGe epitaxial layers using an $\mathrm{SF_6}$ chemistry, forming circular mesas with diameters ranging from 10 to 60 $\mu\mathrm{m}$. A portion of the p-region of the epitaxy, approximately 250 nm thick, is left unetched, as shown in Fig. 1(b). The chip is cleaned using a heated bath of photoresist stripper (Baker PRS-1000). The native oxide is removed by two cycles of a 50:1 hydrofluoric acid dip followed by a deionized water rinse. After cleaning, both the epi-side and the backside of the chip are coated with 500 nm of silicon nitride deposited by plasma-enhanced chemical vapor deposition (PECVD). An optical lithography process using backside alignment is employed to define windows on the backside of the chip, directly below individual SiGe mesas or groups of SiGe mesas. The window pattern is transferred to the nitride hard mask on the underside of the chip by reactive ion etching. Next, the chip is submerged for several hours in a 22.5%/wt. potassium hydroxide (KOH) solution, heated to 80 °C, that acts as an anisotropic silicon etchant to remove the silicon substrate underneath the SiGe mesas. The KOH etch terminates upon reaching the bottom p-SiGe epitaxial layer, leaving smooth, approximately 250-nanometer thick SiGe membranes, upon which the SiGe mesas are situated.

Following the KOH etch, the nitride hard mask on the top and bottom sides of the chip is removed by etching in 20:1 buffered oxide etch (BOE).

Next, the $\mathrm{SiO_2}$/a-Si:H DBR portion of the top, high reflectance mirror is deposited by PECVD at 350 °C. This stack

also serves to passivate the exposed SiGe surfaces and provide electrical isolation. A 5 nm a-Si:H layer is deposited on top to prevent etching of the mirror during a subsequent BOE etch step.

To contact the n-region of the mesa, vias are defined using optical lithography, then plasma etched using a CHF_3/O_2 chemistry through the mirror layers until the n-SiGe is reached. A 10 nm-thick PECVD SiO_2 cap layer is then deposited in preparation for an ion implantation step. The chips are implanted with phosphorus ions (18 keV, 4×10^{15} cm^{-2} dose) in order to increase the dopant concentration near the n-SiGe surface for lower n-contact resistance [35]. The dopants are activated by rapid thermal annealing in a nitrogen ambient at 685 °C for 1 min, resulting in an electrically active dopant concentration of $N_d \approx 1 \times 10^{19}$ cm^{-3} at the surface. The SiO_2 cap layer is then removed by a dip in 50:1 HF.

After formation of the n-contact vias, p-contact vias are patterned and etched in the same manner. Because of the larger p contact area and Fermi-level pinning at the valence band of the SiGe [36], ion implantation is not necessary for the p contact.

Once both n- and p-contact vias are formed, the structure is metallized. The metal pattern is defined using optical lithography. A 2-nm Ti layer and 300 nm of Al are deposited by electron beam evaporation, then the pattern is lifted off in acetone. The metal serves as the top layer of the high reflectance mirror on the devices as well as the forming n and p contact wires and pads.

At this stage, light from a tunable laser is focused onto the underside of one of the SiGe mesas, and the reflection and photocurrent spectra are recorded. A layer of aSi:H is deposited on the underside of the chip in order to tune the resonance such that the wavelength matches that of maximum QCSE contrast from the Ge/SiGe quantum well structure. This step is performed using a high-density (HD) PECVD system operating at 90 °C. Finally, the 96% reflective DBR mirror (described in Section IV) is deposited on the underside of the chip by HD-PECVD to complete the asymmetric Fabry–Perot resonant cavity. The structure of the completed device is illustrated in Fig. 1.

Although thin, the membranes are mechanically stable and can be made large enough such that several modulators are fabricated on single membrane. Fig. 6(a) shows an optical microscope image of several completed modulators over a single membrane, viewed from the top. In Fig. 6(b), a scanning electron microscope (SEM) image of a single device is shown. The circle in the center is the SiGe mesa, with the etched via for the n-contact visible. The p-contact via and the metal contact lines surround the mesa. In Fig. 6(c), an SEM of the underside of the chip is shown. The slanted sidewalls are the $< 111 >$ crystal planes of the silicon exposed by the KOH etch. The smooth surface in the center of the image is the bottom of the suspended SiGe membrane containing a single modulator. The faint outlines of the p-contact via and the mesa are visible from the underside.

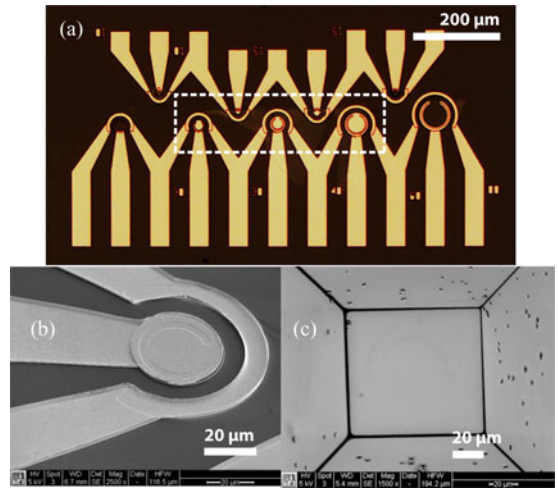


Fig. 6. (a) Microscope image showing a group of devices over a single suspended membrane. The edges of the membrane are indicated with a dotted line. Devices outside the membrane are top-illuminated test structures; (b) SEM image of the top side of a single modulator; (c) SEM image of the underside of a device, showing the anisotropic silicon etch profile and the bottom surface of the suspended SiGe membrane.

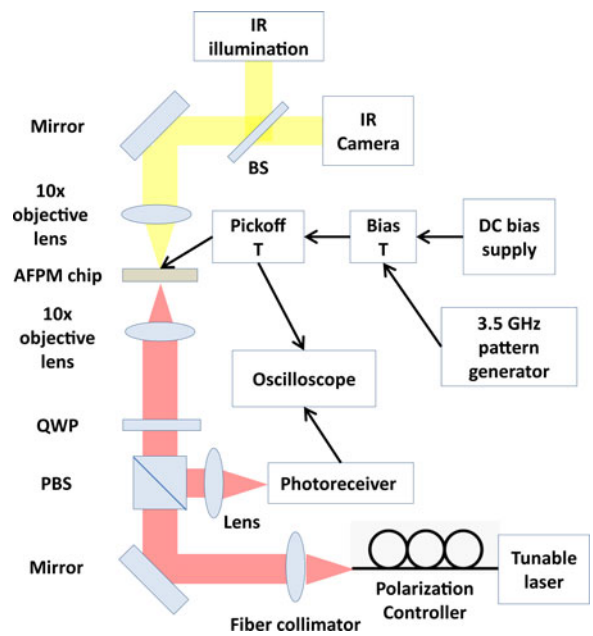


Fig. 7. Measurement setup. The configuration shown is for high-speed measurements. DC reflection measurements are made by replacing the oscilloscope with a lock-in-amplifier.

VI. DC Characterization

Optical measurements were conducted using the setup depicted in Fig. 7. The measurement technique is described in detail in Ref. [22]. Photocurrent spectra, plotted in Fig. 8, show the amount of optical absorption inside the modulator at different bias voltages. The cavity resonance near 1470 nm is clearly visible. At 6.5 V bias, the ratio of absorption 1470 nm (on resonance) to the absorption at 1460 nm (off resonance) is 17.5 times higher than the ratio of absorption at the same two wavelengths for the bare epitaxy (see Fig. 3). The cavity resonance redshifts as the applied voltage is increased, as expected based on the Δn curves plotted in Fig. 4. Furthermore, the photocurrent contrast with applied voltage is consistent with the bulk epitaxy measurements shown in Fig. 3. The absorption contrast between 3.5

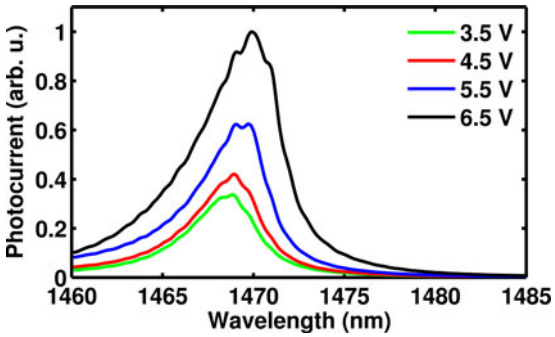


Fig. 8. Photocurrent spectra at several reverse bias voltages, indicating the amount of optical absorption inside the resonant cavity, measured for a 40 μm diameter device.

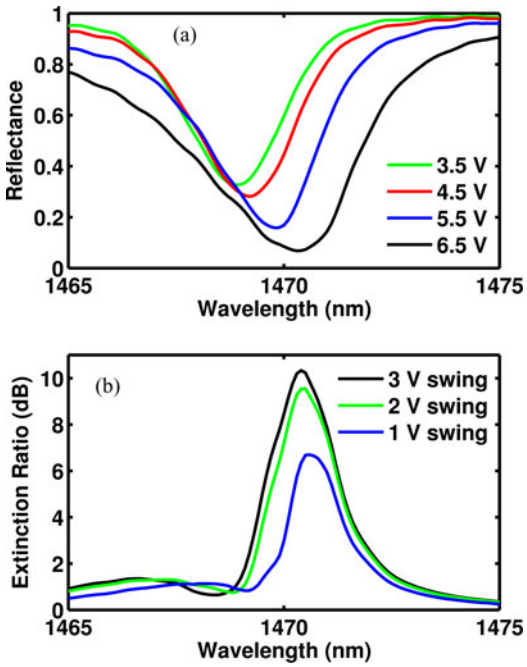


Fig. 9. DC optical performance of a 40 μm diameter modulator; (a) reflection spectra at different reverse bias voltages and (b) plot of the corresponding extinction ratio versus wavelength for 1, 2, and 3 V swings (from 5.5 to 6.5 V, 4.5 to 6.5 V, and 3.5 to 6.5 V, respectively).

and 6.5 V at the corresponding resonant wavelengths is 3, close to the measured absorption contrast of 3.2 for the bare epitaxy between the same bias voltages and wavelengths.

Reflectance spectra from a completed device are shown in Fig. 9(a). As the absorption inside the cavity increases, the device reflectance decreases, as predicted by (1). Additionally, as the bias voltage is increased, a shift in the resonant wavelength is apparent, as was seen in the photocurrent spectra.

The minimum reflectance of 6% is achieved for a bias voltage of 6.5 V at 1470.3 nm. At the same wavelength, the reflectance at a 3.5 V bias is nearly 71%; hence, for a 3 V swing (between 3.5 V and 6.5 V), the extinction ratio is 10.3 dB, and the insertion loss (high reflectance state loss) is only 1.3 dB. An extremely large change in the absolute reflectance of the device is also observed. For a 3 V swing, a maximum ΔR of 74% is attained at 1471 nm, slightly redshifted from the cavity resonance. Excellent performance is also achieved for smaller voltage swings. Maximum extinction ratio, insertion loss, and ΔR values are tabulated for 1, 2, and 3 V swings in Table II. These represent a substantial improvement over the previously reported SiGe/Ge AFPM on a Pyrex substrate, which had an extinction ratio of 3.4 dB for a 3 V swing, and a higher 4.5 dB insertion loss [22].

TABLE II
DC PERFORMANCE SUMMARY FOR SEVERAL DRIVE VOLTAGE SWINGS

	3 V	2 V	1 V
Extinction Ratio (dB)	10.3	9.6	6.7
Insertion Loss (dB)	1.3	1.8	4.1
Max ΔR (%)	74	58	43

The moderate Q resonator employed in this device (low-absorption state Q $\sim$ 600) sufficiently enhances the QCSE absorption while maintaining an operating bandwidth of more than a nanometer, allowing the devices to operate over a range of several degrees Celsius without active thermal stabilization or tuning (and the potentially large associated power consumption).

There is excellent agreement between the experimental results in Fig. 9(a) and the transfer matrix simulations in Fig. 5. Both the change in reflectance and the refractive shift are modeled well. The discrepancy in the minimum absorption at 6.5 V (6.5% versus less than 3% in simulation) is likely due to the finite incident spot size [37].

The good agreement between simulation and experiment indicates that the backside etching process (which results in the QWs being situated on top of thin, suspended SiGe membranes) does not substantially affect QW absorption spectra, which suggests that strain in the QW active region is essentially unchanged.

VII. HIGH-SPEED MEASUREMENTS

High-speed measurements of the devices were made using the setup illustrated in Fig. 7. Large signal modulation was demonstrated using a 3.5-GHz pulse generator producing a nonreturn to zero (NRZ) $2^{23} - 1$ pseudorandom binary sequence (PRBS). Both the pulse generator and a dc power supply (to provide a bias voltage) were connected to the device using a bias-T. An Agilent 30-GHz digital communications analyzer (DCA), connected via a 20 dB pickoff-T, was used to monitor the voltage applied at the modulator. The laser was operated in continuous wave mode, set to a fixed wavelength, with an optical power of approximately 500 μW incident upon the modulator. To measure large-signal eye diagrams, reflected light was focused onto a 1-GHz photoreceiver (New Focus 1611), which was connected to one of the electrical input channels of the DCA. A 15 μm diameter device was tested.

An open eye diagram at 2 Gb/s data rate with 5 V reverse bias and 2 V peak-to-peak swing is shown in Fig. 10. The rise and fall times are limited by the detector rise time (400 ps) rather than the modulator response. A faster, fiber-coupled 30-GHz detector on the Agilent DCA was used to observe the modulator response to a 3 GHz square wave stimulus under similar bias conditions. As shown in Fig. 11, the 10%–90% transition time is approximately 85 ps. Given $t_{10-90} \approx 2.2 t_{\mathrm{RC}}$

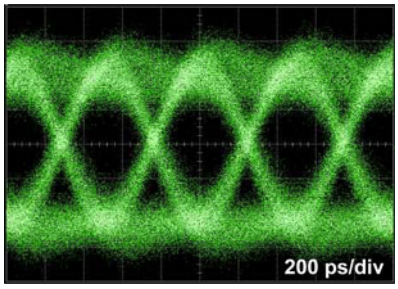


Fig. 10. Open eye diagram at 2 Gb/s, for a 15 μm diameter device, given a DC bias voltage of 5 and 2 V swing at $\lambda = 1471$ nm. Transition times are limited by the photoreceiver rise time (400 ps), rather than the modulator response.

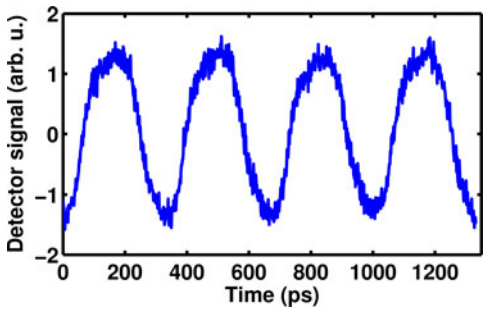


Fig. 11. Reflected optical signal, given a 3 GHz square wave stimulus with amplitude of 2 V, and DC bias voltage of 5 V.

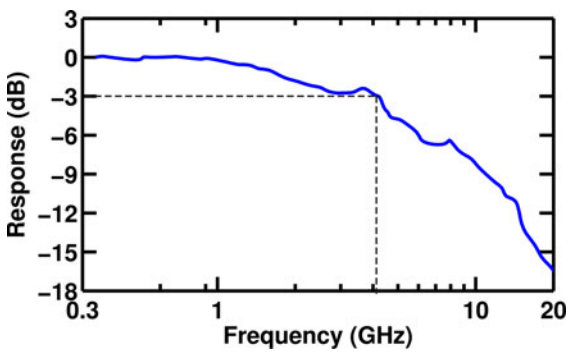


Fig. 12. Small signal measurement showing a 3 dB modulation bandwidth of 4 GHz.

TABLE III
HIGH-SPEED MODULATION PARAMETERS FOR A 15-μm DIAMETER DEVICE

Device capacitance	96 fF
Parasitic capacitance (probe pads)	250 fF
Switching energy per bit (1.5 V swing, excluding parasitics)	54 fJ/bit
3 dB frequency	4 GHz

for a simple RC load step response, this correlates to a 4.1 GHz cutoff frequency. The 3 dB bandwidth of the device was verified by small signal measurement performed using an HP 20 GHz lightwave component analyzer. The response curve is shown in Fig. 12, indicating a 3 dB bandwidth of 4.0 GHz.

Quantities relevant to high speed operation are summarized in Table III. The capacitances are estimated using a parallel plate approximation. The switching energy per bit (ignoring the parasitic pad capacitance, which could be substantially reduced with design changes) of $1/4\ C(V_{\rm on} - V_{\rm off})^2$ [38] is calculated to be approximately 54 fJ/bit for a 1.5 V swing.

The speed of MQW electroabsorption modulators is typically RC limited [39]. Ge/SiGe QW devices in particular should be relatively unaffected by saturation effects at higher optical intensities, due to the fast rate of carrier scattering out of the conduction band Γ valley [40]. A 3 dB bandwidth of 37 GHz has been previously reported in III–V AFPMs, and similar performance is likely attainable with optimization of the current Ge/SiGe devices. Both the capacitance and resistance of the modulators can be reduced substantially. Currently, the device capacitance is dominated by the parasitic capacitance of the n-contact pad over the semiconductor substrate. This capacitance (250 fF) is substantially larger than the actual device capacitance ($<$ 100 fF) for a 15 μm diameter device. Decreasing the pad size and incorporating a thick dielectric isolation layer underneath the pad would substantially decrease the parasitic capacitance.

Additionally, the modulation rate is limited by the large sheet resistances associated with the low doping in the n and p regions ($\sim 1 \times 10^{17}\ {\rm cm}^{-3}$), as the present epitaxy was not optimized for high-speed operation. It is possible to decrease this resistance significantly and improve the modulation rate by increasing the dopant flow during epitaxial growth. SiGe epitaxy with excellent QCSE has been demonstrated by our group with p-doping of $4 \times 10^{19}\ {\rm cm}^{-3}$ and n-doping of $6 \times 10^{18}\ {\rm cm}^{-3}$ [41].

Contact resistances are less substantial than sheet resistances in the present devices, as the ion implantation step is expected to result in n-contact resistivites of $\sim 5 \times 10^{-6}\ \Omega\,{\rm cm}^2$. Techniques that could further decrease the n-contact resistance include formation of nickel germanides [42] and Fermi level depinning via atomic layer deposition (ALD) of TiO_2 [43]. The p-contact resistance is less significant due to larger contact areas and Fermi level pinning near the valence band, as mentioned previously.

VIII. CONCLUSION

We have demonstrated the first surface-normal quantum well reflection modulators fabricated entirely on standard silicon substrates. The devices are created using an anisotropic silicon etch that allows formation of resonant cavities with low scattering losses around SiGe/Ge membranes suspended in air. We demonstrate extinction ratios above 10 dB and low insertion loss by utilizing the refractive shift in conjunction with the electroabsorption effect. Despite an unoptimized epitaxial structure with low p and n region doping, we demonstrate high-speed modulation of 15 μm-diameter devices at several GHz. The low swing voltages and small device size allow for device switching energies in the tens of fJ per bit. The overall link energy of systems based on these QCSE modulators is thus expected to be quite attractive [2], [21], [38]. Given the potential for full CMOS compatibility of these devices, such modulators may prove suitable for highly parallelized free-space optical interconnects between silicon chips.

By optimizing the quantum well structures, modulators could be engineered to provide large absorption contrast at wavelengths near 1550 nm [41] or in the 1300 nm band [21], [44].

Operation at lower bias voltages or lower voltage swings is feasible by using thicker quantum wells or by decreasing the overall intrinsic region thickness. The use of coupled quantum well epitaxial structures [45] can further optimize modulator efficiency. Although the current backside etching process does not substantially alter the strain in the QW region, the addition of a stressor layer, as has been demonstrated for enhanced Ge electroluminescence [28], could potentially be used to tailor the QCSE spectra of the Ge/SiGe QWs in our modulators.

The modulator presented here is designed in a backside illuminated configuration, in which light is incident and reflected from the substrate side. This has several advantages. From a fabrication perspective, it enables the electrical contact metallization to double as an optical reflector, enhancing the 1.5 layer pair DBR to form a mirror with 99.8% reflectance. From a system perspective, the backside illuminated configuration means that the anisotropic etch pits could be used to self-align optical fibers or microsphere lenses to the modulator, which could increase system robustness and mitigate alignment tolerance issues. It should be noted, however, that it would be straightforward to reconfigure the modulator to operate as a front side illuminated device, which may be more suitable for some applications. This could be done by removal of the metal over the top surface of the modulator and increasing the reflectance of the mirror on the backside of the device.

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Author's biographies not available at the time of publication.