

Symmetric Self-Electrooptic Effect Device: Optical Set-Reset Latch, Differential Logic Gate, and Differential Modulator/Detector

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Abstract—We discuss the symmetric self-electrooptic effect device (S-SEED), a structure consisting of two p-i-n diodes electrically connected in series that acts as an optically bistable set-reset latch, and present applications and extensions of this device. The device does not require the critical biasing that is common to most optically bistable devices, and thus is more useful for system applications. We have optically cascaded these devices in a photonic ring counter, and have used them to perform differential NOR, OR, NAND, and AND logic functions. Using the same device, we have also demonstrated a differential modulator that generates a set of complementary output beams with a single voltage control lead, and a differential detector that gives an output voltage dependent on the ratio of the two optical input powers.

I. INTRODUCTION

THE potential use of optics in telecommunications switching and computing has generated much interest lately. One approach is to build two-dimensional arrays of devices that are optically interconnected with lenses and other optical elements using optical beams propagating perpendicular to the arrays. One class of devices uses Fabry-Perot etalons containing semiconductor nonlinear refractive materials [1]–[4]. Uniform operation over different areas of the resonator [3] and fast switching times [4] have been demonstrated. Another device is the quantum well self-electrooptic effect device (SEED) [5]–[8]. SEED's rely on changes in the optical absorption that can be induced by changes in an electric field perpendicular to the thin semiconductor layers in quantum well material. This effect has been called the quantum confined Stark effect (QCSE) [9], [10]. In the simplest SEED, combining the QCSE with optical detection in the same structure causes optoelectronic feedback and bistability to occur. The first SEED's consisted of a resistor connected in series with a p-i-n diode with quantum wells in the intrinsic region [5]. By replacing the resistor with a photodiode, optically bistable devices have been made whose power scales over many decades by adjusting the power

of the light incident on the photodiode [7]. Arrays of photodiode-biased SEED's (D-SEED's) as large as 6×6 have been made [8]. The device doubles as an optically controlled spatial light modulator whose infrared output is determined by the visible light incident on the photodiode [8]. It can also act as a dynamic memory by removing both beams simultaneously, holding its state up to 30 s without optical power.

Another type of device uses a phototransistor as the load [11], [12]. This transistor-biased device (T-SEED) is a true three-terminal device in that a weak signal can control a stronger signal giving effective optical gain. Still another device uses the output of a FET whose gate voltage is controlled by the current in a photodiode to drive a quantum well modulator [13]. In this device, the photodiode happens to be another quantum well p-i-n diode. This FET-biased device (F-SEED) also acts as a three-terminal device, in that the weak signal incident on the photodiode controls a much stronger signal incident on the quantum well modulator.

The present device has two p-i-n diodes, each containing quantum wells in the intrinsic region, with one diode behaving as the load for the other (and vice versa). This device has complementary outputs whose switching point is determined by the ratio of the two optical input powers and acts as a set-reset latch [14]. If both p-i-n diodes are the same, we have a symmetric device (S-SEED). The S-SEED is therefore insensitive to optical power supply fluctuations if both beams are derived from the same source. The device has time-sequential gain, in that the state of the device can be set with low-power beams and read out with subsequent high-power beams. The device also shows good input/output isolation because the large output does not coincide in time with the application of the input signals. Therefore, the device does not require the critical biasing that is common to most optically bistable devices, and has the attributes of a three-terminal device. A similar device, a wavelength converter, has also been demonstrated using one p-i-n diode with InGaAs/InP quantum wells and another diode using GaAs/AlGaAs quantum wells [15].

We will begin by briefly describing the S-SEED's that were used in the experiments that we present here and

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explain the basic operation of the S-SEED. We will then show how the devices can be cascaded and how they can be used for logic functions. Finally, we will describe a differential modulator that generates a complementary set of output beams with a single voltage control lead and a differential detector that gives an output voltage dependent on the ratio of two optical input powers.

II. DEVICE FABRICATION

The schematic and physical layout of the device are shown in Fig. 1 [14]. The material was grown by molecular beam epitaxy on an Si-doped n-type GaAs substrate. The p region was grown as a fine-period GaAs/AlGaAs superlattice to improve the quality of the material. The structure, which is n-i-p-i-n, results in two back-to-back diodes between the substrate and the top n regions. The multiple quantum well p-i-n diodes (on top) are connected “horizontally” by external connection rather than “vertically” during growth as in the D-SEED, circumventing the problem that limited the speed of the D-SEED, namely, the limited current that could be carried by the internal ohmic contact in that structure. The isolation diodes (bottom), comprised of the AlGaAs i and n and superlattice p regions, ensure electrical isolation between the p regions of the two quantum well diodes. In operation, both of the isolation diodes are always reverse biased by connecting the substrate to a positive voltage. The quantum well diodes are made by etching separate mesas and are electrically connected using ohmic contacts and evaporated gold over a polyimide insulator. The mesas are $\sim 200 \times 200 \mu\text{m}$ on $400 \mu\text{m}$ centers, and the optical window on each mesa is $\sim 100 \times 200 \mu\text{m}$. The substrate is cleaved into separate 1×2 arrays that are packaged individually. The electrical connections to the device are made using silver epoxy to hold the bond wires to the gold metalization. A connection was also made to the center of the device (between the two quantum well p-i-n diodes) so that they could also serve as modulators or detectors. The GaAs substrate and buffer layer are etched away underneath the optical windows, and an antireflection coating is applied.

III. DEVICE OPERATION

The operation of the device can be understood through the use of load lines as shown in Fig. 2(a). By solving for the voltages across the quantum well diodes as a function of the two input power levels, we can determine the optical transmission of the two diodes and hence the input/output characteristics. The solid curves are the photocurrent versus voltage for a quantum well diode at three different input powers. The dashed line is the current of the rest of the circuit versus the voltage on the first p-i-n diode. In this case, this current is the photocurrent on the second (load) quantum well diode for an input power on the load diode equal to that incident on the first diode in the middle curve. The solid curve in Fig. 2(b) is the transmission versus voltage for the first quantum well diode, and the dashed curve is the transmission of the load quan-

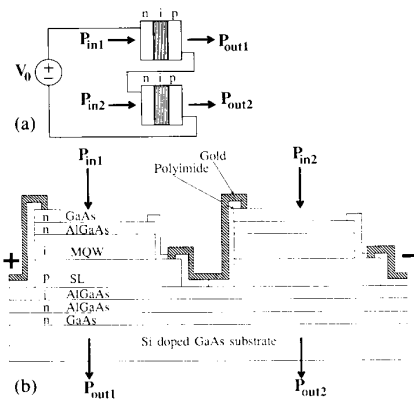


Fig. 1. The symmetric SEED. (a) Schematic diagram. (b) Physical layout (not to scale). The Al mole fraction in $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As}$ is 0.4. Epitaxial layer thicknesses and dopings (from bottom to top): n-GaAs— $0.17 \mu\text{m}$, $n = 10^{18} \text{ cm}^{-3}$; i-AlGaAs— $1.92 \mu\text{m}$; p-superlattice (SL)—250 periods of alternate 25 \AA AlGaAs and 21 \AA GaAs, $p = 10^{18} \text{ cm}^{-3}$; i-multiple quantum wells (MQW)—63 periods of alternate 80 \AA AlGaAs and 105 \AA GaAs layers; n-AlGaAs— $0.64 \mu\text{m}$, $n = 10^{18} \text{ cm}^{-3}$; n-GaAs— $0.105 \mu\text{m}$, $n = 10^{18} \text{ cm}^{-3}$. Both the GaAs substrate and the GaAs buffer layer are removed by a selective etch under the device active area.

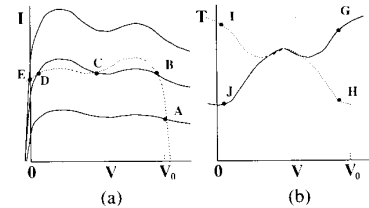


Fig. 2. Characteristics of both quantum well diodes. (a) Solid curves are the photocurrent versus voltage for a quantum well diode at three different optical input powers. Dashed line is the photocurrent on the load quantum well diode versus voltage on the first quantum well diode for an optical input power on the load diode equal to that incident on the first diode in the middle curve. (b) Solid curve is the transmission versus voltage for the first quantum well diode. Dashed curve is the transmission of the load quantum well diode versus the voltage on the first diode.

tum well diode versus the voltage on the first diode. Since the voltage on the load diode is equal to the supply voltage minus the voltage on the first diode, the transmission versus voltage and current versus voltage curves for the load diode are the same as the first diode, but shifted to the right by an amount equal to the supply voltage and inverted from left to right. The responsivity (current versus voltage) and optical transmission curves were measured by sinusoidally varying the voltage across only one of the quantum well diodes and measuring the corresponding current (using a series resistor with a voltage drop of about 0.1 V) and optical output. The data in Fig. 2 were measured at 856 nm , which corresponds to the excitonic absorption peak wavelength occurring at 0 V external bias. As the bias is increased, the electric field perpendicular to the wells causes the location of the peak to shift to longer wavelengths (the QCSE), and the absorption at 856 nm decreases and the optical transmission increases. By a similar argument, the responsivity of the device decreases with increasing applied voltage (because less light

is absorbed) provided that the intrinsic region is fully depleted of carriers, which occurs at voltages greater than ~ 2 V. With roughly equal optical input powers on each diode [the middle solid curve in Fig. 2(a)], there are three intersection points (*B*, *C*, and *D*), and the device is bistable. At intersection point *D*, the first diode has low voltage and low transmission [point *J* in Fig. 2(b)], whereas the load diode has high voltage and high transmission [point *I* in Fig. 2(b)]. At intersection point *B*, the situation is exactly reversed corresponding to the other stable state, with the first diode having high voltage and high transmission (point *G*) and the load diode having low voltage and low transmission (point *H*). Point *C* is easily shown to be unstable [6].

In operation, two sets of two beams are incident on the device as shown in Fig. 3(a). First, a set of unequal power beams (signal beams) sets the state of the device. Provided the difference in power between the signal beams is sufficiently large, we can force the device to be in one state [point *A* in Fig. 2(a)] or the other state [point *E* in Fig. 2(a)]. A contrast ratio of 2:1 is more than sufficient to ensure this, and since the signal beams will likely be derived from the output of another S-SEED, the contrast ratio will normally be greater than 2:1. For example, if the power incident on the first diode is significantly less than that on the load diode, the device will be in a state shown by point *A* in Fig. 2. Conversely, if the power incident on the first diode is significantly greater than that on the load diode, the device will be in a state shown by point *E* in Fig. 2. Since the currents from the first diode and load diode scale with input power, it is only the ratio of the two input powers that determines the operating point. Thus, if both input signal beams are derived from the same laser, any variations of the laser power will occur in both beams, and the device will be insensitive to these fluctuations.

The second set of beams are equal-power clock beams that are used to read the state of the device. During the application of the signal beams, the clock beam powers must be low compared to the signal beam powers. Since the state of the device is determined by the ratio of the total power incident on each of the two quantum well p-i-n diodes, any clock power present when the signal beams are trying to set the state of the device will effectively degrade the contrast ratio of the input beams, possibly causing the device not to switch. After the state of the device has been set, we apply the equal power clock beams to each diode to read the state. As we stated above and illustrated in Fig. 2(a), the device is bistable when there are three intersection points (i.e., *B*, *C*, and *D*). This will only occur if we operate the device at a wavelength where there is a region of decreasing absorption (and therefore decreasing current) for increasing voltage (for example, at the wavelength shown in Fig. 2). Furthermore, the device will only be bistable when the optical input power levels are comparable, and will have only a single state when the power in one diode significantly exceeds the power in the other. Therefore, when reading

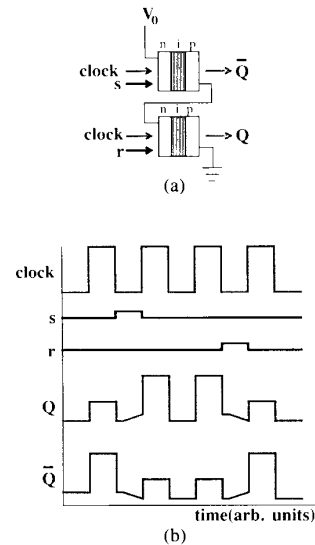


Fig. 3. S-SEED operating as a clocked S-R flip-flop. (a) Schematic diagram showing signal inputs, *s* (set) and *r* (reset), clock inputs, and outputs, *Q* and \bar{Q} . (b) Timing diagram illustrating time-sequential gain.

the state of the device, the two clock beams must have sufficiently equal optical powers to ensure that the device remains in the bistable region so that either state can be read out without altering it. However, since the bistable loop is wide (particularly at 15 V), it is easy to satisfy this requirement.

This device has an interesting attribute which we call "time-sequential gain." Since the currents in both the first diode and load diode scale with input power, the operating point when read out will be independent of clock power and only dependent on the state of the device before the clocks were applied [i.e., point *A* or *E* in Fig. 2(a)]. Therefore, the input clock powers may be many times greater than the input signal powers that were used to set the state of the device, and the device has optical gain illustrated in Fig. 3(b). It is not optical gain in the sense of an optical amplifier where the optical signal itself is amplified, but in this device, the weaker signal beams control a set of stronger clock beams, much like in a bipolar transistor where a weaker base current controls a stronger collector current. Because we apply the signal beams first and then the clock beams, we refer to this as time-sequential gain. In addition, because the output does not coincide in time with the application of the input, the device has effective input/output isolation in that a reflection of the output signal back onto the input will not occur at a time when the device is most sensitive to the input. Since the device can hold its state (i.e., the voltage on the two diodes) for a short period of time without any incident light, it does not matter if there is a time between the removal of the signal beams and the application of the clock beams where no light is present. Therefore, the timing of the optical inputs is not critical.

The measured input/output characteristics of the device are shown in Fig. 4. The characteristics were measured

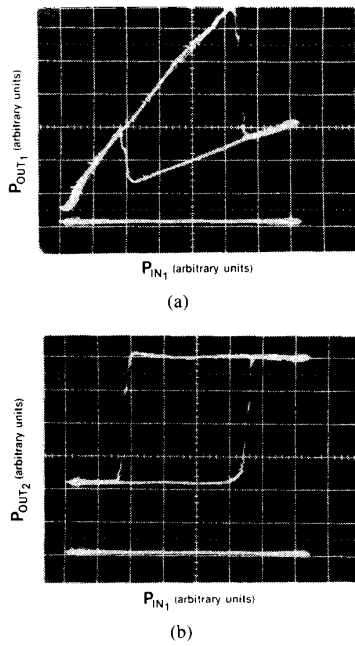


Fig. 4. Optical input/output characteristics of the S-SEED measured at a supply voltage of 15 V at 856 nm with average input power levels of $\sim 20 \mu\text{W}$. (a) Optical power exciting first diode (P_{out_1}) versus optical power incident on first diode (P_{in_1}) with the optical power incident on second diode (P_{in_2}) held constant. (b) Optical power exciting second diode (P_{out_2}) versus P_{in_1} with P_{in_2} held constant. Optical transmission levels are ~ 41 and 14 percent for the two states shown in the figure.

using an argon-ion-laser-pumped styryl 9 dye laser, although some measurements were also made using a commercially available AlGaAs semiconductor diode laser. To measure bistability and switching speeds, the light emitted from the laser was split into two paths using a polarization beam splitter. The optical power in one side was varied using an acousto-optic modulator. The two beams are combined using another polarization beam splitter and focused through a $5\times$ microscope objective onto the device. The spot size of the optical beams was varied from ~ 7 to $50 \mu\text{m}$ in diameter as measured using a television camera looking at the light transmitted through the device. The relative optical power of the light in each path was adjusted by rotating a half-wave plate to vary the polarization of the light incident on the first beam splitter.

The device showed bistability at 856 nm for supply voltages greater than 3 V, and showed bistability from 845 to 862 nm at 15 V. The transmission ($P_{\text{out}}/P_{\text{in}}$) of the quantum well diodes at 856 nm in the two states were 31 and 14 percent at 5 V (2.2:1 contrast ratio), increasing to 41 and 14 percent (2.9:1 contrast ratio) at 15 V. The devices had greater than a 2:1 contrast ratio from 855.5 to 857 nm at 5 V and from 854.7 to 857.7 at 15 V. It follows directly from the voltage dependence of the optical transmission of the device that the contrast ratio is better at high voltages than at low voltages because the transmission of the device in the ‘‘high’’ state is greater at higher voltages. Also, since the exciton peak shifts more at higher applied fields, the wavelength range over

which there is decreasing absorption with increasing field is larger (the condition required for bistability), and thus there is a greater range of operating wavelengths at higher voltages.

All of the above measurements were made with optical input power levels below $100 \mu\text{W}$. The fastest switching time measured was 40 ns when the modulation frequency of the acousto-optic modulator was 1 MHz, increasing to 60 ns for a 100 kHz sine wave output. In these measurements, the average optical power level incident on each mesa was $\sim 8 \text{ mW}$. This speed was limited by the maximum optical power available rather than any intrinsic limit of the device. To see how the measured speed compares to the predicted speed, consider that the speed is determined by the time it takes to charge the capacitance of each p-i-n diode by the photocurrent generated in the diodes. If we use Kirchoff’s current law at the center node of the two diodes, we get

$$P_{\text{in}_1}S(V) - P_{\text{in}_2}S(V_0 - V) + C \frac{dV}{dt} - C \frac{d(V_0 - V)}{dt} = 0 \quad (1)$$

where C is the capacitance of a single p-i-n diode, P_{in_1} and P_{in_2} are the optical input powers incident on the first and second diodes, respectively, $S(V)$ and $S(V_0 - V)$ are the responsivities of the two diodes, V_0 is the power supply voltage, and V is the voltage across the first p-i-n diode. This expression is difficult to calculate directly, so we can make an approximation by assuming that the responsivity of the two diodes is constant and given by \bar{S} and assuming dV/dt is equal to the voltage V_0 divided by the switching Δt . In this case, we get

$$\Delta t = \frac{C_{\text{tot}}V_0}{\bar{S}(P_{\text{in}_2} - P_{\text{in}_1})} \quad (2)$$

where C_{tot} is the total device capacitance across the two quantum well p-i-n diodes plus the additional capacitance of one of the isolation diodes that were used to isolate the two p layers of the quantum well diodes. For these devices, the total capacitance is $\sim 8 \text{ pF}$ and the responsivity is $\sim 0.3 \text{ A/W}$. For this measurement, the supply voltage was 10 V, the spot sizes were $50 \mu\text{m}$ in diameter, and the average optical input power level into each p-i-n diode was 8 mW at 866 nm. (The wavelength was adjusted for optimum contrast ratio at these power levels and the shift in wavelength from the optimum at low power levels was probably due to local heating of the device.) If we use these numbers in (2), we can calculate the switching speed of 33 ns, which agrees well with our measured results at a modulation frequency of 1 MHz. This method of calculating switching speeds ignores the effects of critical slowing down that are present in any bistable device, and therefore one must solve (1) to calculate the switching speed as a function of the modulation frequency of the ramped signal.

We can define an optical switching energy E_{opt} that is

the additional optical energy that would have to be provided by a single additional beam to switch a symmetrically biased device. An approximation to E_{opt} can be found by multiplying both sides of (2) by the difference in the optical power levels incident on the two diodes. This gives

$$E_{\text{opt}} = \Delta t \Delta P = \frac{C_{\text{tot}} V_0}{S} \quad (3)$$

where $\Delta P = P_{\text{in}_2} - P_{\text{in}_1}$. Using the values given above, E_{opt} for this device is 264 pJ and the corresponding measured value is 320 pJ for the 1 MHz sine wave input. Equation (3) shows that the speed and power scale inversely and the switching energy remains constant. [This is also evident from the exact solution to (1).] We measured a constant switching energy from 10 nW to 8 mW, limited on the low end by our ability to detect small signals and on the high end by the laser power available. We also observed that, for small spot sizes less than $\sim 12 \mu\text{m}$, a degradation in contrast ratio was seen at power levels greater than 1 mW. We believe this is related to saturation of the quantum well material. Similar saturation effects have also recently been reported [16]. This saturation may ultimately be the upper limit on switching speed that can be obtained. (Without saturation, carrier transit times and series resistance will limit the switching speed.) We could also define the total optical switching energy as being the total average power incident on both p-i-n diodes times the switching time. This gives a somewhat higher number for the measured optical switching energy of 640 pJ. Since the usable device area is $40\,000 \mu\text{m}^2$, the total optical switching energy density is $16 \text{ fJ}/\mu\text{m}^2$.

There is also an electrical switching energy which can be defined as

$$E_{\text{elect}} = \frac{1}{2} C_{\text{tot}} V_0^2 \quad (4)$$

Using a supply voltage of 10 V, the electrical switching energy is 400 pJ, which is comparable to the optical switching energy. Additionally, both the electrical and optical switching energies are linearly related to the device capacitance, so the switching energies could be reduced by a factor of two by growing the material on a semi-insulating substrate and eliminating the two isolation diodes, one of which needs to be charged or discharged during switching. Of course, this required switching energy can be reduced further by making the devices smaller. Experience with D-SEED's does show performance scaling with device area as expected [8].

IV. CASCADED DEVICES

Since bistability was observed at optical input powers varying from less than 10 nW to greater than 8 mW, we can have a large effective signal gain. Of course, switching at low powers takes proportionately longer, so that gain is obtained at the expense of switching speed. Thus, the device has a constant gain-bandwidth product, just like many other amplifiers. The amount of gain in a system built entirely with S-SEED's will be determined by

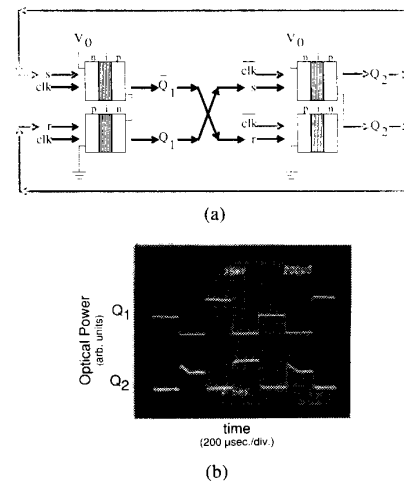


Fig. 5. Photonic ring counter. (a) Schematic diagram “*clk*” and “ $\overline{\text{clk}}$ ” are the clock and complement clock beams, and *s* and *r* are the set and reset beams, respectively. (b) Optical output power levels (in arbitrary units) of the bottom quantum well p-i-n diode from the first (Q_1 —top trace) and second (Q_2 —bottom trace) devices.

the absorption losses in the devices themselves, the fan-out of the devices, and reflections, absorption, and scattering losses in the optical components used to interconnect the devices. We want to minimize these losses so that the signal beams will be as large as possible and the switching time will be small.

A photonic ring counter was built to demonstrate cascading of the S-SEED's. Such a counter can be made by routing the outputs from one device onto the inputs of the other device as shown in Fig. 5(a). The operation of the counter is described as follows. Suppose Q_1 is initially greater than the \overline{Q}_1 . This means the *s* input is greater than the *r* input to the second flip-flop. When the *clk* inputs are applied to the second flip-flop, Q_2 will be greater than the \overline{Q}_2 . Therefore, the *r* input will be greater than the *s* input to the first flip-flop. When the *clk* inputs are then applied to the first flip-flop, Q_1 will be less than \overline{Q}_1 . Therefore, each flip-flop output toggles between a logic one and a logic zero on subsequent clock cycles. This is shown experimentally in Fig. 5(b). Two current-modulated AlGaAs semiconductor diode lasers supplied the complementary clock beams to the devices. The lasers were turned off when the clock was in the low state, ensuring that the signal beams were greater than the clock beams. The use of complementary clock beams for cascaded devices would be used in any system built using S-SEED's. A beam splitter not shown in the figure was used for the output beams to simulate a fan-out of two and provide an optical signal for the photodiodes. The maximum speed of the ring counter ($T_s \sim 300 \mu\text{s}$), shown in Fig. 5(b), was limited by the laser power available ($\sim 125 \mu\text{W}$ per p-i-n diode). It was estimated that the signal beams incident on the devices have optical powers of ~ 7.8 and $\sim 3.9 \mu\text{W}$ for the complementary inputs. Sources of loss include the loss of the quantum well diodes in the “on” state (transmission ~ 33 percent), excess losses of the

lenses and the beam splitter (transmission ~ 38 percent), and the fan-out of two. Even though the total optical switching energy of these devices was 640 pJ, the total optical energy that was supplied by each laser supplying the clock beams in the ring counter was ~ 75 nJ ($2 \times 125 \mu\text{W} \times 300 \mu\text{s}$). Thus, the optical energy that must be supplied for each device when attempting to build photonic switching or optical computing systems using these devices is considerably greater than the energy required to switch a single uncascaded device. Of course, we expect improvements in switching speed and energy of these systems as well by using smaller devices and by using optical elements with smaller losses.

V. DIFFERENTIAL LOGIC

Since the S-SEED has many desirable qualities, such as insensitivity to optical power supply fluctuations and time-sequential gain, we would like to be able to perform logic functions (such as NOR, OR, NAND, and AND) in addition to memory functions (i.e., set–reset latch). We would like the inputs to be differential, thus still avoiding any critical biasing of the device. We have demonstrated a differential S-SEED logic gate performing any of the four logic functions that, like the S-SEED flip-flop, does not require critical biasing and has time-sequential gain. One way to achieve a logic gate operation is shown in Fig. 6(a). We will define the logic level of the inputs as being represented by the power of the signal on the set input relative to the power of the signal incident on the reset input. For example, when the power of the signal incident on the set input is greater than the power of the signal on the reset input, we will call this a logic “1.” For the noninverting gates OR and AND, we can represent the output logic level by the power of the signal coming from the Q output relative to the power of the signal coming from the \bar{Q} output. As before, when the power of the signal incident coming from the Q output is greater than the power of the signal on the \bar{Q} output, we will call this a logic “1.” To achieve AND operation, the device is initially set to its “off” or logic “0” state (i.e., Q low and \bar{Q} high) with preset pulse B incident on only one p-i-n diode as shown in Fig. 6. If both input signals have logic levels of “1” (i.e., set = 1, reset = 0), then the S-SEED AND gate is set to its “on” state. For any other input combination, there is no change of state, resulting in AND operation. After the signal beams determine the state of the device, the clock beams are then set high to read out the state of the AND gate. For NAND operation, we simply redefine the logic level as being represented by the power of the \bar{Q} output signal relative to the power of the Q output signal. That is, when the power of the signal incident coming from the \bar{Q} output is greater than the power of the signal on the Q output, we will now call this a logic “1.” The operation of the OR and NOR gates is identical to the AND and NAND gates except that preset A is used instead of preset B . Thus, a single array of devices can perform any or all of the four logic functions and memory functions with the proper optical interconnections and preset pulse routing.

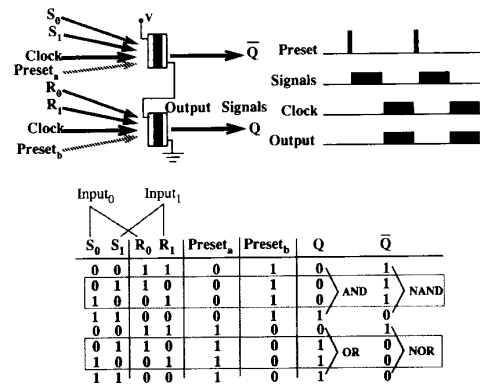


Fig. 6. S-SEED logic gate showing schematic diagram, timing diagram, and truth table.

We have tested the logic gate using the outputs from two electrically driven two S-SEED devices (we will discuss this modulator in the next section) to provide the correct signal levels for the input of the logic gate. The optical input signals to the modulators consisted of a pair of clock beams, and the clock beams incident on the logic gate were the complement of the clock beams on the modulator, as would be the case be if we cascaded logic gates. In Fig. 7(a)–(d), all four logic functions are demonstrated, showing the two set inputs and either the Q or \bar{Q} outputs, as dictated by the table in Fig. 6. The preset pulse was an acoustooptic modulated HeNe laser at 633 nm at peak power levels from ~ 6 to $\sim 100 \mu\text{W}$ at 12.5 percent duty cycle, although any wavelength that is significantly absorbed by the device can be used. In theory, a short pulse from a mode-locked laser could preset the device very quickly, provided that it has the required energy. In the experiment, the preset pulse was applied at the beginning of the data input; however, it may be applied before the data input, resulting in very little change in the speed of operation. The fastest switching speed ($T_s \sim 200 \mu\text{s}$) used a $6 \mu\text{W}$ prepulse, and was again limited by the available laser power at 855 nm ($77 \mu\text{W}$ per p-i-n diode). In this case, we estimate the individual signal levels incident on the logic gate at ~ 4.8 and $2.4 \mu\text{W}$ for the complementary input beams. In this experiment, the total optical energy of the clock beams incident on each of the differential modulators was ~ 31 nJ ($2 \times 77 \mu\text{W} \times 200 \mu\text{s}$). Since the logic gate has two sets of input beams present, both working to change the state of the device, less energy is needed in the clock beams of cascaded logic gates than cascaded flip-flops.

Both the photonic ring counter and differential logic gate experiments were built with devices with contrast ratios of $\sim 2 : 1$. This was somewhat less than the $2.9 : 1$ contrast that we measured using the dye laser because the semiconductor lasers were not quite at the optimum wavelength. These experiments demonstrate that poor contrast ratios do not limit the usefulness of these devices. It is true, however, that the required optical switching energy of the devices depends on the *difference* of the two input

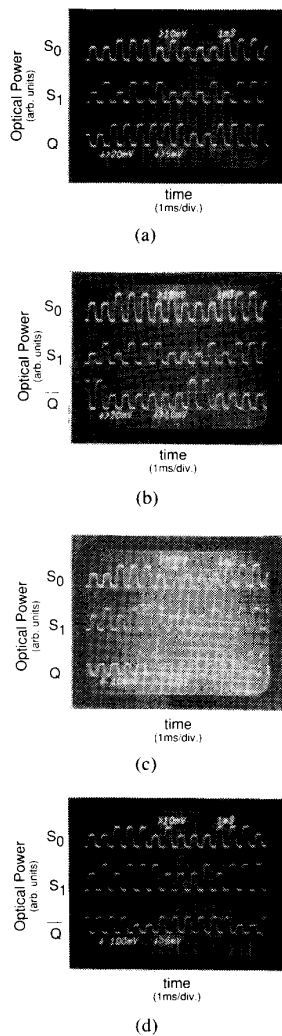


Fig. 7. Measured S-SEED logic gate. (a) OR gate. (b) NOR gate. (c) AND gate. (d) NAND gate. Shown are the optical data inputs (s_0 —top trace and s_1 —middle trace) and optical output (Q or \bar{Q} —bottom trace).

power levels as given in (1)–(3). If we assume that the inputs are derived from the output of another S-SEED, and if we improved the contrast of the devices from 2:1 to an infinite contrast by removing the smaller signal completely, we would only improve the switching energy by a factor of two. The S-SEED is perhaps the first device where a moderately poor contrast ratio is not a major limitation in trying to build optical processing systems.

VI. DIFFERENTIAL MODULATOR/DETECTOR

Quantum well modulators have been demonstrated with good contrast ratios and high speeds at a variety of wavelengths (see, for example [17], [18]). As we mentioned in the last section, we can adjust the voltage in the center of the device (between the two quantum well p-i-n diodes) to get a differential or complementary modulator with two complementary outputs with only a single voltage control

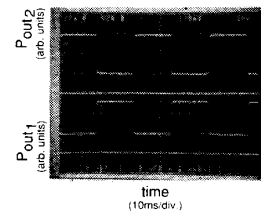


Fig. 8. Dual outputs from the differential quantum well modulator measured at 855.8 nm with a power supply voltage of 15 V and modulating voltage swing of 15 V. Horizontal lines are baselines for the traces immediately above them.

lead. The device has proven useful in providing an interface between electronics and optical logic devices described above.

The characteristics of the modulator were measured by applying two CW signals at 856 nm to the two diodes of the differential modulator. Fig. 8 shows the two complementary output signals with a supply voltage of 15 V and a modulating voltage swing of ~ 15 V. The slight difference in the contrast ratio for the two outputs may be due to a slightly asymmetric modulating voltage. For high-speed measurements, a 50Ω resistor was connected across the bottom quantum well p-i-n diode and the power supply was bypassed by an external 1000 pF chip capacitor as well as 9.5 pF of additional capacitance on the chip. The fastest switching speed was ~ 1.5 ns, limited by the RC time constant of the modulator ($2.2RC = 0.88$ ns), the parasitic capacitance of the test fixture, and inductance of the relatively long bond wires used to connect the modulator to the external modulating voltage. In this measurement, the contrast ratio was only $\sim 1.4:1$ because the modulating voltage swing was only ~ 2 V. Faster switching speeds should be easily attainable with smaller devices and better packaging.

In a second mode of operation, the differential modulator can act as a detector as shown in Fig. 9. At 856 nm, the detector output voltage is bistable when the two optical input power levels are comparable, and either essentially 0 V (or a slight forward bias voltage) or the supply voltage when the optical input power into one of the p-i-n diodes exceeds the other one by a significant amount. Operating at a longer wavelength (~ 865 nm) gives an output voltage that is not bistable, but roughly proportional to the ratio of the optical powers. Resistively loading each p-i-n diode can also remove the bistable characteristics, particularly when the optical powers are low. For example, at a supply voltage of 10 V and $20 \mu\text{W}$ of input power per diode, the device was bistable with $11 \text{ M}\Omega$ across each device, but was not bistable with $1 \text{ M}\Omega$ as shown in Fig. 10. We can easily understand this behavior by using the same load line techniques that we used to analyze the operation of the S-SEED. We will consider the same current-voltage characteristics shown in Fig. 2, and add currents flowing through the resistors as shown in Fig. 11. In the case of a resistor across the load, an additional current equal to $(V_0 - V)/R$ must be added in parallel with the photocurrent in the load p-i-n diode. For

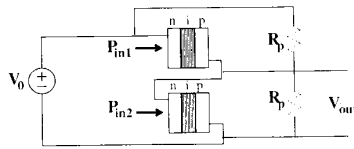


Fig. 9. Schematic diagram of a differential detector. P_{in1} and P_{in2} are the optical input powers and V_{out} is the detector output voltage.

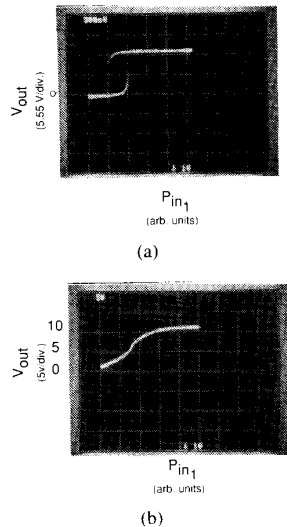


Fig. 10. Detector voltage output as a function of the optical input power on the top p-i-n diode P_{in1} with the optical input power level on the bottom p-i-n diode P_{in2} equal to $20 \mu\text{W}$ and the power supply voltage equal to 10 V . Both optical inputs at 856 nm . (a) Parallel resistance of $11 \text{ M}\Omega$ (Since the oscilloscope input impedance is $1 \text{ M}\Omega$, a $10 \text{ M}\Omega$ resistor was connected in series with the scope to read the detector voltage. Hence, the detector output voltage is equal to the oscilloscope voltage multiplied by 11.) (b) Parallel resistance of $1 \text{ M}\Omega$.

a resistor in parallel with the first p-i-n diode, the additional current of V/R must be added in parallel with the photocurrent from that diode. It is easy to see that effectively the curves are tilted upward toward the center of the graph (i.e., $V_0/2$). If the value of the resistance is low enough, there will be only one intersection point for all optical input powers and the device will not be bistable. The resistance required to maintain bistability scales with optical input power as well, and for small optical input powers, this resistance must be very large. When the device is not bistable, the output voltage will be a slightly nonlinear function of the ratio of the two optical input power levels centered at one half of the supply voltage. Resistively loading only one of the two p-i-n diodes also effects the characteristics in such a way that bistability is maintained with lower parallel resistances. Since the $I-V$ curve for one of the two p-i-n diodes is tilted upward and the other is not, it is no longer a symmetric device for power levels that generate currents comparable to V_0/R .

The same analysis technique can also be applied to leakage currents flowing in an S-SEED. If the leakage currents are too high, the device will not be bistable at

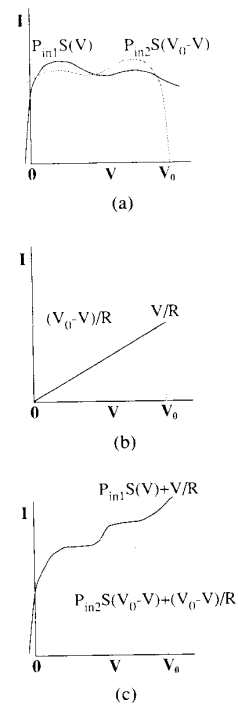


Fig. 11. Current-voltage characteristics of a resistively loaded differential detector. (a) Photocurrent generated by quantum well diodes. (b) Resistive current. (c) Sum of both currents showing loss of bistability in the detector.

low operating powers (or it may be asymmetric), and thus the ability to achieve time-sequential gain over a wide dynamic range is lost.

VII. CONCLUSION

In conclusion, we have demonstrated the symmetric self-electrooptic effect device (S-SEED) that consists of two quantum well p-i-n diodes connected electrically in series and operates as an optical set-reset latch. The device is insensitive to optical power supply fluctuations, has effective optical gain, and has good input output isolation, attributes that make it behave like a three-terminal device instead of traditional two-terminal devices. We have shown how to make a differential logic gate using these devices capable of performing NOR, NAND, OR, and AND functions, and have demonstrated cascability of the devices in a photonic ring counter. Using the same devices, we have shown how to make a modulator that provides two complementary outputs with a single voltage control lead. The device doubles as a detector that gives an output voltage dependent on the ratio of two incident optical signals. The symmetric SEED and these related devices are very flexible and powerful devices and potentially very useful for optical signal processing.

ACKNOWLEDGMENT

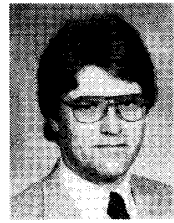
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