Charge trapping at the low-*k* dielectric-silicon interface probed by the conductance and capacitance techniques

J. M. Atkin,[1] E. Cartier,[2] T. M. Shaw,[2] R. B. Laibowitz,[3] and T. F. Heinz[1,3,a)]
[1]*Department of Physics, Columbia University, New York, New York 10027, USA*
[2]*IBM Research Division, Yorktown Heights, New York 10598, USA*
[3]*Department of Electrical Engineering, Columbia University, New York, New York 10027, USA*

(Received 31 July 2008; accepted 4 September 2008; published online 23 September 2008)

Trap states close to the interfaces in thin films of porous low-*k* dielectric materials are expected to affect interfacial barriers with contacts and consequently electrical leakage and reliability in these materials. These interfacial traps were investigated using capacitance and conductance measurements in metal/insulator/silicon capacitor structures composed of carbon-doped oxide low-*k* dielectric films with gold counterelectrodes. The measurements yielded information on the charge state of the low-*k* dielectric and an estimated density of traps near the Si interface of 2×10^{11} cm^{-2} eV^{-1}, considerably greater than in typical SiO_2 films. The effects of temperature and annealing were also investigated. An activation energy of 0.36 ± 0.04 eV for trap filling and emptying was inferred. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2990648]

Electron trap states within low-*k* dielectric (LKD) films play a significant role in electrical leakage and time-dependent dielectric breakdown in these materials.[1] An important conduction mechanism within these LKD films involves charge hopping from trap states, as described, for example, by the Poole–Frenkel model.[2,3] Thus, the properties of the trap states are closely related to the overall reliability of LKDs, a central problem for many industrial applications of these insulating films.[3,4] In particular, trapped charge at interfaces is important in charge transport since it may change the barrier height and provide a low-energy conduction pathway.[5]

In the present investigation, we characterize trap states within the LKD films by means of impedance measurements. Impedance spectroscopy of metal-insulator-semiconductor (MIS) structures provides a wealth of information about charge trapping processes in both the bulk of the insulator and the trapping properties of the Si/insulator interface.[6,7] The semiconductor (silicon) surface potential provides a monitor of charging and trapping in the adjoining insulator. The interface states are characterized using frequency-dependent ac conductance $G(\omega)$. From the magnitude and frequency dependence of $G(\omega)$ we can identify both the concentration of trap states and the dynamics of their filling and emptying.[8,9] The present investigations complement our earlier studies[10] of charge transport in LKD materials using internal photoemission spectroscopy. In addition to identification of barrier heights, this work provided information on long-lived trap states presumed to consist of deep levels within the bulk of the film. Here application of impedance spectroscopy permits us to probe the nature of the short-lived states that are characteristic of interfacial trapping.[11]

The LKD films investigated in this study were porous carbon-doped oxide films, sometimes designated as porous SiCOH films, with a relative dielectric constant of $k=2.4$. The materials, of production quality, were obtained from industrial sources as blanket films (see acknowledgments). The films were deposited using plasma-enhanced chemical vapor deposition on *p*-type silicon (100) wafers with resistivities of 1–10 Ω cm. Information about the precursors,[12–14] the conditions of deposition,[15,16] and the structure of the final films[17,18] (as used in integrated circuits) has been reported elsewhere. The surface of the silicon wafers on which the films were deposited was typically covered by a native oxide layer of less than 1 nm thickness. This oxide layer may be important for the interfacial states, as it provides dangling Si bonds similar to those of other Si/SiO_2 interfaces. As in Si/SiO_2, the high-defect transition region is not expected to be abrupt and is likely to extend 3–4 nm into the LKD.[9] The measurements reported in this paper were performed on 130 nm thick LKD films with a thermally deposited thin Au electrode. Gold is used as a counterelectrode because it forms a sharp interface, with little interdiffusion, with the LKD films. The gold electrodes, approximately 25 nm in thickness, had areas of 0.05 and 0.006 cm^2.

Impedance measurements as a function of bias voltage and frequency were performed with a standard impedance analyzer (HP 4194). Our measurements could be performed at temperatures from 0 to 200 °C with control of the sample ambient conditions. Measurements characterized the frequency-dependent impedance $Z(\omega)$ of the structure, where ω denotes the angular frequency. Both the real and the imaginary parts of $Z(\omega)$ provide information about traps. Below we describe this impedance in terms of the equivalent normalized conductance $G(\omega)/\omega=1/\{\omega\,\mathrm{Re}[Z(\omega)]\}$, which is proportional to the power dissipated per cycle, and the capacitance $C(\omega)=1/\{\omega|\mathrm{Im}[Z(\omega)]|\}$. The frequency dependence of these quantities is of particular interest for extracting information about the trap states. For a depleted Si surface, only the capacitance and conductance associated with quickly responding traps exhibit variation with frequency. In capacitance measurements, the experimentally determined system capacitance includes contributions from the oxide layer (C_{ox}) and the depletion layer (C_d) as well as from the interface traps (C_{it}). Conductance measurements access information about the traps more directly. If we consider the capacitance from the oxide and depletion to have small losses, then measured conductance under depletion arises

a)Electronic mail: tony.heinz@columbia.edu.

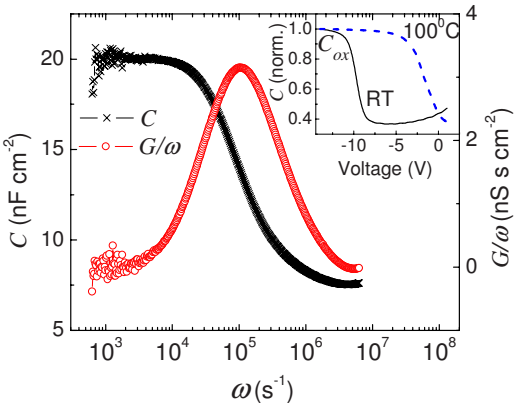

FIG. 1. (Color online) Measured capacitance (C, black crosses) and normalized conductance (G/ω, red circles) per unit area as a function of frequency ω for LKD structure in the as-received condition. The sample was held at room temperature with a dc bias of 0 V. Inset: C-V curves at room temperature (solid black) and 100 °C (dashed blue), indicating that the MIS structure is in depletion at 0 V bias. The oxide capacitance is $C_{ox}=24$ pF cm^{-2}.

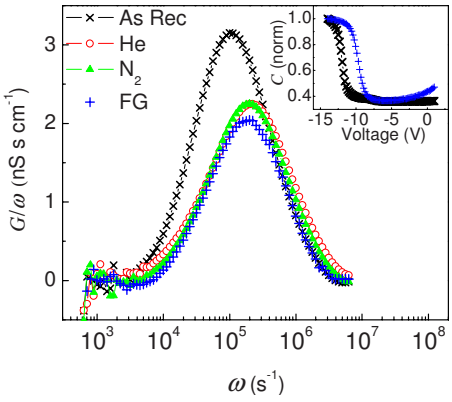

FIG. 2. (Color online) Normalized conductance G/ω as a function of the frequency ω (logarithmic scale) for LKD samples in the as-received form and subjected to annealing at 350 °C for 20 min in an ambient of the indicated gas. The reduced peak height implies a decreased interfacial state density. Inset: C-V curves for an as-received sample (black crosses) and the sample annealed in FG (blue pluses), showing a shift of approximately 2 V in V_{fb}.

only from the contribution of the interfacial trap states (G_{it}).[9]

The frequency-dependent response of our test structures, presented as capacitance C and normalized conductance G/ω (per unit area), is shown in Fig. 1. The measurements were performed at a dc bias of 0 V. For this bias, the MIS structures are in depletion, as can be seen from the voltage dependence of the overall capacitance (inset of Fig. 1). Measurements performed in this regime can be readily analyzed since minority-carrier effects can be neglected.[9] The peak in G/ω corresponds to a maximum in the loss for application of a voltage at a frequency comparable to that of trap filling and emptying. More precisely, within the model proposed by Nicollian and Brews,[9] a peak in G/ω will appear at a frequency of $\omega=1.98/\tau$. Here τ is the interface trap time constant for majority carriers, defined in the circuit model as C_{it}/G_{it}. The model assumes that the interface states are uniformly distributed in energy within the band gap and are all characterized by the same time constant. At the normalized conductance peak, the density of interfacial states D_{it} (per unit area, per unit energy) can be inferred from the relation $G/\omega=0.4eD_{it}$, also derived by Nicollian and Brews.[9] Here e is the electronic charge and the quantity G/ω is evaluated at the frequency where it reaches its maximum. Applying this relation to the data in Fig. 1, we deduce a trap density of 2×10^{11} cm^{-2} eV^{-1} with a trap time constant of $\tau=20$ μs. This rate of filling and emptying is a strong indication that we are detecting trap states at or near the interface, as bulk traps tend to respond more slowly.[10,19]

In Si/SiO_2 systems, the interfacial traps are known to arise principally from dangling bonds at the interface.[20] These traps can be altered by annealing the sample in forming gas (FG), which lowers the density of interfacial states by saturating the dangling bonds.[21] As a comparative study, we examined the results of annealing our LKD samples in various gases. Figure 2 shows conductance data for samples in the as-received state and after annealing at 350 °C for 20 min in He, N_2, and FG. The annealing was performed before deposition of the Au electrodes. The observed decrease in the peak height under all annealing conditions indicates a reduction in the density of interface states. The calculated interfacial trap density D_{it} for samples annealed in He and N_2 was found to be 8×10^{10} cm^{-2} eV^{-1}, a reduction of about 30% from the as-received sample. The sample annealed in FG exhibited a still lower trap density of 7×10^{10} cm^{-2} eV^{-1}. Just as is the case in the Si/SiO_2 interface, the trap density can be decreased by annealing. These values are, however, still appreciably higher than those obtained for good quality SiO_2 films, which typically exhibit an interfacial density of 10^{10} cm^{-2} eV^{-1}.[22] The inset of Fig. 2 shows that there is a corresponding change in the flatband voltage upon annealing, indicating that the total charge has also been decreased.

Measurements at various temperatures were performed on as-received samples to investigate the effect of temperature on both the interface trap state density and trapping rate τ^{-1}. The frequency-dependent conductance data (Fig. 3) show little change in peak height as a function of temperature. On the other hand, we see a large shift in the frequency of the conductance peak. From the relation of $\omega=1.98/\tau$ at the peak, we infer a significant increase in the trapping rate with increasing temperature. As indicated in the inset of Fig. 3, the temperature dependence of the trapping rate can be fitted to a thermally activated form of $\tau^{-1}=\tau_0^{-1}\exp(-E_A/kT)$ with an activation energy of $E_A=0.36\pm0.04$ eV. This energy corresponds to the barrier for

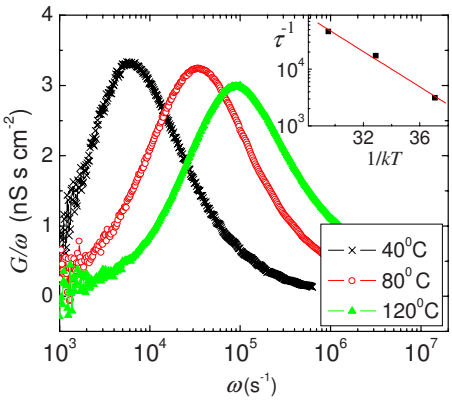

FIG. 3. (Color online) Normalized conductance G/ω as a function of frequency ω (logarithmic scale) for as-received LKD films measured at different temperatures. The shift in the peak frequency as a function of temperature implies a change in the time constant of the traps. Inset: log plot of trapping rate $1/\tau(s^{-1})$ plotted against the reciprocal temperature $1/kT(eV^{-1})$. An activation energy of 0.36 eV is inferred.

populating and depopulating of trap states. This result is consistent with trap distributions measured at the Si/SiO_2 interface,[23] where the majority of traps are approximately 0.3 eV from the intrinsic Fermi energy.

Although the inferred density of interface states D_{it} was not significantly affected by temperature, there is a clear change in the *C-V* behavior. This is indicated in the inset of Fig. 1. As the temperature is increased, we observe a positive shift in the flatband voltage V_{fb}. The shift for a temperature of 100 °C compared with room temperature corresponds to an increase in positive trapped charge of $+10^{17}$ cm^3 throughout the bulk of the LKD film. This effect is much larger than the ordinary thermal shift in V_{fb}[22] and is attributed to the removal of water at higher temperatures. The porous state of the films leads to moisture uptake,[24,25] an effect not present in conventional SiO_2 films.

Our results for LKD films indicate the presence of a significant density of interfacial states. Some of these states are attributed to defects associated with excess silicon or excess oxygen[26] at or near the Si/LKD interface. This assignment is supported by the observed reduction in the density of traps in samples by annealing since such defects react with hydrogen to become electrically neutral.[23] The significant remaining density of interfacial traps after the annealing under the current protocols suggests, however, that there are many more impuritylike defects in Si/LKD than in Si/SiO_2. This difference presumably reflects the more complicated chemical composition of the LKD films, which may include carbon and hydrogen impurities. We note that the annealing procedures used in this work were not adjusted for LKD films. Optimization of the anneal may further reduce the trap densities both at the interface and in the bulk. This should, in turn, provide a link to lower leakage current and improved breakdown and reliability properties for the films.[27]

This work was supported by the Semiconductor Research Corporation (SRC, Contract No. 2005-KC-1292) and New York CAIST program and a graduate fellowship for J.M.A. from the Intel Corporation. We thank Freescale, IBM, and Intel for the LKD films and I. Kymissis and E. Kwok at Columbia for assistance with the deposition of the Au electrodes. We gratefully acknowledge the guidance and discussion with J. Lloyd, R. Rosenberg, and E. Liniger at IBM, E. Andide at Intel, and K. Ramakrishna at Freescale.

[1] K. Y. Yiang, W. J. Yoo, and A. Krishnamoorthy, IEEE Trans. Electron Devices **52**, 2333 (2005).
[2] K. Y. Yiang, W. J. Yoo, Q. Guo, and A. Krishnamoorthy, Appl. Phys. Lett. **83**, 524 (2003).
[3] F. Chen, O. Bravo, K. Chanda, P. McLaughlin, T. Sullivan, J. Gill, J. Lloyd, R. Kontra, and J. Aitken, Proceedings of the IEEE International Reliability Physics Symposium, 2006 (unpublished), Vol. 44, p. 46.
[4] J. Michelon and R. J. O. M. Hoofman, IEEE Trans. Device Mater. Reliab. **6**, 169 (2006).
[5] S. Shamuilia, V. V. Afanas'ev, P. Somers, A. Stesmans, Y. L. Li, Z. Tokei, G. Groeseneken, and K. Maex, Appl. Phys. Lett. **89**, 202909 (2006).
[6] R. S. Muller, T. I. Kamins, and M. Chan, *Device Electronics for Integrated Circuits*, 3rd ed. (Wiley, New York, 2003).
[7] Traps close to the metal/insulator surface are typically screened by the large amount of charge within the metal electrode.
[8] A. S. Nowick and B. S. Berry, *Anelastic Relaxation in Crystalline Solids* (Academic, New York, 1972).
[9] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology* (Wiley, Hoboken, 2003), Chap. 5.
[10] J. M. Atkin, D. Song, T. M. Shaw, E. Cartier, R. B. Laibowitz, and T. F. Heinz, J. Appl. Phys. **103**, 094104 (2008).
[11] P. Balk, in *The Si-SiO2 System*, Materials Science Monographs Vol. 32 (Elsevier, Amsterdam, 1988).
[12] A. Grill and V. Patel, Appl. Phys. Lett. **79**, 803 (2001).
[13] A. Grill, V. Patel, K. P. Rodbell, E. Huang, M. R. Baklanov, K. P. Mogilnikov, M. Toney, and H. C. Kim, J. Appl. Phys. **94**, 3427 (2003).
[14] A. Grill, J. Appl. Phys. **93**, 1785 (2003).
[15] S. M. Gates, D. A. Neumayer, M. H. Sherwood, A. Grill, X. Wang, and M. Sankarapandian, J. Appl. Phys. **101**, 094103 (2007).
[16] S. M. Gates, A. Grill, C. Dimitrakopoulos, D. Restaino, M. Lane, V. Patel, S. Cohen, E. Simonyi, E. Liniger, Y. Ostrovski, R. Augur, M. Sherwood, N. Klymko, S. Molis, W. Landers, D. Edelstein, S. Sankaran, R. Wisnieff, T. Ivers, K. Yim, V. Nguyen, T. Nowak, J. C. Rocha, S. Reiter, and A. Demos, Proceedings of the Advanced Metallization Conference, 2006 (unpublished), p. 351.
[17] A. Grill and D. A. Neumayer, J. Appl. Phys. **94**, 6697 (2003).
[18] V. Ligatchev, T. K. S. Wong, B. Liu, and J. Rusli, J. Appl. Phys. **92**, 4605 (2002).
[19] R. J. Carter, E. Cartier, M. Caymax, S. De Gendt, R. Degraeve, G. Groeseneken, M. Heyns, T. Kauerauf, A. Kerber, S. Kubicek, G. Lujan, L. Pantisano, W. Tsai, and E. Young, Proceedings of the IEEE International Workshop on Gate Insulators, Tokyo, 2001 (unpublished), p. 94.
[20] E. Cartier, J. H. Stathis, and D. A. Buchanan, Appl. Phys. Lett. **63**, 1510 (1993).
[21] E. Cartier and J. H. Stathis, Appl. Phys. Lett. **69**, 103 (1996).
[22] S. Sze and K. Ng, *Physics of Semiconductor Devices* (Wiley, Hoboken, 2007).
[23] M. J. Uren, J. H. Stathis, and E. Cartier, J. Appl. Phys. **80**, 3915 (1996).
[24] R. A. Farrell, K. Cherkaoui, N. Petkov, H. Amenitsch, J. D. Holmes, P. K. Hurley, and M. A. Morris, Microelectron. Reliab. **47**, 759 (2007).
[25] J. R. Lloyd, E. Liniger, and T. M. Shaw, J. Appl. Phys. **98**, 084109 (2005).
[26] T. Sakurai and T. Sugano, J. Appl. Phys. **52**, 2889 (1981).
[27] Y. Li, G. Groeseneken, K. Maex, and Z. Tokei, IEEE Trans. Device Mater. Reliab. **7**, 252 (2007).