COMMUNICATION

Transparent electrode requirements for thin film solar cell modules

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The transparent conductor (TC) layer in thin film solar cell modules has a significant impact on the power conversion efficiency. Reflection, absorption, resistive losses and lost active area either from the scribed interconnect region in monolithically integrated modules or from the shadow losses of a metal grid in standard modules typically reduce the efficiency by 10–25%. Here, we perform calculations to show that a competitive TC must have a transparency of at least 90% at a sheet resistance of less than 10 Ω/sq (conductivity/absorptivity $\geq$ 1 Ω^{-1}) for monolithically integrated modules. For standard modules, losses are much lower and the performance of alternative lower cost TC materials may already be sufficient to replace conducting oxides in this geometry.

Thin film solar cell modules can be manufactured either as a series of individual standard cells strung together in a fashion similar to silicon wafer based solar modules or as a series of cells monolithically interconnected during the film deposition process (Fig. 1). For both architectures, the top electrode has a significant impact on the efficiency and much of this reduction in efficiency is due to trade-offs associated with the transparent conductor (TC) material. Making the TC thin to increase its transmittance to light raises resistive losses. Making the finger spacing or electrode width narrow to reduce resistive losses causes a larger fraction of the module area to be composed of dead space, where the dead space is either shadow losses under the metal grid for standard cells or the interconnect scribe area for monolithically interconnected cells.

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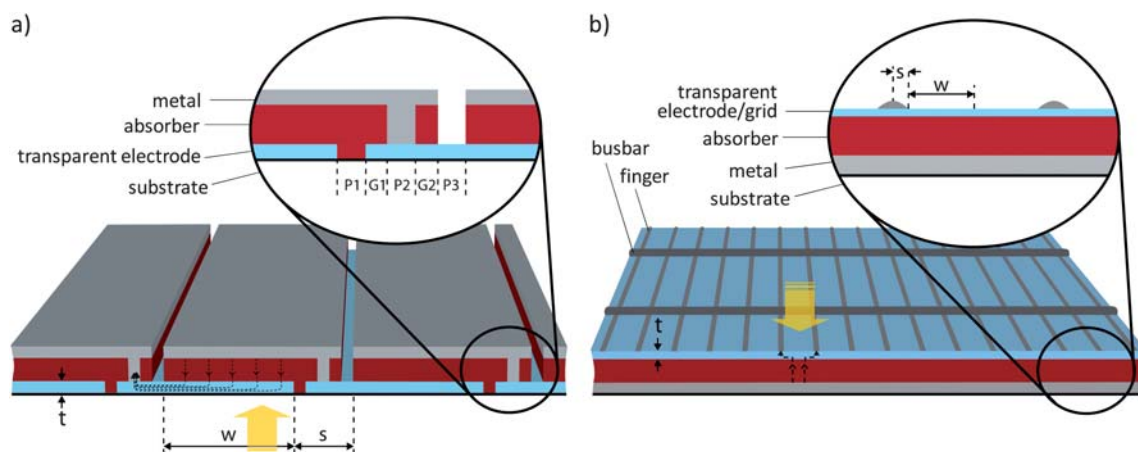
Monolithic integration is advantageous in that it eliminates the need to handle and assemble individual cells and thereby reduces manufacturing costs. A drawback, however, is that parasitic losses associated with the TC layer are more significant for monolithic modules—typically 15–25%.[1] For standard modules employing large cells covered with a metal grid reinforced TC, losses are typically 10–15%. For both architectures, typically high quality sputtered transparent conducting oxides (TCO),[2] such as indium tin oxide (ITO) or doped zinc oxide (ZnO), are used owing to their high conductivity and low absorptivity. Several new systems being investigated for use as the TC, including carbon nanotubes,[3–7] graphene,[8–10] nanowires[11,12] and metal thin films,[13] have the potential for both reductions in cost and gains in performance relative to TCOs.

Here, we calculate the total losses due to the limitations of the TC for a solar cell that has a nominal ("lab scale") efficiency of 10%. For monolithically integrated thin-film modules, we show that a TC performance of at least 90% transmission, T, with a sheet resistance (R_{sh}) less than 10 Ω/sq is important. While higher TC performance will result in meaningful efficiency gains, lower TC performance will have a precipitous effect on efficiency. For standard modules employing a metal grid reinforced TC over large area cells, losses are much lower and improvements in TC performance will only result in marginal gains in efficiency. Alternative lower cost TC materials may already be sufficient to replace TCOs in this geometry.

Fig. 1 shows a cross section of both monolithically integrated thin film cells and a standard thin film cell employing a metal grid/TC as the transparent electrode. In monolithic modules, typically each cell is ~1 cm wide and runs the length of the module. A module that is ~1 m wide will then have on the order of 100 cells connected in series. The interconnect region, often referred to as "dead space", does not

Broader context

High power conversion efficiency and the use of abundant materials are critical to the adoption of photovoltaic power at scale. The transparent conductor (TC) layer is a necessary component of all thin film solar cells and it has a significant impact on efficiency, resulting in a 10–25% power loss even for the best TCs. In the last several years there has been renewed interest in this area with the development of several new transparent and conductive oxides and nanostructured materials, many with the potential for both cost and performance advantages. For the development or adoption of any new TC material, it is useful to know the impact on efficiency and the necessary TC performance requirements. Here, we compare the two different ways of manufacturing thin film solar cells and quantify the transparent electrode related losses for a TC material of any performance and we specify the material figure of merit necessary for a TC material to be a compelling candidate for photovoltaic applications.

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Fig. 1 a) Cross section of a monolithically integrated thin film module. Only the active area of width w contributes to the power generation and the interconnect area of width s is lost area. Photogenerated current, denoted by the dashed lines, is injected into the transparent electrode and then driven laterally to one edge of the device where contact to the back metal electrode of the adjacent device is made. b) Cross section of a standard cell using metal grid/TC. Area under the grid lines is lost area and photogenerated current between the lines is conducted laterally over a short distance by the TC film.

contribute to the photocurrent and so the width of this region is kept as small as possible. The dead space width, labeled s in Fig. 1, cannot be infinitely narrow, however, due to both limitations in scribing technology and requirements for good isolation and a low resistance series connection between adjacent cells.[14] In the commercialized thin film market, which is dominated by CdTe, CIGS and amorphous Si, the scribing is typically performed with laser processing,[15] though mechanical scribing has also been demonstrated in the case of CdTe and CIGS where the semiconducting layer is only weakly adhered.[16] Scribe widths, labeled P1–3 in Fig. 1, can be as narrow as 25 μm, but 50–150 μm is typical. Similarly, the gap between scribe lines, labeled G1–2, can be very narrow but limited accuracy in registry between scribe lines means gaps are typically 50–150 μm.[17–19,20] With these restrictions, s can be 140–1000 μm and is typically 500 μm. In the case of solution processed TCs and active layers, such as organic semiconductors, it may be advantageous to eliminate the scribe processing steps and rely on printing to define the interconnect region. In this case, the limitations on s will likely be different.

Standard modules are made of individual cells stacked adjacent to one another and serially connected in a long string. The cells are typically on the order of 6 inches square and the front electrode consists of both a TC layer and a metal grid deposited with a low cost technique such as screen printing or inkjet printing of a metal paste that is then sintered. The grid normally consists of fine parallel lines (fingers) crossed by two thicker bus bars that collect current from the fingers and then make a serial connection to the adjacent cell. Ideally the grid lines are narrow and tall such that shadow losses are minimized and the line resistance is low. Typically the finger lines cannot be economically deposited at a width less than 130 μm and the busbar lines are ~2 mm wide.[21]

For either module architecture, there is an optimum film thickness and device width, w, or finger spacing, $2w$, that minimizes the net losses from the scribe or shadow area, the TC absorption and the TC sheet resistance. Calculating the fraction of power lost due to the scribe area and the TC absorption is straightforward. Accurately estimating the power loss due to the sheet resistance is more difficult. For small power losses, i.e. in the limit where the voltage variation in the transparent electrode is so small that the current injection across

the device can be considered uniform, the fraction of power lost due to the TC sheet resistance can be reasonably predicted by estimating the Joule heating losses in the TC layer, P_{load}, relative to the nominal output power of the cell,[5] P_0:

$$\frac{\Delta \eta}{\eta_0} = \frac{P_{load}}{P_0} = \frac{\frac{1}{3} w^3 L j_{mpp}(t, R)^2 R_{sh}}{w L j_{mpp}(t, R) V_{mpp}} = \frac{w^2 j_{mpp}(t, R)}{3 \sigma t V_{mpp}} \quad (1)$$

where $\Delta \eta / \eta_0$ is the fractional loss in efficiency, j_{mpp} is the current density at the maximum power point, V_{mpp} is the voltage at the maximum power point, L and w are the active area length and width of the cell, respectively, σ is the TC conductivity, t is the TC thickness and R is reflection. At larger power losses this equation is not
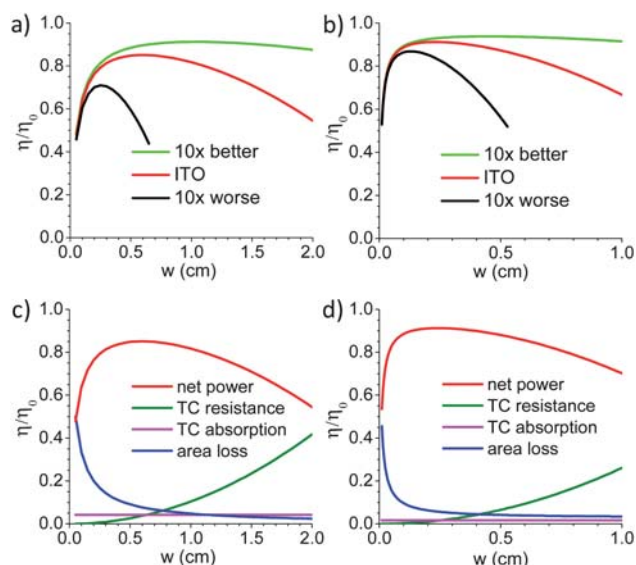
Fig. 2 Fraction of nominal efficiency for three materials as a function of width, w, for monolithic (a) and standard (b) modules. For ITO, the fraction of nominal efficiency is re-plotted along with the three contributing losses due to TC sheet resistance, TC absorption and scribe area for monolithic (c) or shadow area for standard (d) modules.

expected to be valid. This equation assumes that current injection across the width of the cell is constant. Realistically, with increasing width or sheet resistance across the cell, j_{mpp} will decrease and the power output of the solar cell will decrease. Koishiyev, et al.[22] used a distributed diode model that showed the validity of this scaling up to losses of ~30%. They determined an empirical relation differing from eqn (1) by the substitution of $0.38 \times j_{sc}/V_{oc}$ for $(1/3) \times j_{mpp}/V_{mpp}$. Using this empirical factor, the cumulative effect of these losses can then be described by eqn (2),

$$\frac{\eta}{\eta_0} = \left(1 - \frac{s}{w+s}\right)(1-R)(1-A(t))\left(1 - \frac{0.38w^2 j_{sc}(t,R)}{\sigma t V_{oc}}\right) \quad (2)$$

where absorption, A, is modeled using Beer's law.[23] In this work we neglect reflection losses and set R to 0 because reflection varies greatly with device architecture and can usually be reduced to a few percent or less using antireflection coatings or texturing. Additionally, for solar cells where the active layer thickness is less than the absorption length and the wavelength of light, optical interference is critical and this simplification is not valid.[24]

Fig. 2a shows the fraction of the nominal efficiency, η/η_0, for monolithically integrated panels plotted as a function of w for ITO[25] and two hypothetical materials that are 10 times better or 10 times worse (as defined by the σ/α figure of merit for TCs[26,27] discussed below). For all of these plots the dead space, s, is fixed at 500 μm and an optimum thickness, t, has been found for each material. Typical values for j_{sc}, V_{oc} and the fill factor, FF, (20 mA cm^{-2}, 0.71 V and 0.71, respectively) have been chosen such that the nominal ("lab cell") efficiency is 10%. These plots show the trade-off between increasing the fraction of active area *versus* lowering the resistive losses in the TC. For ITO, the optimum film thickness is 195 nm and the optimal device width ($w + s$) is approximately 0.7 cm. Even at this optimum condition the efficiency is only 84% of the nominal efficiency. For the common device structure using glass–ITO there is an additional 2–3% reflection loss at the glass–ITO interface[28] and additional reflection at the second ITO interface depending on the dielectric constant of the layer on top of the ITO. For the hypothetical material that is 10 times better, η/η_0 reaches 91% at a width of 1.1 cm. And for the material that is 10 times worse, η/η_0 reaches 71% at a width of 0.25 cm.

The loss in efficiency from a grid/TC for standard cells can similarly be calculated from eqn (1) under the assumption that the dominant series resistance contribution is due to the sheet resistance of the TC material between the fingers. Fig. 2 (b) shows the fraction of nominal efficiency for a finger width, $2s$, fixed at 130 μm and a busbar width of 2 mm and spacing of 8 cm.[21] For the materials shown in Fig. 1, the maximum fraction of nominal efficiency for the material 10 times better than ITO is 94% at an optimum TC film thickness and an optimum finger spacing ($2w$) of 9 mm. For ITO and a material 10 times worse, the maximum fraction of nominal efficiency is 91% and 87% at a finger spacing ($2w$) of 5 mm and 2.5 mm, respectively. For finger spacing much larger or finger width much smaller than the values given here, the resistive loss in the finger itself may be significant and adding busbars or controlling the aspect ratio of the grid lines will be critical.

The smaller efficiency loss for standard modules in comparison with the monolithically integrated configuration is an important factor in considering the advantages and disadvantages of these two different solar module manufacturing techniques. Significantly, the requirement for σ/α of the TC material for standard modules is less critical and so materials other than high performance TCOs may be compelling.
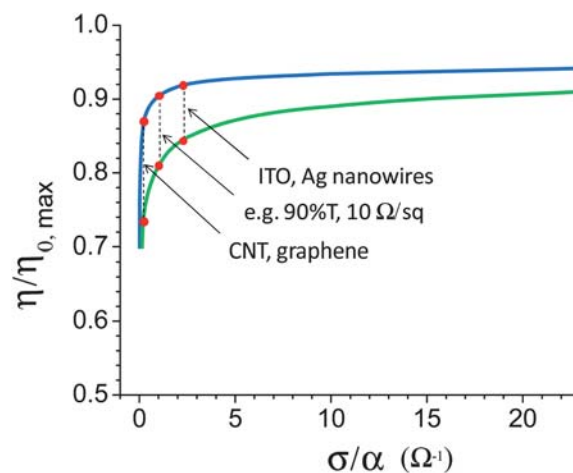
Fig. 3 Maximum fraction of nominal efficiency as a function of the TC material figure of merit for monolithic integration (lower green line) and for standard integration (upper blue line). For monolithic integrations, achieving high module efficiencies will require $\sigma/\alpha \geq 1$ Ω^{-1}, which corresponds to a performance equivalent to at least 90% T and 10 Ω/sq.

In Fig. 2 (c)–(d), the individual losses are plotted along with the net power for the same materials in Fig. 2 (a). At narrow widths the scribe loss becomes significant and at greater widths the resistive losses dominate. Comparing the three materials, the importance of the finite scribe width is apparent. If, for example, s could be reduced by half, this would nearly compensate for a 10 times change in the TC performance. It should also be noted that the resistance losses plotted here are for the specific solar cell parameters listed above, and from eqn (1) or (2), the resistance losses are seen to scale with j_{sc}/V_{oc}. For ITO, doubling the current to 40 mA cm^{-2}, for example, will increase the total losses to ~20%. For multijunction solar cells with lower current and higher voltage, however, losses will be lower.

For TC materials, the most direct figure of merit for ranking the performance of a TC is σ/α, given by eqn (3),

$$\frac{\sigma}{\alpha} = \frac{1/R_{sh}t}{\frac{-\ln(1-A)}{t}} \approx \frac{G_{sh}}{A} \quad (3)$$

where σ is the DC conductivity and α is the absorptivity (absorption coefficient). Importantly, this figure of merit does not depend on device architecture or film thickness and can be easily determined from R_{sh} and A. This ratio can be put in context by realizing that for very thin films σ/α is approximately G_{sh}/A, where G_{sh} is the sheet conductance and A is the absorption.

While σ/α describes the performance of a TC material and can be used to rank the potential of different materials, the relationship between σ/α and η/η_0 is non-linear. Fig. 3, shows the maximum η/η_0 (optimized w and t) as a function of σ/α for the same limits on s used in Fig. 2 for both monolithic and standard integration. As σ/α drops below a value of ~1 (equivalent to ~90% T and 10 Ω/sq), the efficiency drops off rapidly. For σ/α much greater than 2, the efficiency continues to increase but less rapidly. For monolithically integrated solar modules, it is clear that for any TC material to be compelling as the transparent electrode, σ/α must be high enough to achieve at least 90% T and 10 Ω/sq ($\sigma/\alpha \geq 1$ Ω^{-1}). For standard cells, the optimum TC film thickness is much less and so that the impact of the TC

material is reduced. Even for materials as much as 10 times worse than TCOs, the loss in efficiency will be less than 15%, which may be an acceptable trade-off for alternative materials with cost or other benefits.

Figure of merit values as high as 7 Ω^{-1} have been reported for TCOs,[26] but this is predicted to be near the upper limit for TCOs.[29] Recently much effort has been directed towards the use of nano-structured materials for transparent electrodes.[30]

Materials such as carbon nanotubes and graphene have shown promise but performance to date has been much lower than TCOs due to high intertube[31] or intersheet resistances which greatly reduce the film mobility. The individual tubes or sheets have much higher electron mobility than TCOs, however, and so the upper limit for their performance may be significantly higher.[9,10,32]

In the last few years, films made of Ag nanowires[11] or printed microgrids[33] have achieved performance comparable to TCOs and the upper limit for these systems would seem to be much higher.[11] In these systems, relying on nanostructures enables one to shrink the open space between the wires to the point where very little or no TC material is required in the open space. Often, a window layer such as CdS or conductive polymer is sufficiently conductive and the network acts as a homogeneous conductor. With further developments in this area, cutting the losses due to the TC by as much as 40% for monolithic modules and 30% for standard modules would seem to be within reach.

Acknowledgements

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