

Introduction

GPS receivers can be grouped into two categories: First, the traditional heterodyning receiver architecture, where the RF signal is downconverted to an IF frequency through mixing before the A/D conversion takes places. The second group of receivers sample the RF signal directly, often at sampling frequencies that have the same order of magnitude that the GPS signal frequency. GPS receivers based on subsampling, that is sampling at a considerably lower frequency with respect to the frequency of interest, to our knowledge have never been implemented in a single RF CMOS IC but only explored as off-chip architectures [5]. One reason for this is the difficulty to achieve a sufficiently narrow and well controlled bandpass filters in RF CMOS [2]. It has been recently demonstrated [4], that such an architecture – a 900 MHz receiver example – is indeed possible to implement on single chip.

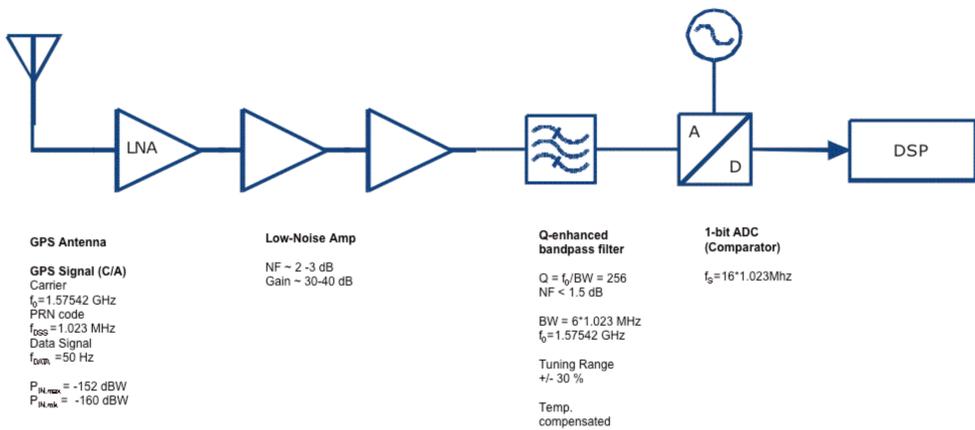
GPS receivers based on subsampling will have two very important advantages over heterodyning and direct RF sampling receivers:

- 1.) The power consumption can be substantially reduced since the subsampling process renders the PLL and the LO obsolete
- 2.) Multiple RF frequencies can be captured and processed at the same time, making this architecture suited for GNSS applications. This, however, requires some optimization of the sampling frequency[3]
- 3.) The simpler architecture will decrease the development time of the GPS receiver

GPS/GNSS Receiver Architecture

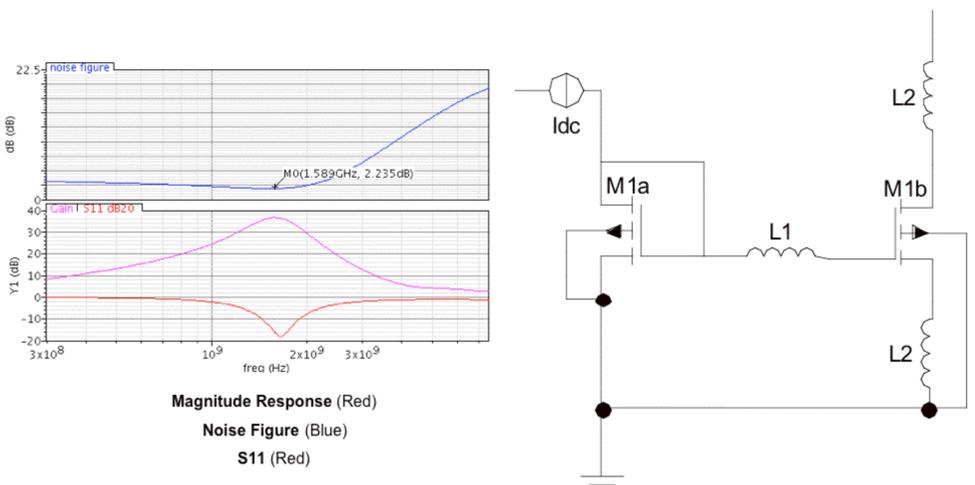
The proposed receiver architecture is shown below. The main components of the architecture are a Low-Noise Amplifier (LNA), a Q-Enhanced bandpass filter and a 1-bit Analog-to-Digital Converter (ADC). Several components such as the single – ended to differential conversion circuit have been omitted for clarity. The Digital Signal Processing Unit (DSP) is also shown for completeness but will not be considered further in this poster. The GPS / GNSS Receiver Architecture will be fabricated in a standard 250nm BiCMOS process from National Semiconductor. For better comparison with existing GPS receiver front-end architectures, bipolar transistors will not be used in the architecture.

After passing the GPS Antenna, the incoming RF signal is low – noise amplified, filtered and then quantized by the 1-bit ADC. The Low Noise Amplifier provides a 50Ω match at its input to avoid reflection. The proposed gain of the LNA is in the range 30 dB – 35 dB and its Noise Figure (NF) no more than 3 dB. The Q-enhanced bandpass filter provides a very narrowband passband response to filter out any unwanted noise that will alias into the passband through subsampling. To achieve such a narrowband response, very high Q-resonators will have to be implemented, which are typically not available in CMOS RF. Therefore, an active implementation based on negative resistance cancellation is sought. A high-speed, 1-Bit ADC completes the design serving as bridge between the analog and the digital part. The clock is applied to the chip by an external oscillator, allowing to vary the frequency between 0 – 250 MHz. Due to the possibility of independent tuning of the Q and the resonance frequency of the bandpass filter as well as the frequency of the external oscillator a variety of signals in the range $\sim 1 - 2$ GHz can be downconverted through aliasing and processed by the DSP. One key advantage of the subsampling GPS / GNSS receiver architecture compared to conventional heterodyne architectures is the simplicity of the circuit and the lower power consumption since the Phased Locked Loop becomes obsolete. Another key feature is the fact that multiple RF frequencies can be aliased into the passband allowing to monitor several GPS / GNSS signals at the same time by the DSP.



Low Noise Amplifier

The Low Noise Amplifier (LNA) sets the Noise Figure (NF) of the system if the gain of the LNA sufficiently high. The gain of the LNA plus the gain of the Q-Enhanced Bandpass filter need to be high enough so that noise introduced by the subsampling process remains below the thermal noise floor. According to [4], a subsampling frequency of 16×1.023 MHz and a sampling capacitance of 0.3pF of the sample and hold stage results in a Noise Figure (NF) greater than 40dB. Thus, the combined gain of the LNA and the Q-Enhanced Bandpass filter needs to be higher than 40dB so that it does not perturb the noise figure initially set by the LNA. The LNA was optimized using the design procedure outlined in [1] and noise figure of 2.3 dB could be achieved while consuming approximately 8mW of power. A g_m based current reference was implemented to control the g_m of the LNA with an external reference resistor [3]. This allows to set the g_m of the LNA relatively independent of temperature and process variations.

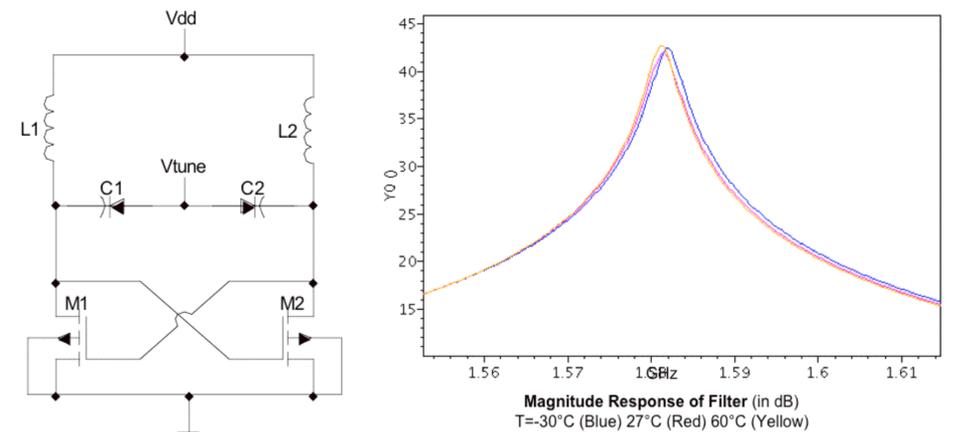


Q-Enhanced Bandpass Filter

The bandwidth of the filter has to be narrowband to filter out any unwanted noise, which would otherwise alias into the baseband and increase the noise figure of the system to undesired levels. A second requirement of the filter is robustness against process variations and mismatch. Last, the GPS receiver potentially will be operating in a harsh environment where it has to withstand the daily temperature variations. The last two requirements are difficult to overcome and a compensation circuit has to be implemented. To process different RF frequencies – such as the L1 and L5 GPS signal - the filter should have sufficient tuning range. Provided a summation circuit is added, several of such filters can process multiple RF frequencies in parallel.

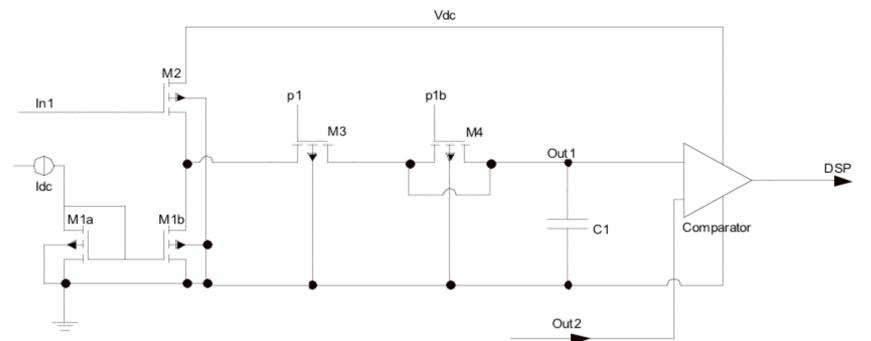
Given the low Q of the on-chip spiral inductor elements, achieving a narrowband filter in a standard CMOS RF process can be challenging. Several approaches are possible, including the use of Gm-C type filters and Q-Enhanced filters [6]. The filter which was chosen for this work is the simplest Q-Enhanced filter possible where the negative resistance of a cross-coupled transistor pair is used to enhance the Q of the spiral inductors. This filter topology has a couple of advantages over other filter types. First, the resonance frequency is actually set by two physical passive elements, namely the capacitance from a MOS varactor and the inductance of an on-chip spiral inductor. Due to the small temperature coefficient of MOS varactors, the resonance frequency of the filter can be set almost independently of temperature, which allows a very predictable tuning. In an uncompensated filter, temperature and process variations can change the center frequency of the filter by +/- 10 %. Second, with the Q of the resonant circuit completely dependent on the transconductance of the cross coupled pair, the temperature coefficient of Q is quite well known and a compensation circuit can be implemented. The compensation circuit is based on the g_m referenced current source that was described in the last subsection. Overall, we chose a filter topology that allows to decouple the tuning of the resonance frequency and the compensation of the Q.

The filter achieves a 3-dB frequency of 6×1.023 MHz, which with a sampling frequency of $f_s = 16 \times 1.023$ MHz will result in a NF < 1dB for the noise folding process of the subsampling mixer, according to calculations in [4] and our own MATLAB simulations.



Sample and Hold Stage (1-Bit ADC)

The requirements on the sampling architecture are twofold. First, the sample and hold stage has to be operational at high speeds. Even though the sampling frequency is orders of magnitude smaller than the GPS signal frequency, the incoming RF signal still needs to be tracked with sufficient precision. Second, distortion from second order effects such as charge injection and clock feedthrough needs to be mitigated to avoid any unwanted spurs. In case of GPS, the constraints on distortion are rather undemanding. However, to achieve the required tracking speed, commonly used architectures such as bottom plate sampling topologies prove to be insufficient. Instead, the most basic – and therefore fastest – architecture consisting of a simple switch and capacitor has been employed. A second switch M4 was inserted between the capacitor and the sampling switch M3. The clock of M4 is inverse to the clock of M3, allowing to cancel the charge that is injected by the sampling switch M4 [7].



Conclusions

We have proposed a GPS/GNSS subsampling based single chip receiver in RF CMOS technology that consumes substantially less power than a conventional heterodyning architectures. The chip allows to process multiple RF frequencies without introducing PLL circuitry as it is conventionally done in GPS receiver IC's. The GPS receiver will have a noise figure of less than 4dB, comparable with products currently on the market.

References

- [1] Shaeffer, D.K., et al. "A 1.5-V, 1.5-GHz CMOS low noise amplifier". *IEEE Journal of Solid States Circuits*, vol. 32, no. 5, pp. 745-759, May 1997.
- [2] Lee, T. "The Design of CMOS Radio-Frequency Integrated Circuits". Cambridge University Press, Second Edition, 2004.
- [3] Psiaki, M., et al. "Design and Practical Implementation of Multifrequency RF Front Ends Using Direct RF Sampling". *IEEE Transactions on Circuits and Systems*, vol. 53, no. 10, pp. 3082-3089, Oct. 2005.
- [4] DeVries, C., et al. "Subsampling Architecture for Low Power Receivers". *IEEE Transactions on Circuits and Systems*, vol. 55, no. 4, pp. 304-308, April 2008.
- [5] Thor, J., et al. "A direct RF sampling multifrequency GPS receiver". *IEEE Position Location and Navigation Symposium*, pp. 44-51, April 2002.
- [6] Li, D., et al. "Design Techniques for Automatically Tuned Integrated Gigahertz-Range Active LC Filters". *IEEE Journal of Solid States Circuits*, vol. 37, no. 8, pp. 745-759, August 2002.
- [7] Choi, M., et al. "A 6-b 1.3-Gsample/s A/D converter in 0.35µm CMOS". *IEEE J. of Solid-State Circuits*, pp. 1847-858, Dec. 2001.