PNT at DARPA and Stanford

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Markus Lutz*, Aaron Partridge*,
Gary Yama, Rob Candler[5], Bosch RTC
Amy Duwel, Mat Varghese, Draper Labs
Richard Nguyen, SPAWAR Amit Lal, DARPA MTO
Current Addresses : *SiTime, [1]UC Berkeley, [2]NetLogic, [3]DARPA, [4]Intel, [5]UCLA

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SiTime It's about time

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DRAPER LABORATORY

SPAWAR Systems Center San Diego

DARPA MTO

DARPA MTO "MEMS Portfolio": >25 Programs

Navigation

Basic R&D

Computation

Power

Manufacturing

Aerospace

Thermal

SERS S&T Fundamentals

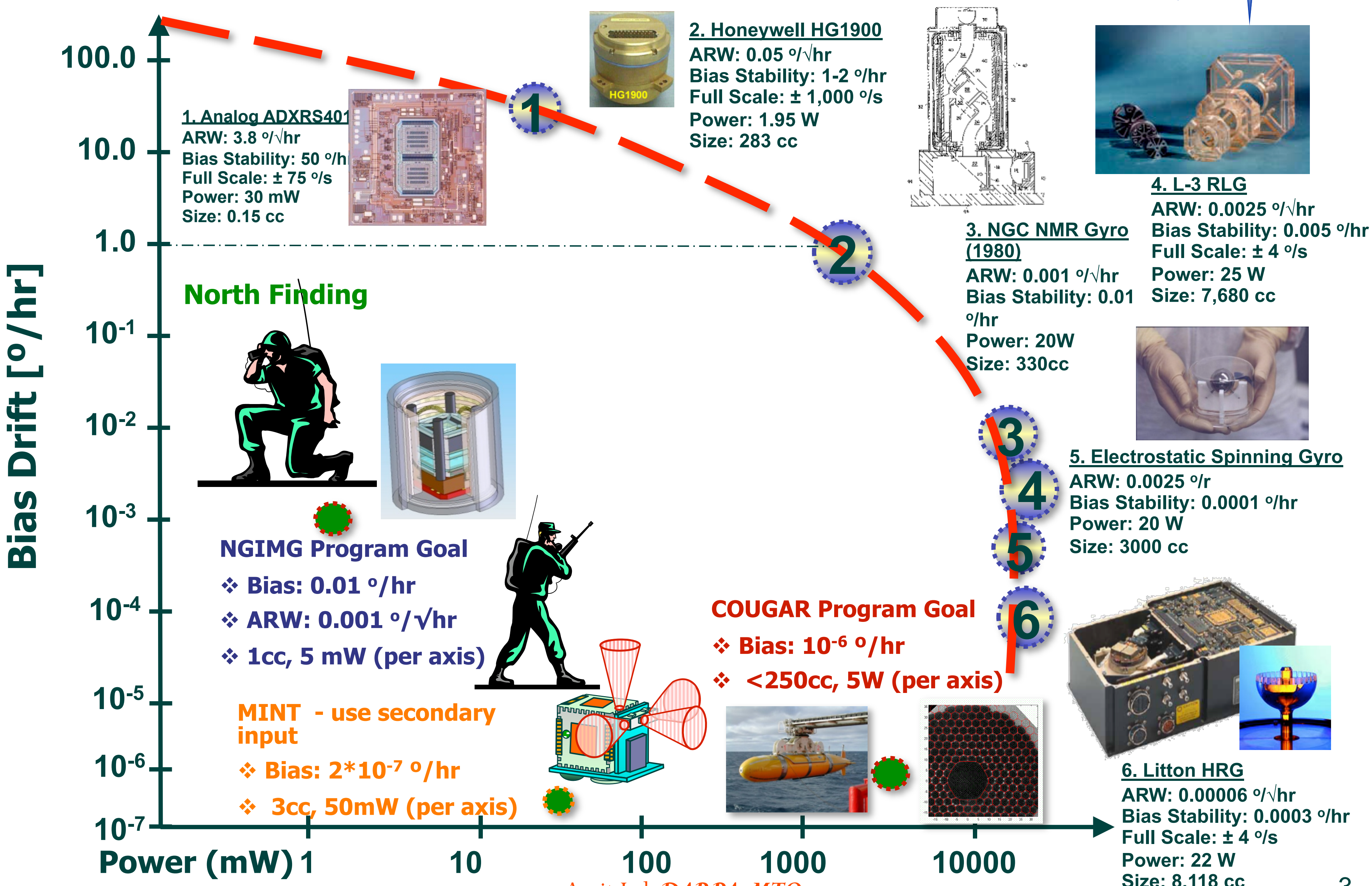
Sensing + Communication

Chip-Scale Vacuum μPump

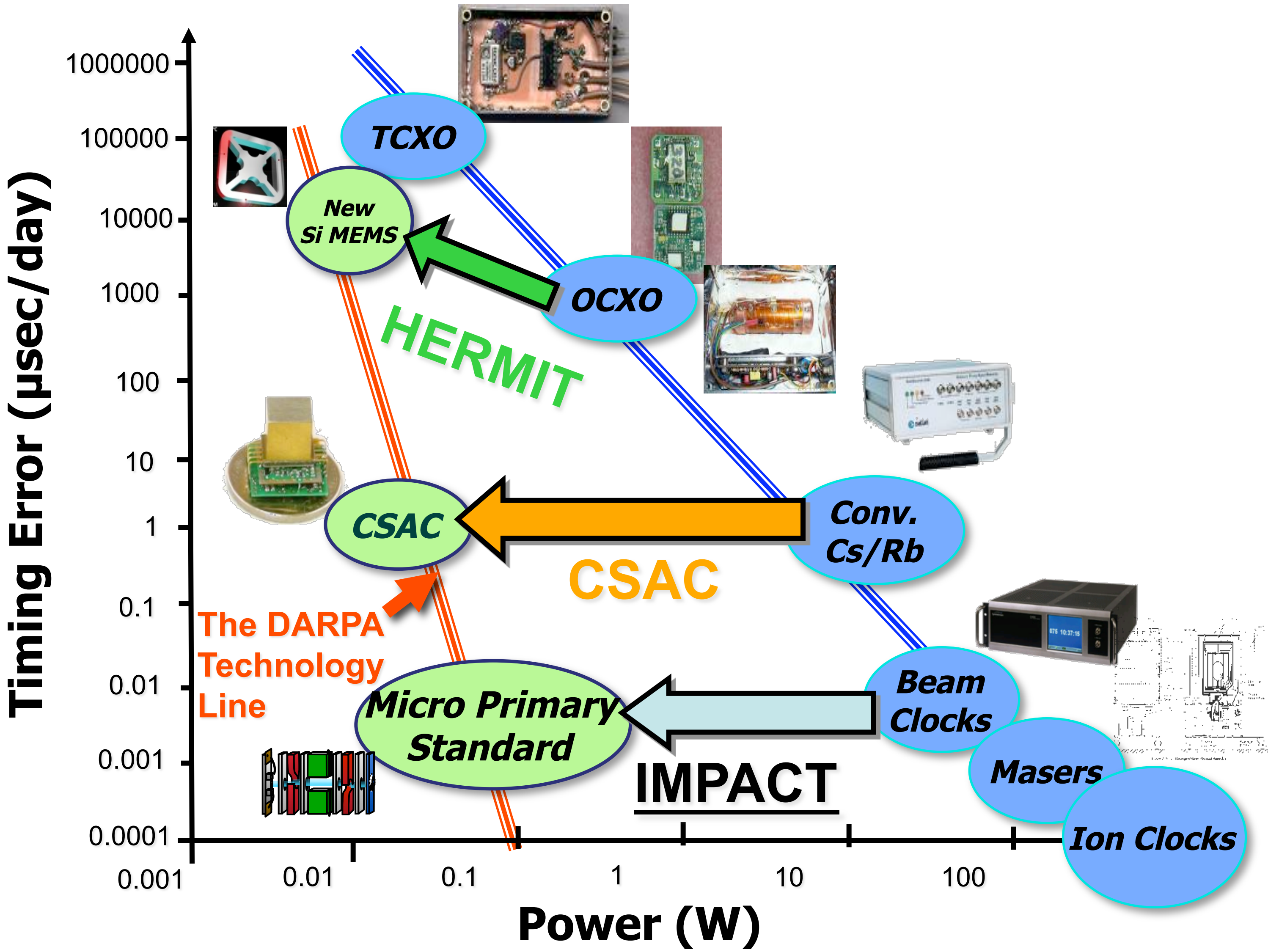
MGA

Chip-Scale Spectrum Analyzers

The Navigation Vision



The Timing Vision



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The Decider

The DARPA Director

Precision Navigation and Timing?

Tony Tether Agreed to hear about ideas for Atomic Clocks, Miniature IMUs, and alternative approaches to Navigation and timing.

Navigation and Timing budgeted at about $50M/year

Looking for Insertions into DoD

New Director : Dr. Regina Dugan

- » CEO, RedXDefense
  - – Xpak Portable Explosives Detection System
- » Co-Founder, Dugan Ventures
- » DARPA DSO PM
  - – Programs including “Dog Nose”

- » PhD, Mechanical Engineering, Caltech
  - – Co-authored textbook on Engineering Thermodynamics
  - – Very unusual background at DARPA
  - – May lead to shift in program emphasis, agency processes

MEMS

What are the barriers to MEMS Insertion?

- **cost and development time**
  - MEMS is slower, more expensive, and harder to scale than VLSI
- **reliability**
  - this is more art than science in MEMS
- **lack of standard processes, universal foundries**
  - MEMS is a very big collection of diverse tools and materials
- **marginal or poor performance**
  - drift in inertial sensors and resonators, selectivity in chem sensors

MEMS/Packaging

Is Packaging a barrier to MEMS Insertion?

- cost and development time
  - packaging adds a lot of cost and time to MEMS products.
- reliability
  - packages can improve reliability.
- lack of standard processes, universal foundries
  - all MEMS devices require custom packages – nothing is standard
- marginal or poor performance
  - better packaging can allow device optimization for performance.

MEMS Packaging Example : Bosch

Most common option is to develop a wafer-scale post-process bonded package.

This approach is widely used in industry, but suffers from significant disadvantages.

- Lost Die space
- Yield
- Temperature budget
- Cost

Device <20% of Die,

Bond Ring is 60% of Die

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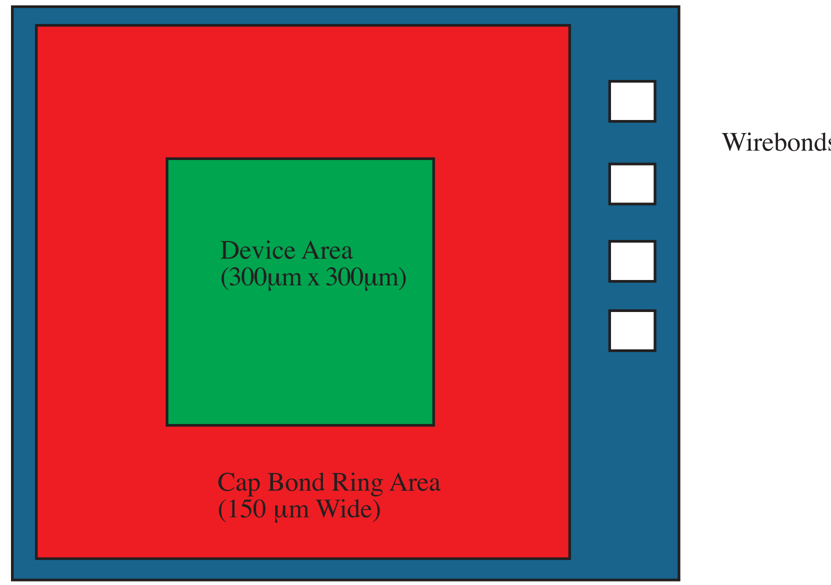

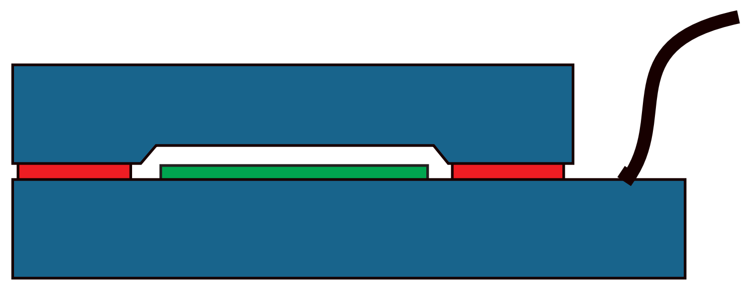

Example numbers Adapted from Bosch Accelerometer

MEMS Packaging Example : Bosch

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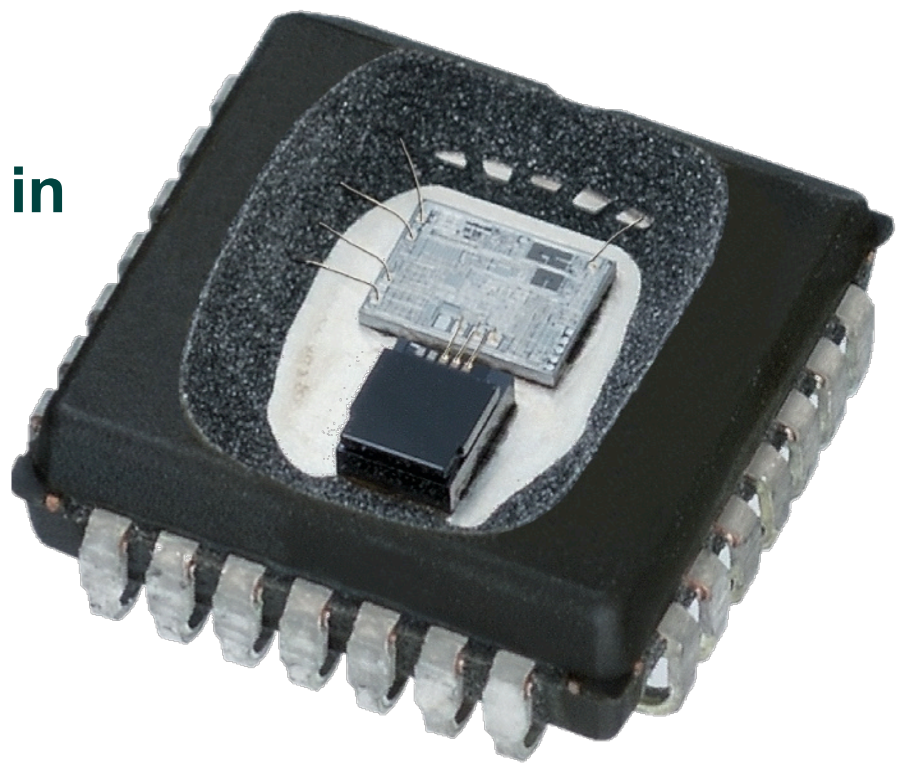

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Example numbers Adapted from Bosch Accelerometer

Integrate?

MEMS First requires packaging to protect MEMS from CMOS Process

- high temperatures, planar litho -> severe restrictions on MEMS
- no commercial examples

CMOS First also places restrictions on MEMS

- No High-Temp steps in MEMS Process
- Passivation of CMOS necessary for protection during MEMS

MEMS+CMOS merged process is most complicated

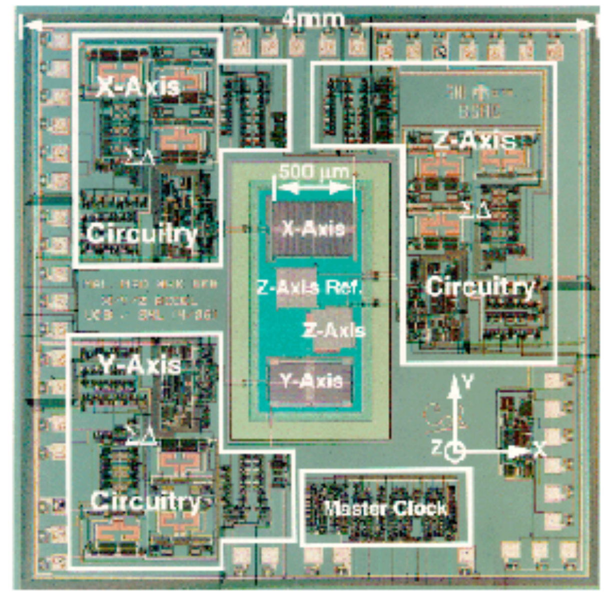
- All materials and steps must be compatible with both technologies

Separate-Chip ("2-chip") Processes are most common

- Eliminates process compatibility issues,
- Known Good Die can be used to eliminate mutliplicative yield issues
- Many commercialization examples

Integration Product Examples

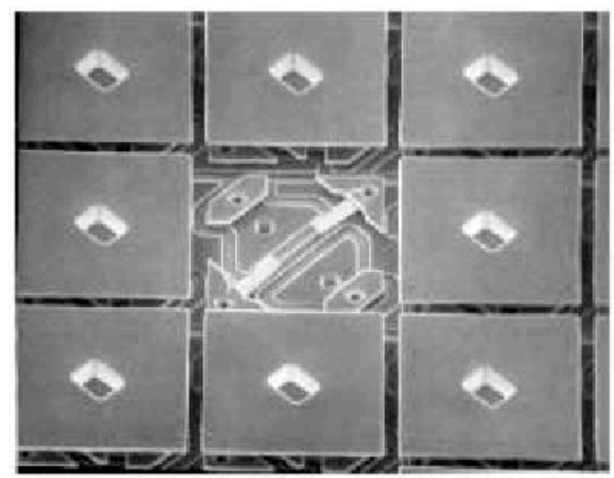
ADI iMEMS and TI DMD are examples of integrated MEMS products presently on the market



ADI iMEMS merged MEMS+CMOS

polysilicon optimized for stress and CMOS – very complicated

TI DMD has "MEMS Last"



low-temperature MEMS structure built on CMOS. MEMS Materials optimization complicated

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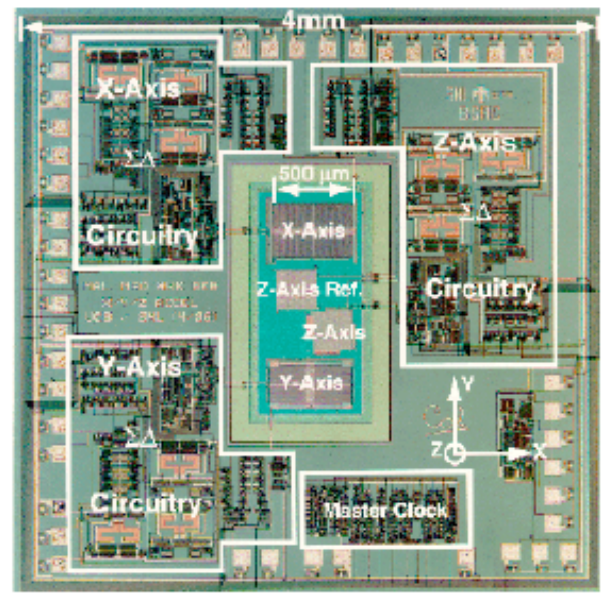

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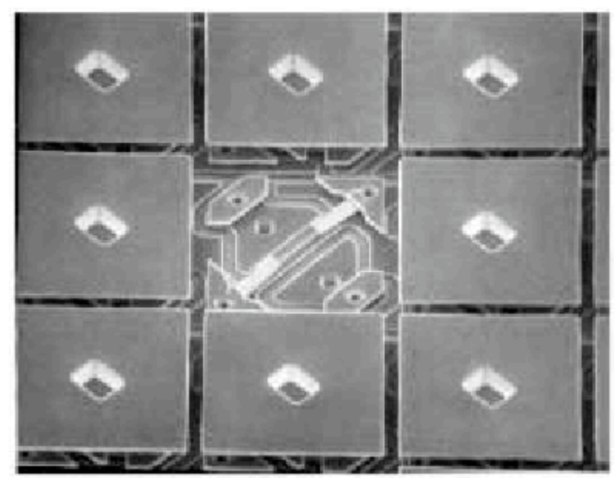

low-temperature MEMS structure built on CMOS. MEMS Materials optimization complicated

Both took >>10 years, and Many $!!

Packaging is a Problem for MEMS

In most MEMS processes:

Design and Process are optimized to improve device performance.

Die Separation is a traumatic event.

Custom processes for packaging are developed after the MEMS devices have shown interesting performance.

"90% of the cost of a MEMS device is in the package"
Kurt Petersen, many others

There is no "fun" (funding, publications, fame/fortune) in packaging research

MEMS is a Packaging Technology

Our Focus:

Turn the "problem" into an opportunity

Also, this is a way to make research on packaging seem more "glamorous", which helps for funding, recruiting, and publishing

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Micro Structures & Sensors Lab

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MEMS is a Packaging Technology

We propose:

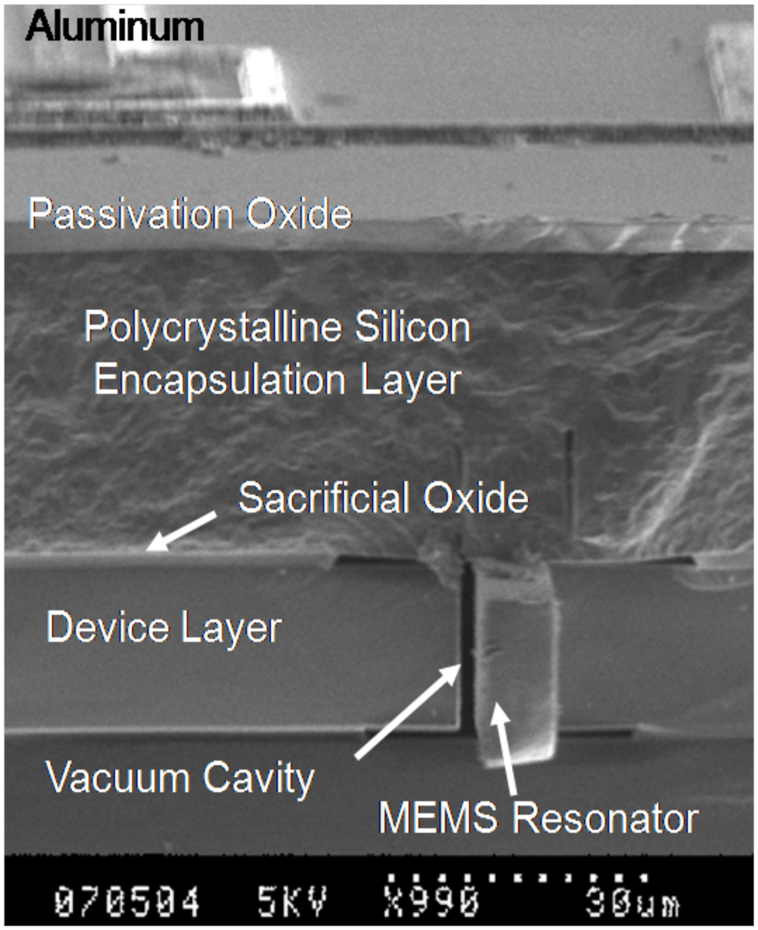
Fabricate Device and Package Together.

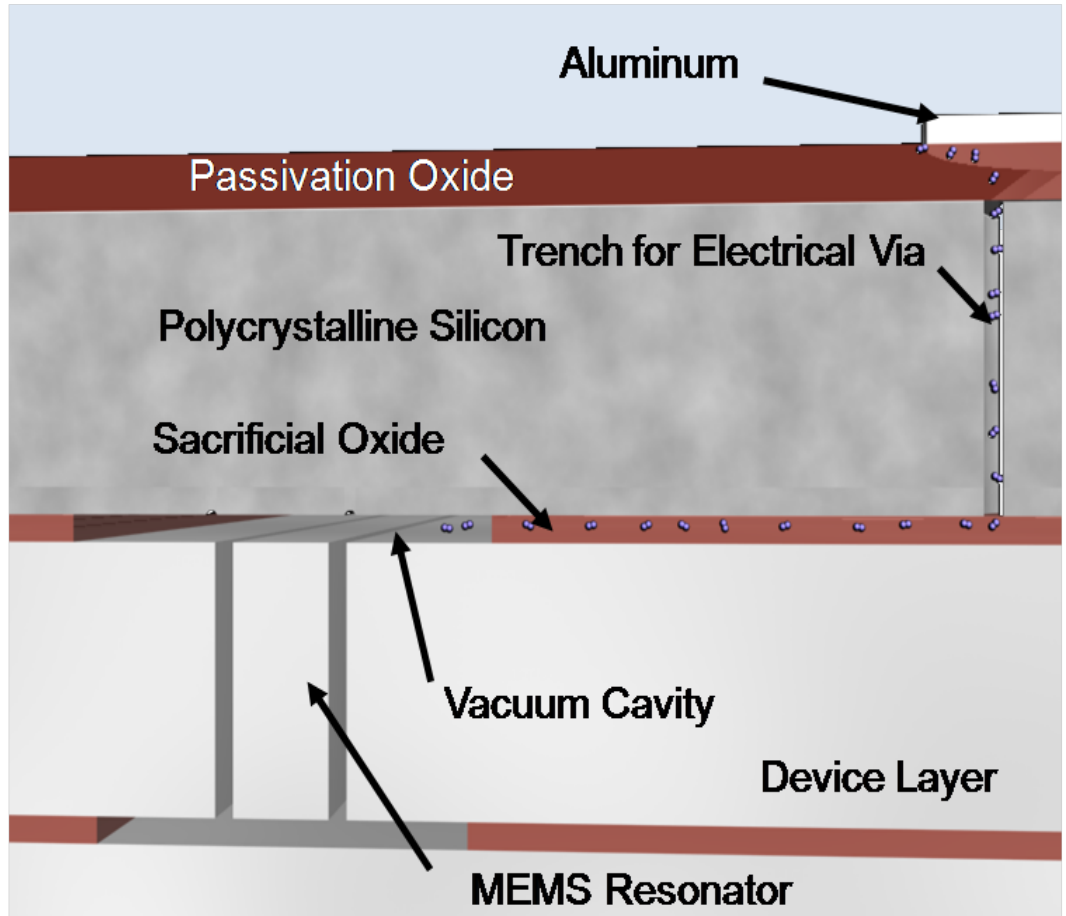
Compromise Required : Constraints on devices

Opportunity Gained : Good packages can improve devices

Simplicity : Packaged MEMS can be handled, inserted, sold

'Epi-seal' Wafer-scale Encapsulation

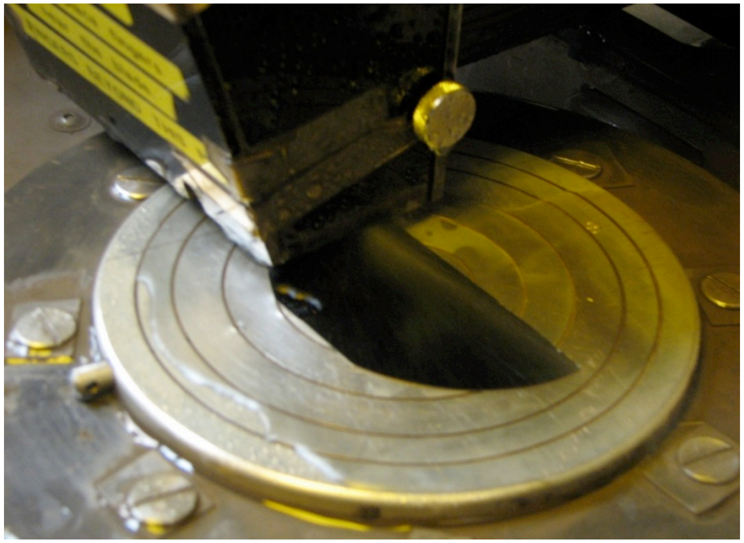


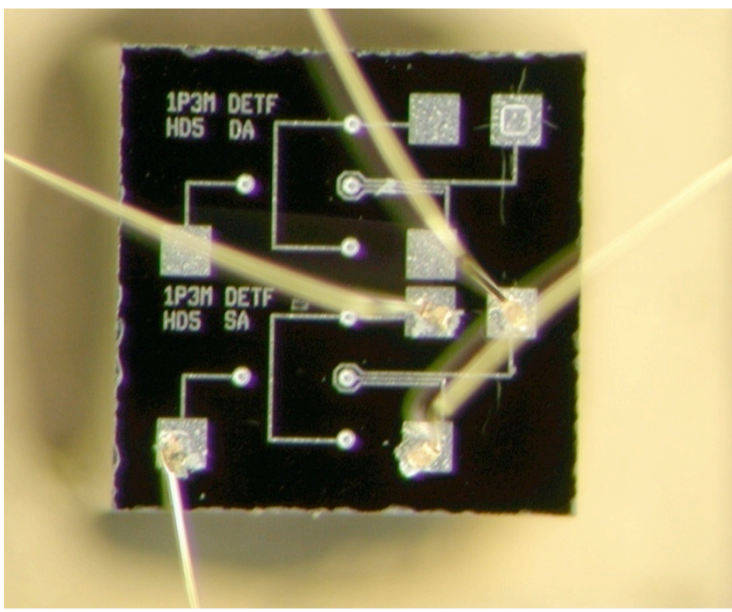


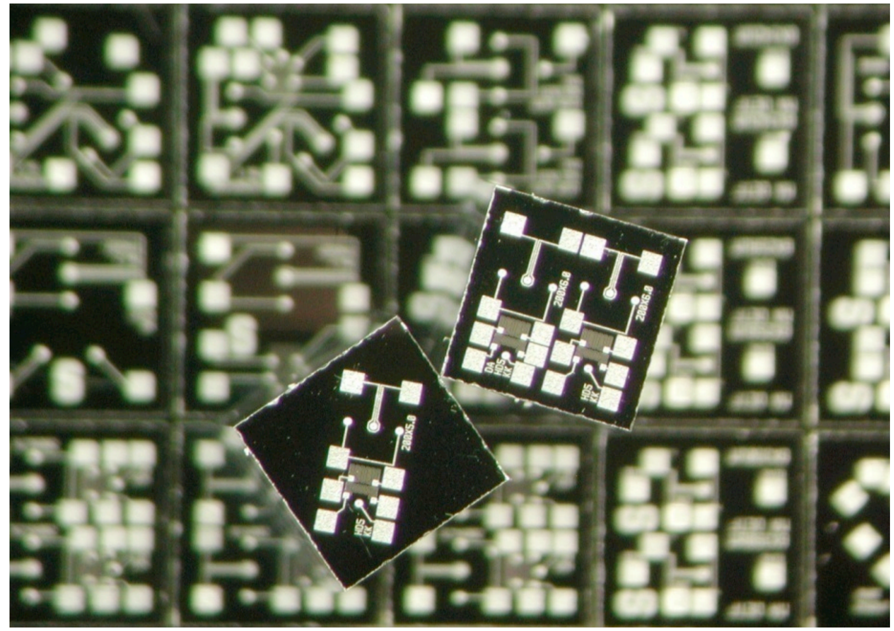
- Polycrystalline silicon thin-film Encapsulation
- Final sealing occurs at ~1000°C in CMOS clean environment
- Provides secure and stable operating conditions for MEMS devices

R. N. Candler et al., IEEE JMEMS, 2006

Robust, High Yield, Mass Producible Packaging







- No loss in production yield during harsh post-processes including wafer dicing, wire-bonding, glueing, and etc.
- Optimized space utilization results in extremely dense manufacture.
- Over 3,000 with higher than 90% production yield (among measured devices) could be achieved.

Wafer-Scale Package

Encapsulation Features

Small Footprint

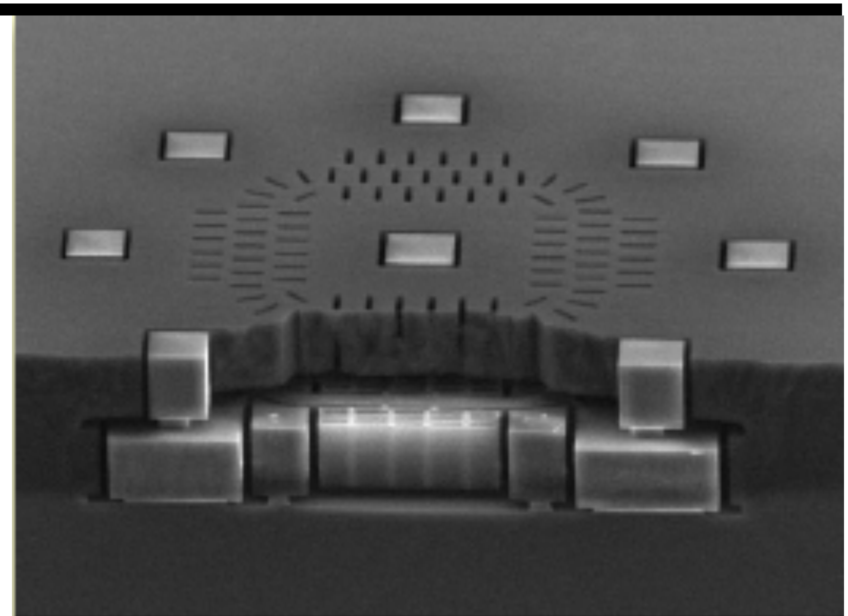
- Many Die/Wafer ($)

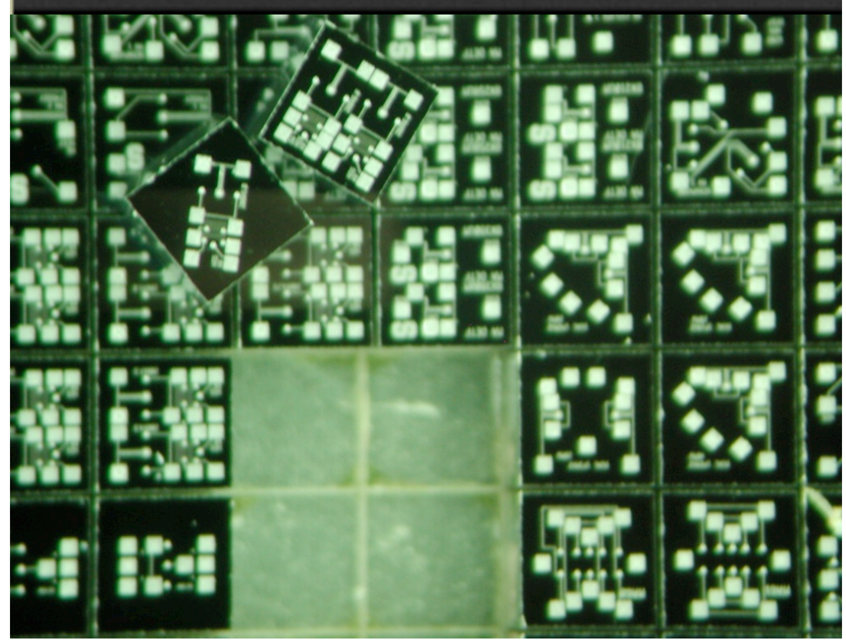
High-Temperature Seal (1000C)

- Ultra Clean Process
- No Getter Required ($)
- CMOS Compatible

Compatible with Standard Electronics Packaging

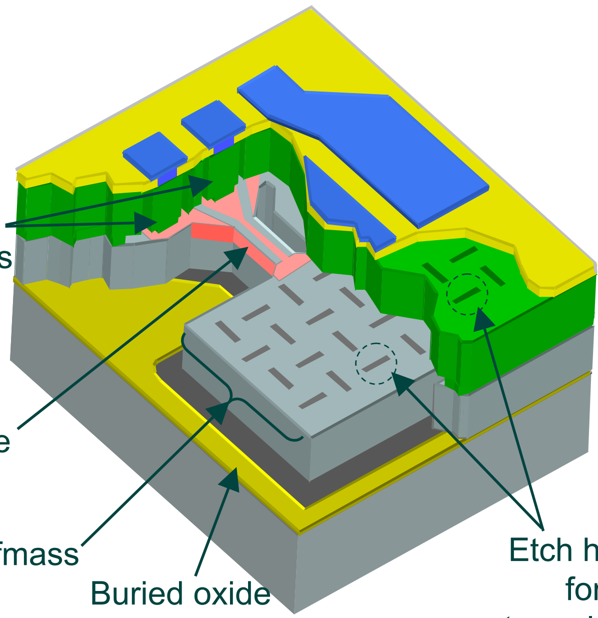
- No custom packaging ($)
- Injection-molded package possible ($)
- Allows use of existing packaging vendors ($)





UltraMiniature Accelerometer

- MEMS Process that builds device AND package in common process
- Allows extreme miniaturization and CMOS integration
- Accelerometers, Gyros, Resonators, RF Switches, all possible within this process.



WT Park, et.al., “Fully-Encapsulated sub-mm Accelerometers”, Proceedings MEMS ‘05, 347 (2005).

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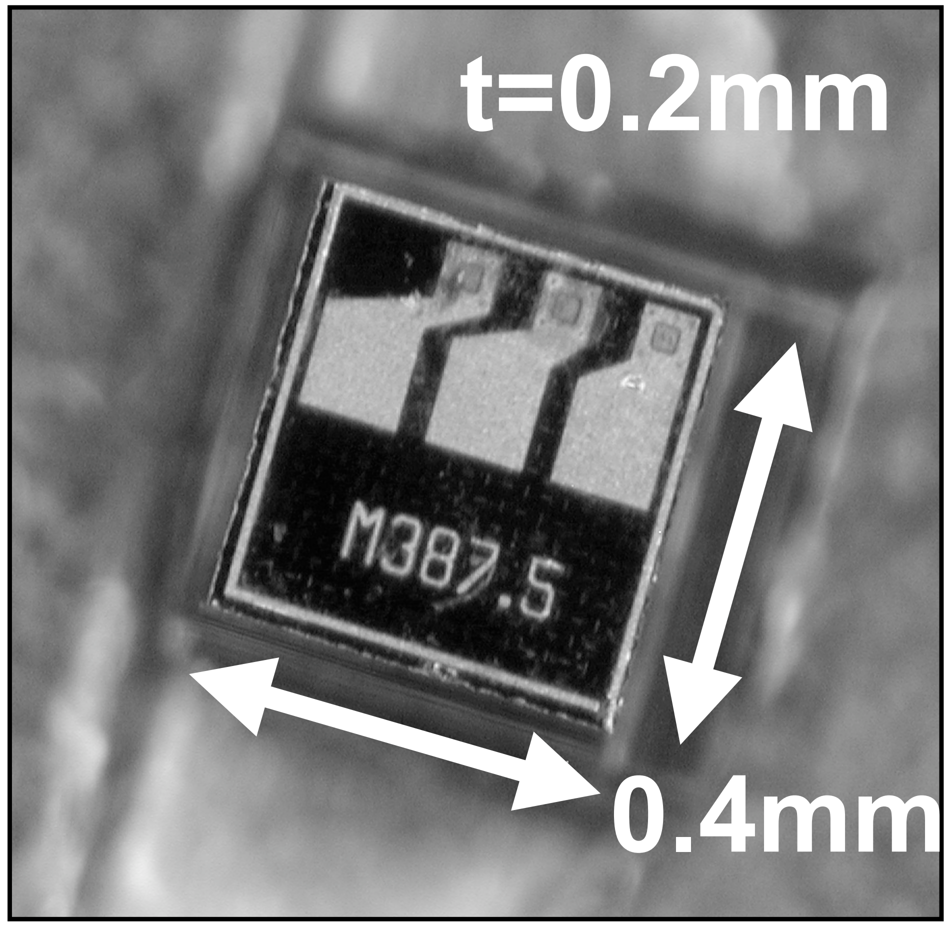


Package-enabled Opportunities

The Package+MEMS approach enables some novel applications for MEMS

UltraSmall Inertial Sensors for

- **Biomedical Applications**
- **Ultra-High Shock**
- **Navigation**

Resonators for replacement of Quartz references

- **watches, USB, CellPhones, PDAs**
- **Microprocessors, all CMOS devices**

Resonators

Opportunity :

- High Q, tunable frequency, good range, nice properties
- Low Cost
- Potential for integration with IC for “Single-Chip systems”

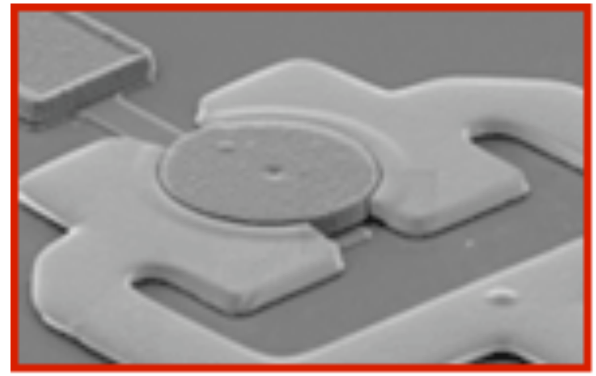
Barriers :

- MEMS resonators MUST be packaged
- Random Frequency Drift, Aging
- Silicon has a high temperature coefficient of modulus - frequency drift more than 10x worse than quartz resonators
- Co-Fabrication with CMOS not demonstrated.
- Lifetime, Reliability not understood.

Excellent Challenge for MEMS Encapsulation!

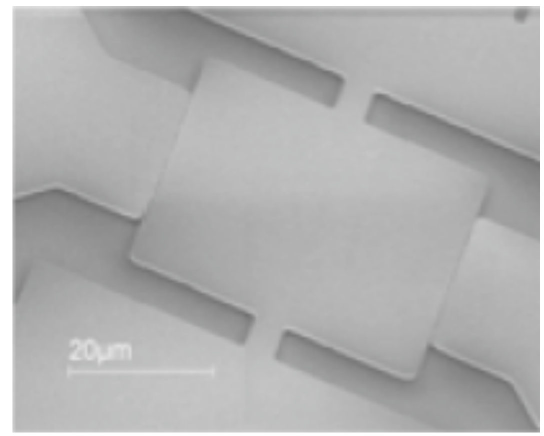
MEMS Resonator Commercialization Examples

First MEMS Resonator published in 1977



Discera (2000 -?) 2-chip products only

- MEMS Released + low-temp bonded package with getter.

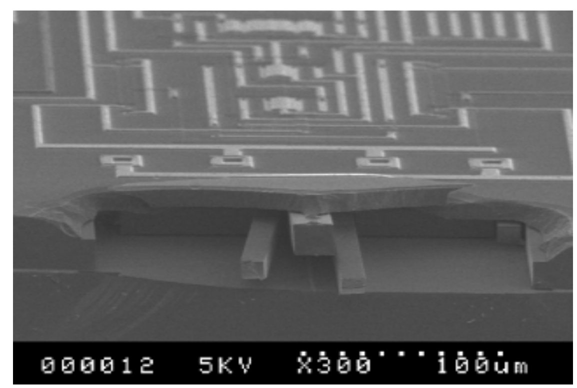


Silicon Clocks (2004-?) MEMS after CMOS

- SiGe resonator deposition at low-temp.
- MEMS Released + low-temp bonded package with getter

SiTime (2004-?) MEMS Before CMOS?

- MEMS formed and sealed "inChip"
- High-Temp package w/o getter
- All early products are 2-chip devices



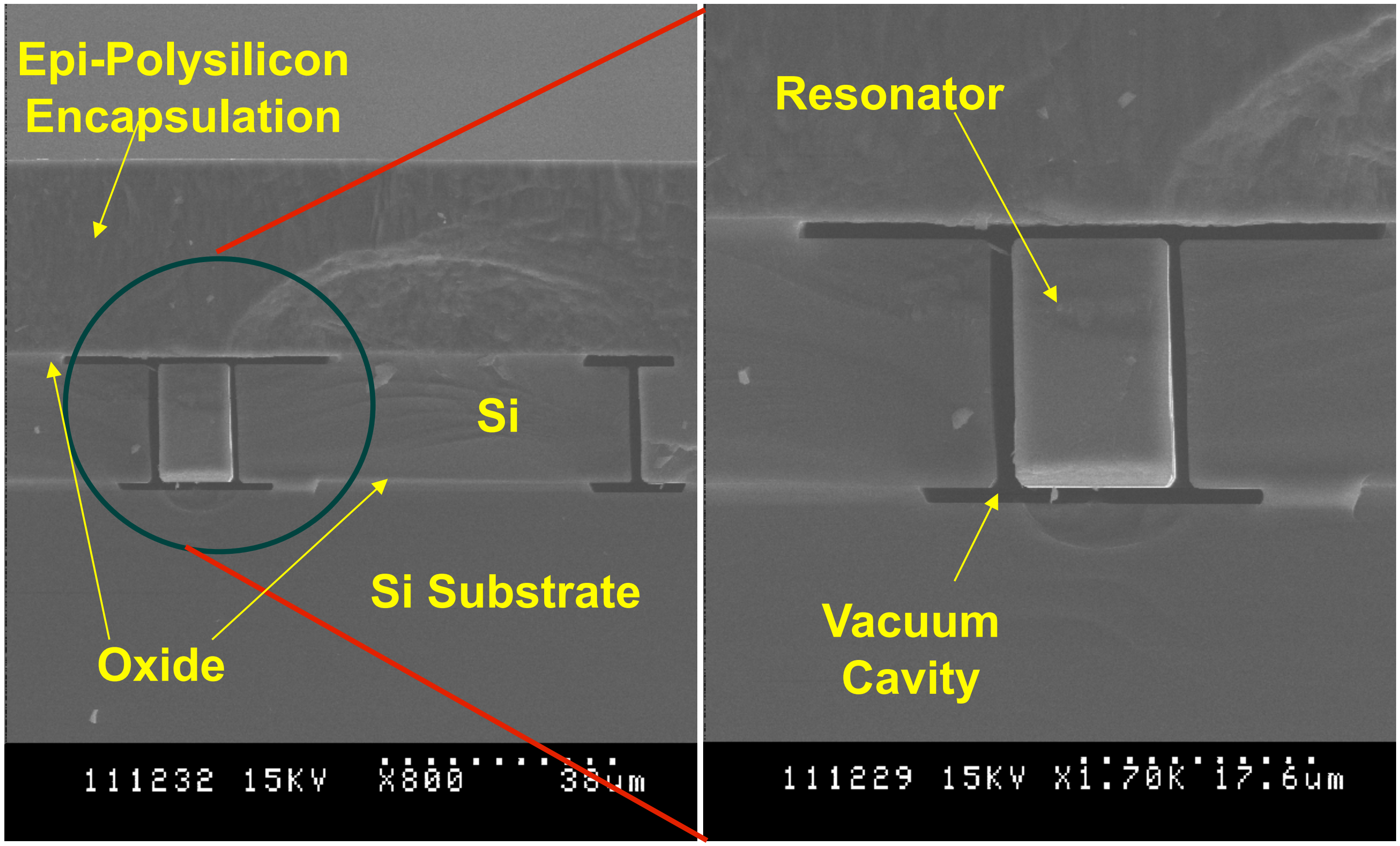
Discera micro communication technologies.

SILICON CLOCKS

SiTime It's about time

Encapsulated MEMS Tuning Fork Resonators

MHz Tuning Fork Resonators

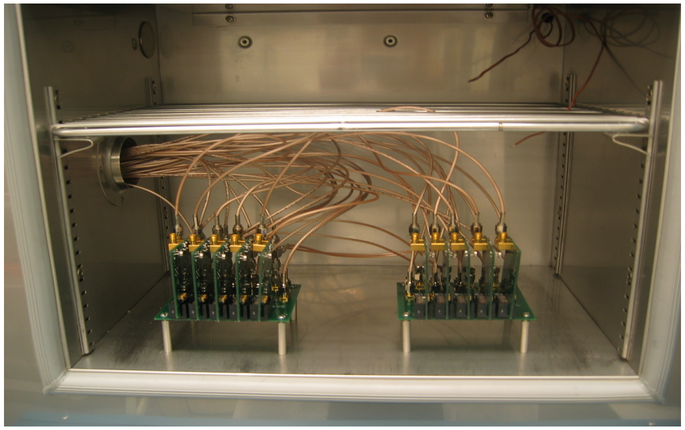


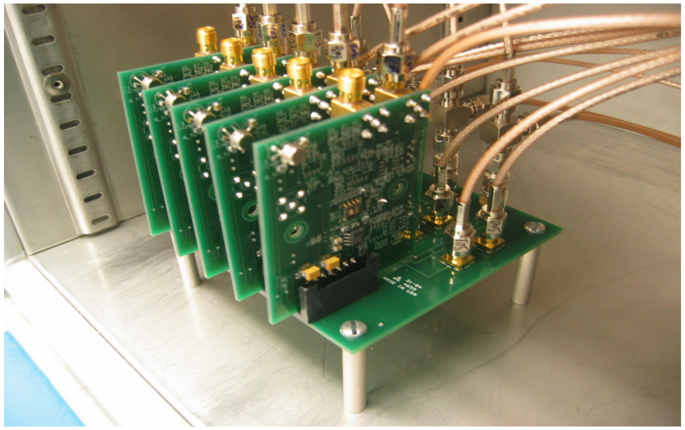
Sensitive to Pressure, Adsorbates, Stress -> Excellent Encapsulation Chamber Test Device!

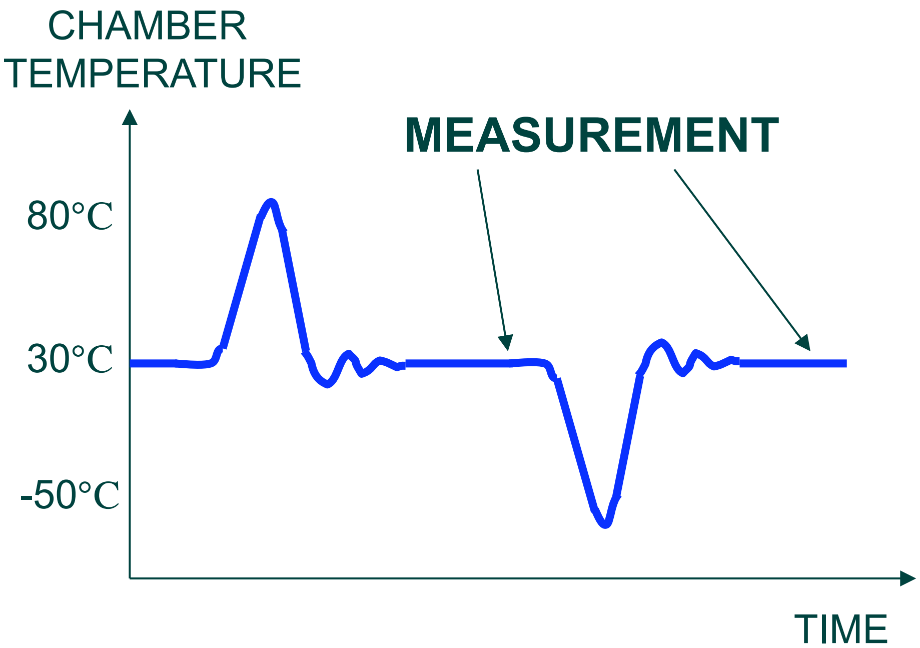
If we can make stable tuning forks in this process, optimally-designed resonators for various applications should be possible.

Issues to test : Hermiticity, Drift, Temperature Compensation Possibilities

Temperature Cycling Encapsulation Tests







-One temperature cycle ranges from +80°CC to -50°CC

- All measurements are performed after temperature is stabilized at 30±0.1°C. Full Cycle takes ~10 hours

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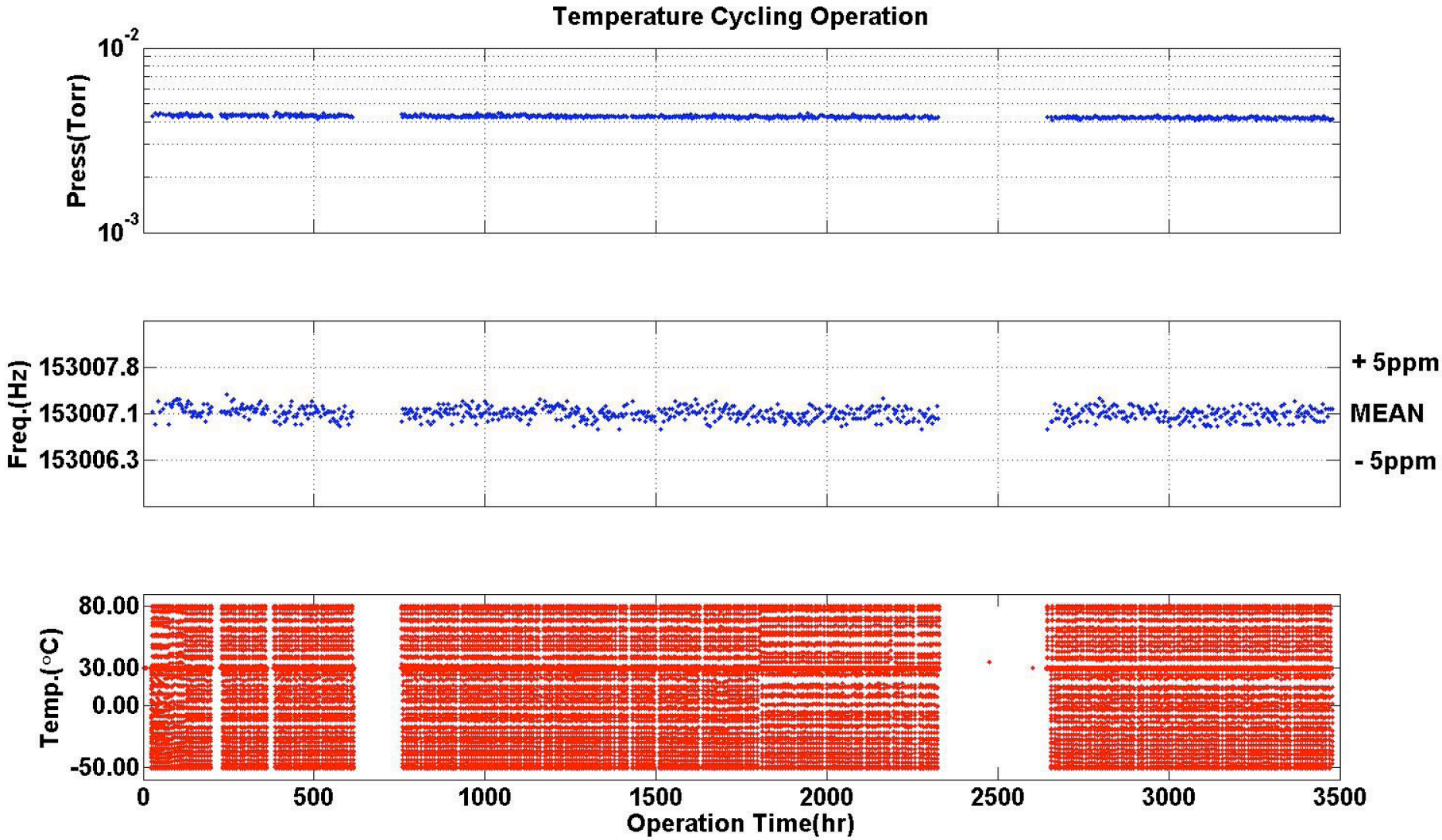
Bongsang Kim

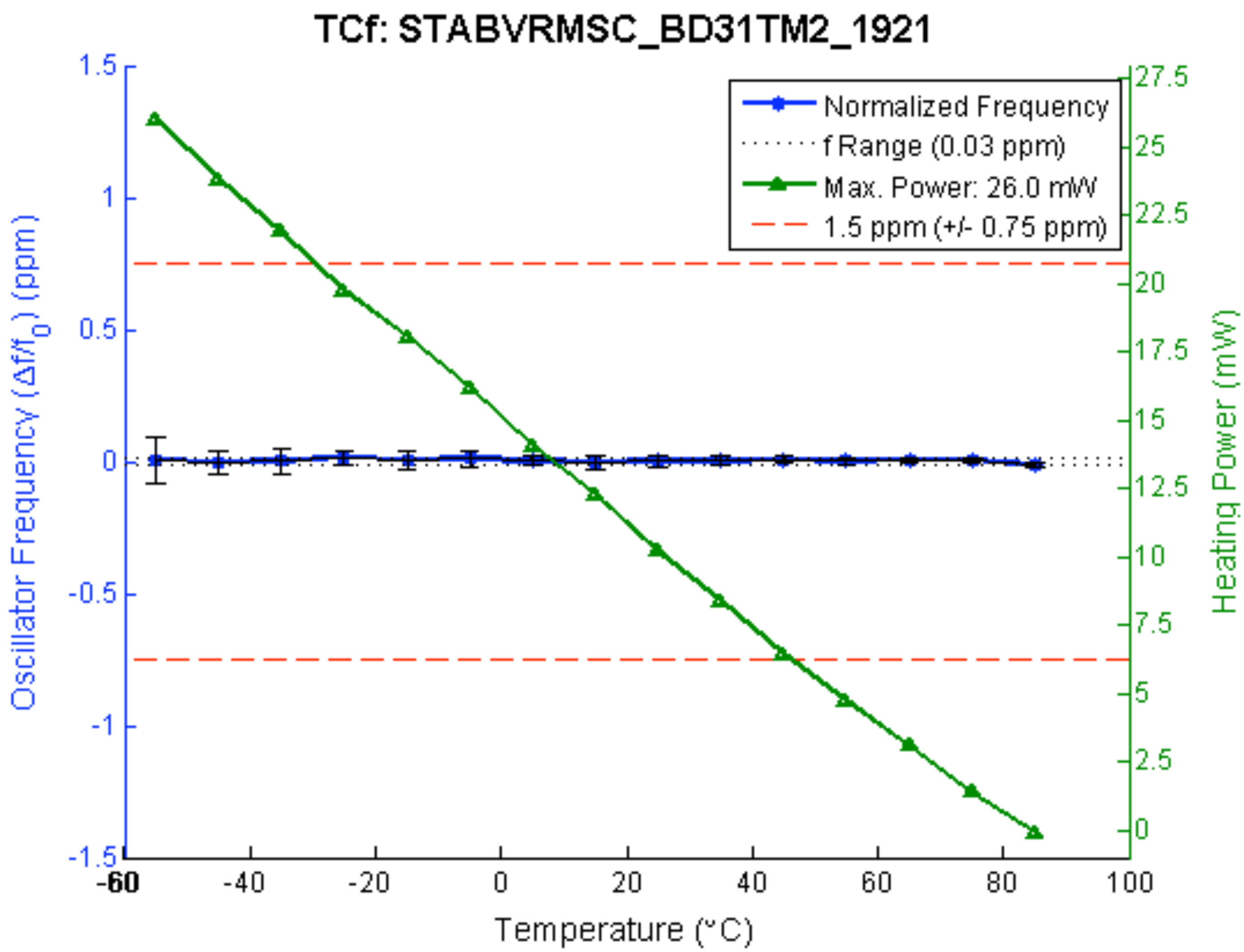
Long-Term Stability during Temperature Cycles from -50C to +80C



No Evidence for Leakage, Drift, Aging, or other fundamental barriers for MEMS references

Bongsang Kim

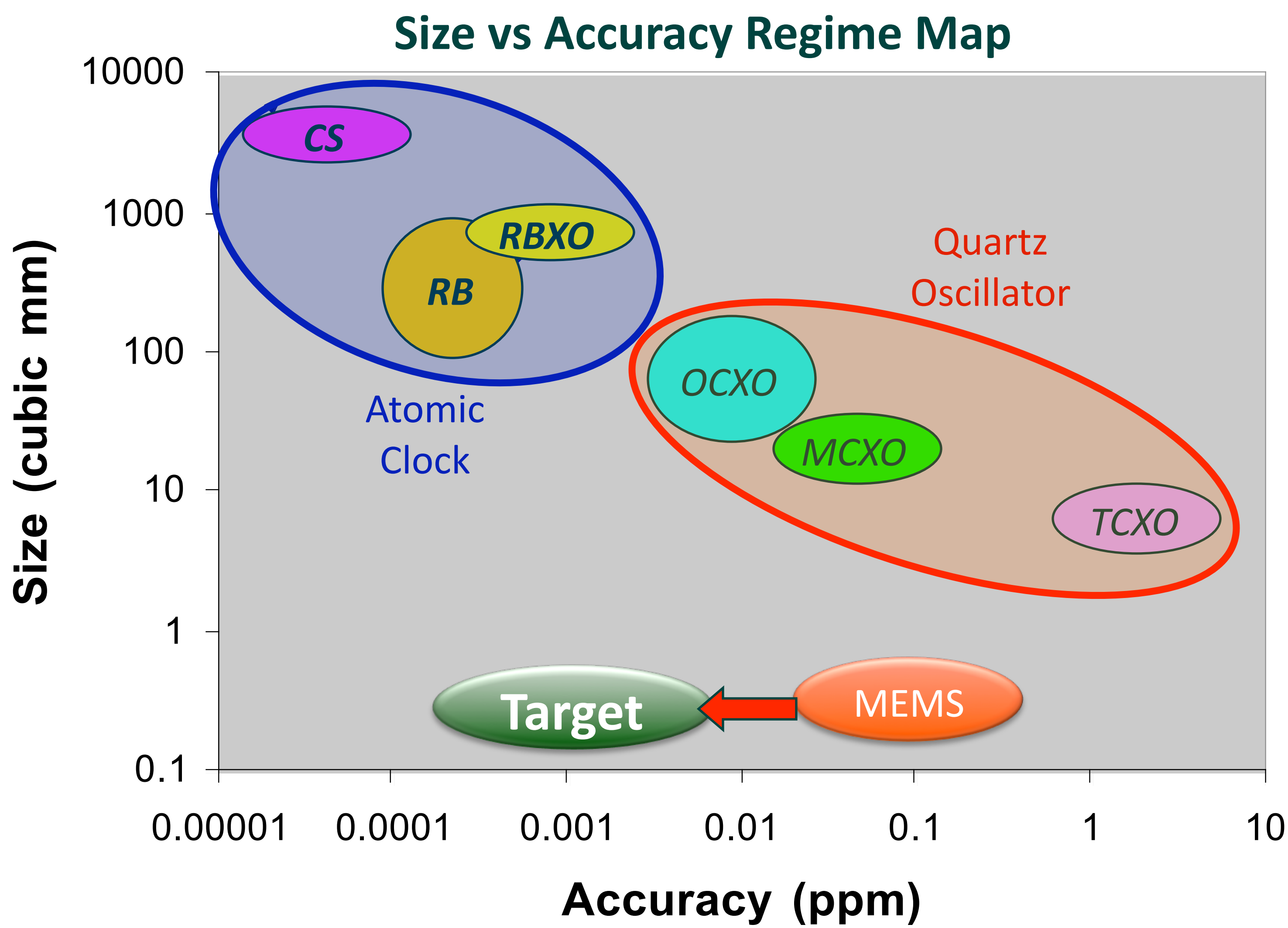
Measurement of Frequency over Temperature



Frequency variation: **0.03 ppm** / -55C to +85 °C

Matt Hopcroft

Various Frequency References



From Quartz Resonators Tutorial by John Vig

MEMS is a Packaging Technology

Advantages of Encapsulation with MEMS Process Steps:

Clean Hermetic Environment
Enhanced Stability in MEMS Resonators
Device Control Opportunities
High Yield MEMS Process
More Chips/Wafer
Smaller Die can enable some interesting applications
MEMS+CMOS Integration Enabled

Faster transition through development to manufacturing and markets?

SiTime:

disrupting the world of electronic timing

It's About Time

SiTime™

SiTime
It's about time

SiRes
MEMS Oscillator Family

Preliminary Datasheet for SiT1101 to SiT1273

Features

Standard Oscillator (resonator + drive circuit = oscillator) features

- 173 frequencies available from 1.000 MHz to 125.000 MHz
- Compare to quartz oscillators and resonators in industry standard footprints
- +/- 50 ppm, +/-100 ppm options
- 20 ps rms jitter, +/- 100 ps peak to peak jitter at 100 MHz
- Output enable

Experience MEMS Benefits as compared to competitive quartz products

- No load capacitors or shunt resistors required for operation
- Always in stock, MEMS resonators are manufacturing in 3 weeks in lot sizes of 1 million units vs. 12 weeks for quartz in lot sizes of 30K.
- Improved manufacturing performance with greater tolerance to shock, vibration, and thermal events to eliminate resonator cracking or permanent shifts in frequency.
- Ultra reliable start up
- Simplifies layout requirements with better immunity to interfering nearby PCB signals and requirement to be near clock destination.
- Better immunity to electro-static discharge

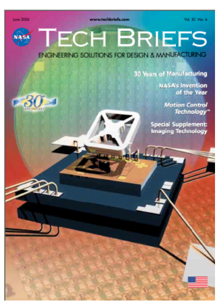
Packaging

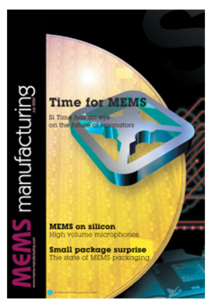
- +/- 2 ppm / year aging in packaging, +/-0.050 ppm / year aging in die form.
- Standard plastic QFN-type packaging
  - Lead free
  - 2.0 mm x 2.5 mm x 0.85 mm
  - 3.2 mm x 2.5 mm x 0.85 mm
  - 5.0 mm x 3.2 mm x 0.85 mm
- 1.8 V, 2.5 V or 3.3 V operation

Initial Frequency Tolerance	@25°C		+/-3	+/-10	ppm
Frequency Drift over temperature	SiT1xxxAx-xQN03 (0 to 70°C)		+/-20	+/-35	ppm
	SiT1xxxAx-xQN04 (-40 to 85°C)		+/-50	+/-90	ppm
Aging	1st year		+/-0.05	+/-2	ppm
Clock Output Duty Cycle		45	50	55	%
Clock Output Rise Time	10kohm II 10 pF Load, 0.8 V p-p min			2	ns
Clock Output Fall Time	10kohm II 10 pF Load, 0.8 V p-p min			2	ns
Cycle to Cycle Jitter	At 24 MHz		+/-200		ps
Cycle to Cycle Jitter	At 100 MHz		+/-100		ps
Start up time			TBD		ms

By end of September, SiTime has sold and shipped >10M resonators, and is shipping at >400,000/week.
Final round of financing completed - expecting break-even and ramp to profits early in 2010.

Encapsulation Already Commercialized!



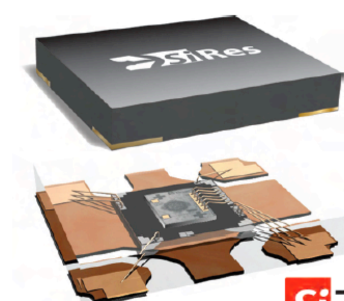


The 44th Anniversary R&D 100 Awards

EuroAsia IC Industry Awards 2006

Plastic Encapsulation

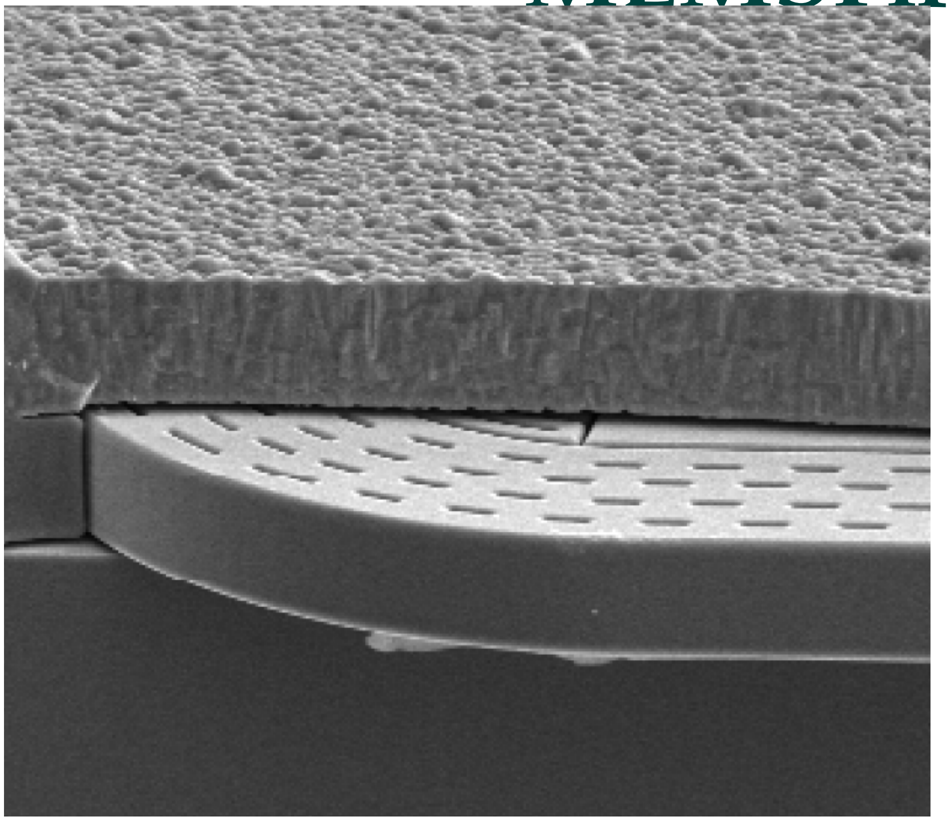
The MEMS First™ encapsulation process enables the use of any standard IC packaging including: SOIC, SSOP, BGA, CSP and QFN. SiTime chose QFN-type plastic transfer molded packaging for high reliability, low lead inductance, good thermal performance, flexible pad layout, and low cost. In comparison quartz crystals require expensive special purpose hermetic ceramic or metal vacuum encapsulated packages.

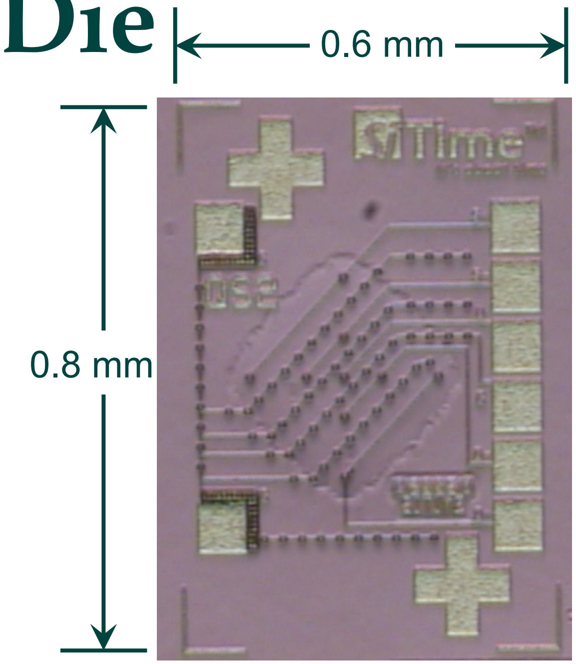


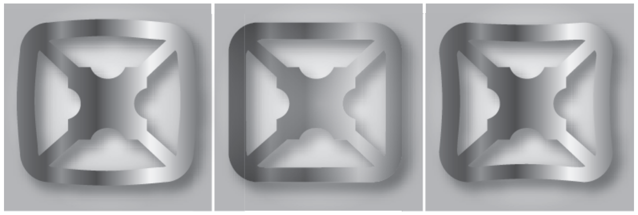
*Data gathered by T.W Kenny, B. Kim. Stanford University

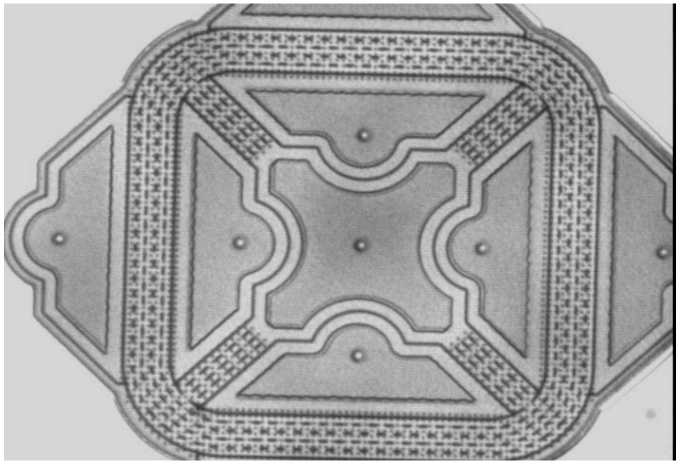
SiTime
It's about time

MEMSFirst Die



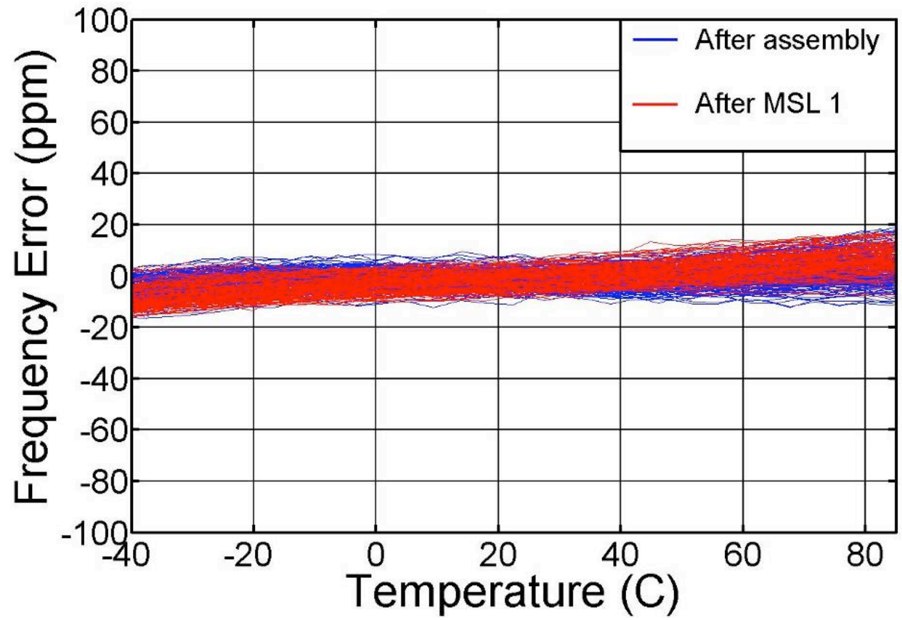






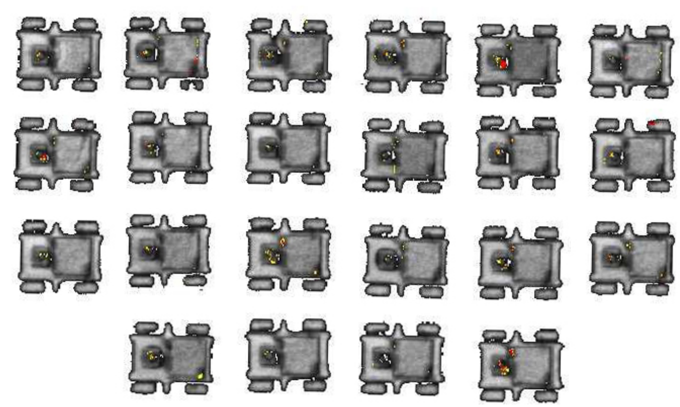
Characterization And Quality

- **20ppm frequency stability**
  - » Before and After MSL 1 Testing
  - » Parts Programmed at ATE
  - » Thermal Offset compensated out of system
- **Quality: MSL 1 Performance**
  - » Units Pass Full Qualification tests
  - » No Performance Failures in 1200 units



Frequency Stability (20ppm)

Lot	Stress	Sample Size	Time Point	Stress Out Date	Status
UT01	*Preconditioning MSL 3*	300		1/22/2008	*All Passed*
	*Temp Cycle (TC)**	80	*500 cycles*	2/5/2008	*All Passed*
			1000 cycles	2/22/2008	*All Passed*
	*Thermal Shock (TS)**	60	*200 cycles*	2/16/2008	*All Passed*
	*Temp Humidity (HAST)**	80	*96 hours*	2/5/2008	*All Passed*
	*Autoclave (PCT)**	80	*168 hours*	2/5/2008	*All Passed*
	Hi Temp Storage (HTS)	80	*500 hours*	1/30/2008	*All Passed*
			1000 hours	2/26/2008	*All Passed*



MSL 1 Test Results: 0/22 Units Failed

Encapsulated MEMS

Doing the MEMS and the Package together has some benefits

- Improved Materials Performance
- Opportunities to improve the device one characteristic at a time
- Ovenization and materials compensation examples shown
- Short path to commercialization?
- Interesting platform for MEMS materials research studies?
- Exciting prospects for MEMS to finally impact PNT

SiTime™ It's about time

BOSCH

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Encapsulated MEMS

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Gary Yama, Rob Candler[5], Bosch RTC
Amy Duwel, Mat Varghese, Draper Labs
Richard Nguyen, SPAWAR Amit Lal, DARPA MTO
Current Addresses : *SiTime, [1]UC Berkeley, [2]NetLogic, [3]DARPA, [4]Intel, [5]UCLA

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DRAPER LABORATORY

SPAWAR Systems Center San Diego

DARPA MTO

Questions???

Funding : DARPA HERMIT, Bosch RTC, NSF

Transducers '07 Program Committee Invitation

Support : Clark Nguyen, John Vig, Kurt Petersen, Gary Yama, …

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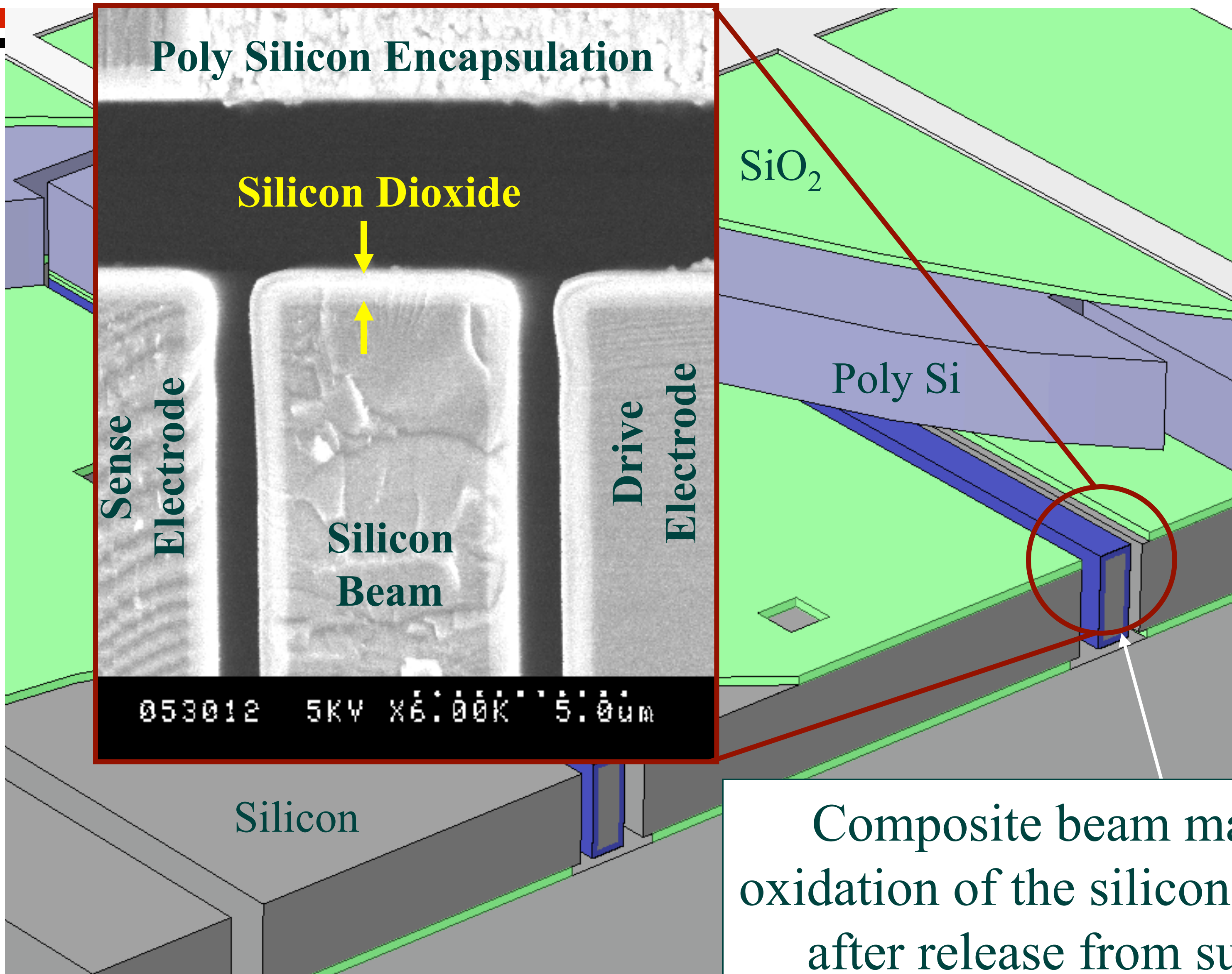
SiTime It's about time

BOSCH

MTO DARPA

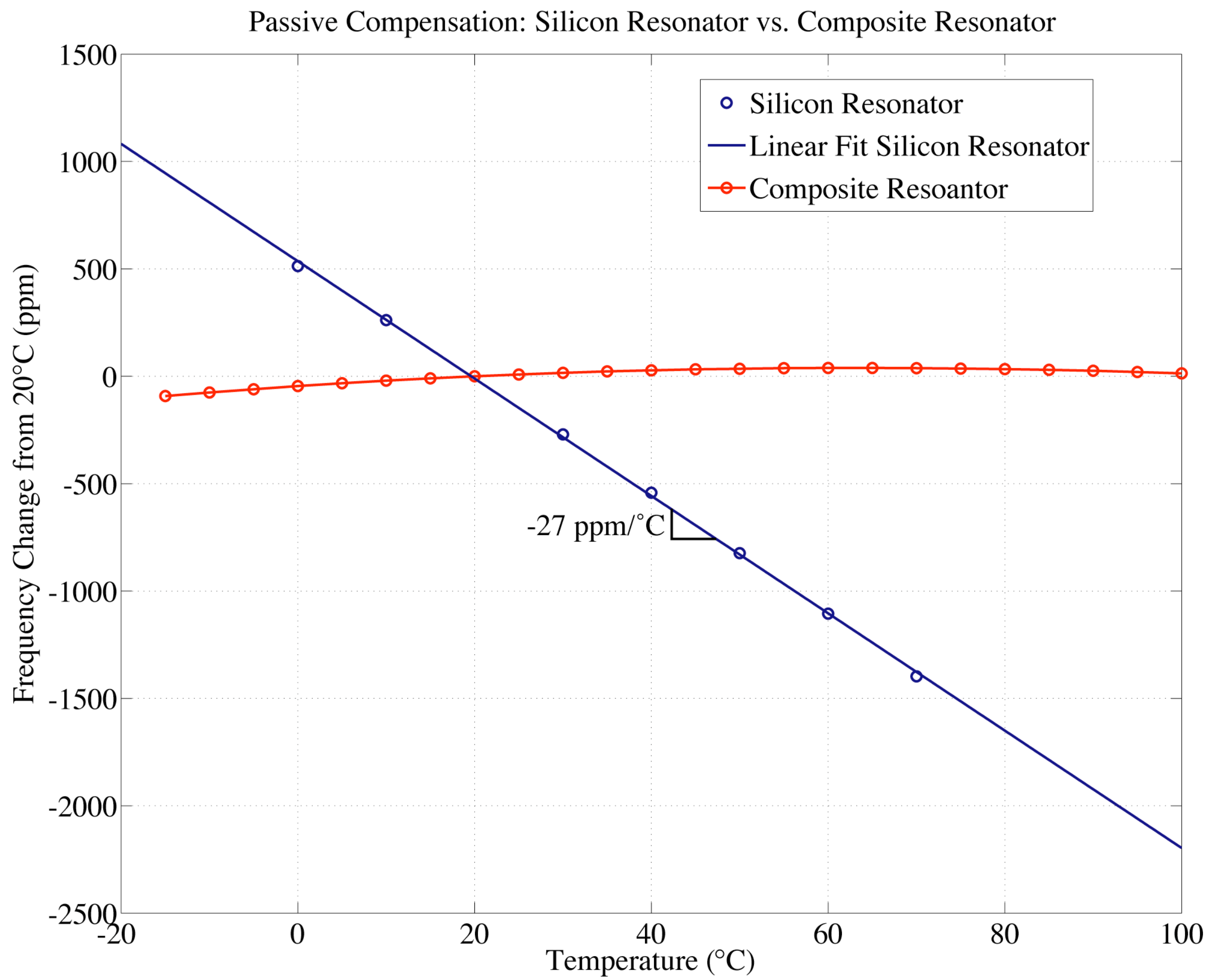
Stiffness Compensation to Reduce TCF

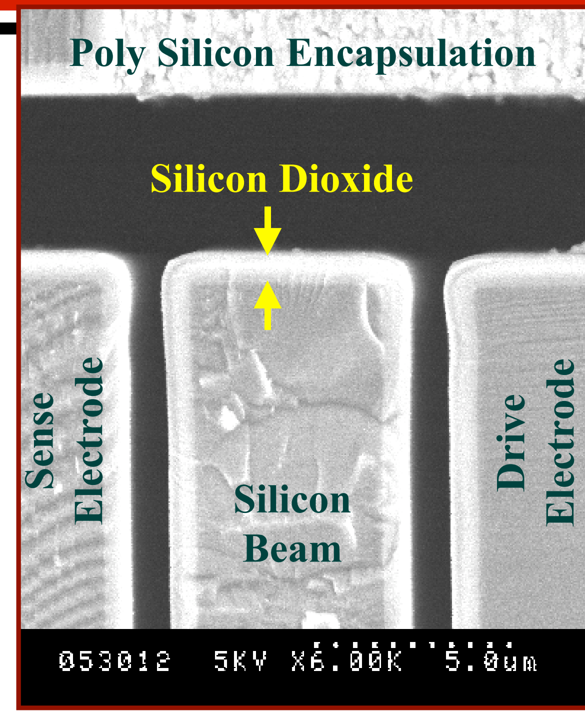


Composite beam made by oxidation of the silicon resonator after release from substrate

Renata Melamud, Bongsang Kim, Matt Hopcroft, …

Stiffness Compensation to Reduce TCF



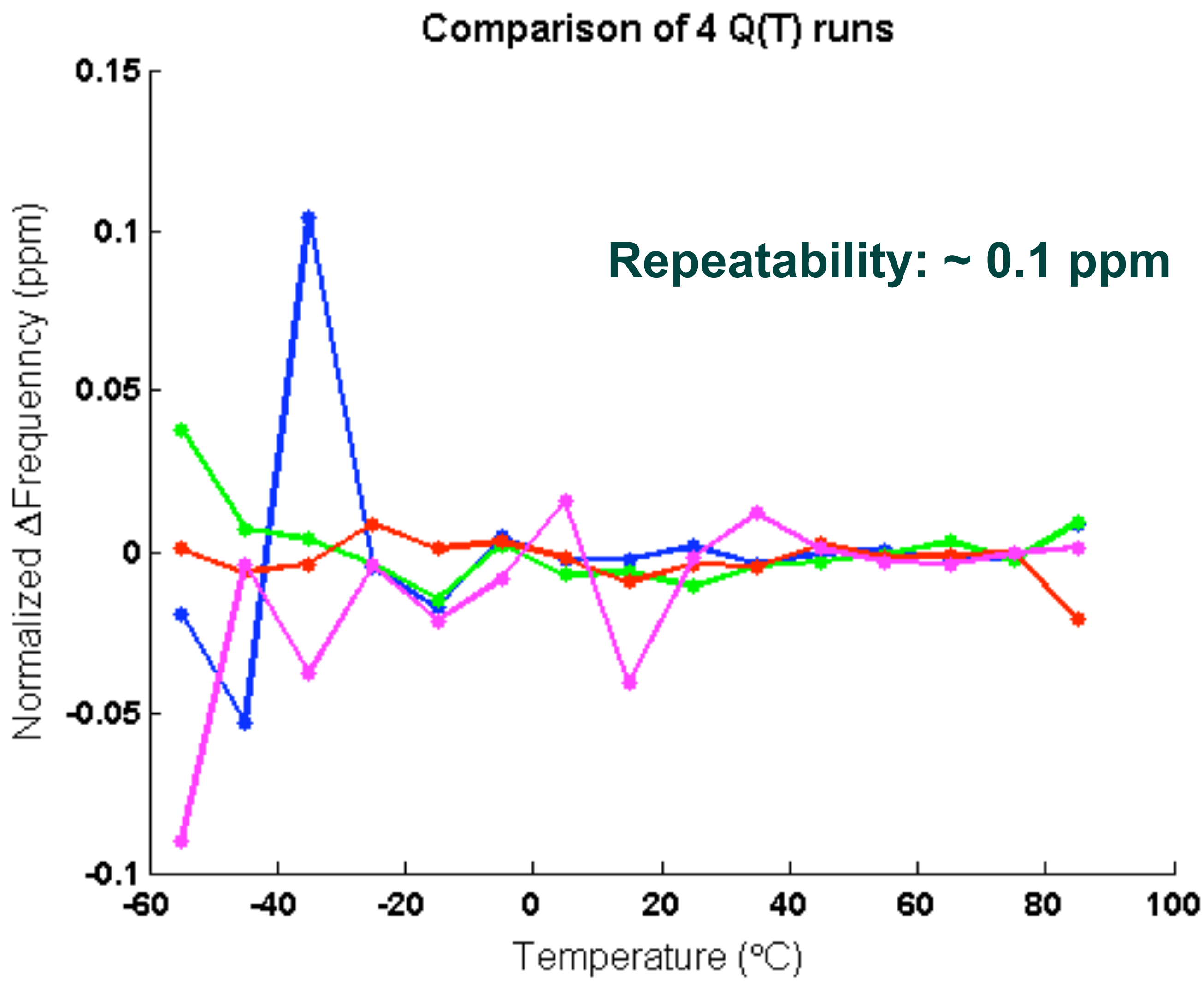


Should provide 20 reduction in frequency error of resonators without any other improvements

Brings these devices into the sub-ppm error range

Renata Melamud, Bongsang Kim, Matt Hopcroft, …

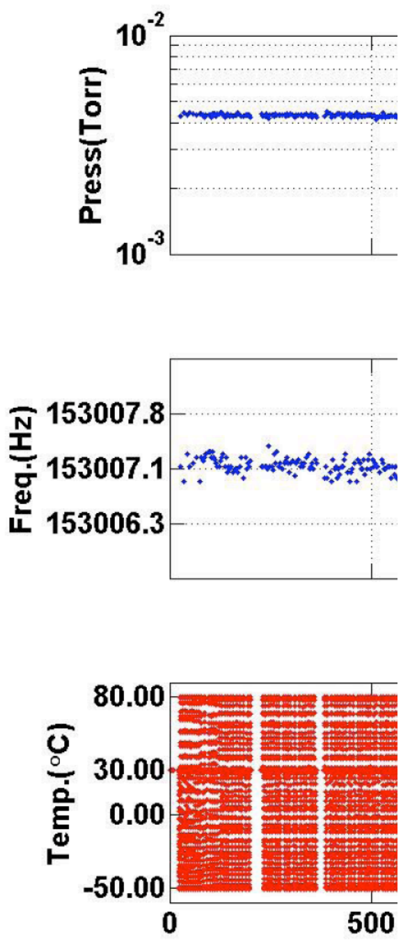
12/06 Result -> Theoretical Limit



Limited by drift and temperature sensitivity of external circuits -> more work needed here

Matt Hopcroft

Long-Term Stability during Temperature Cycles from -50C to +80C



Intermediate conclusion :

Ultra-clean, high-temperature package eliminates drift, aging, etc.

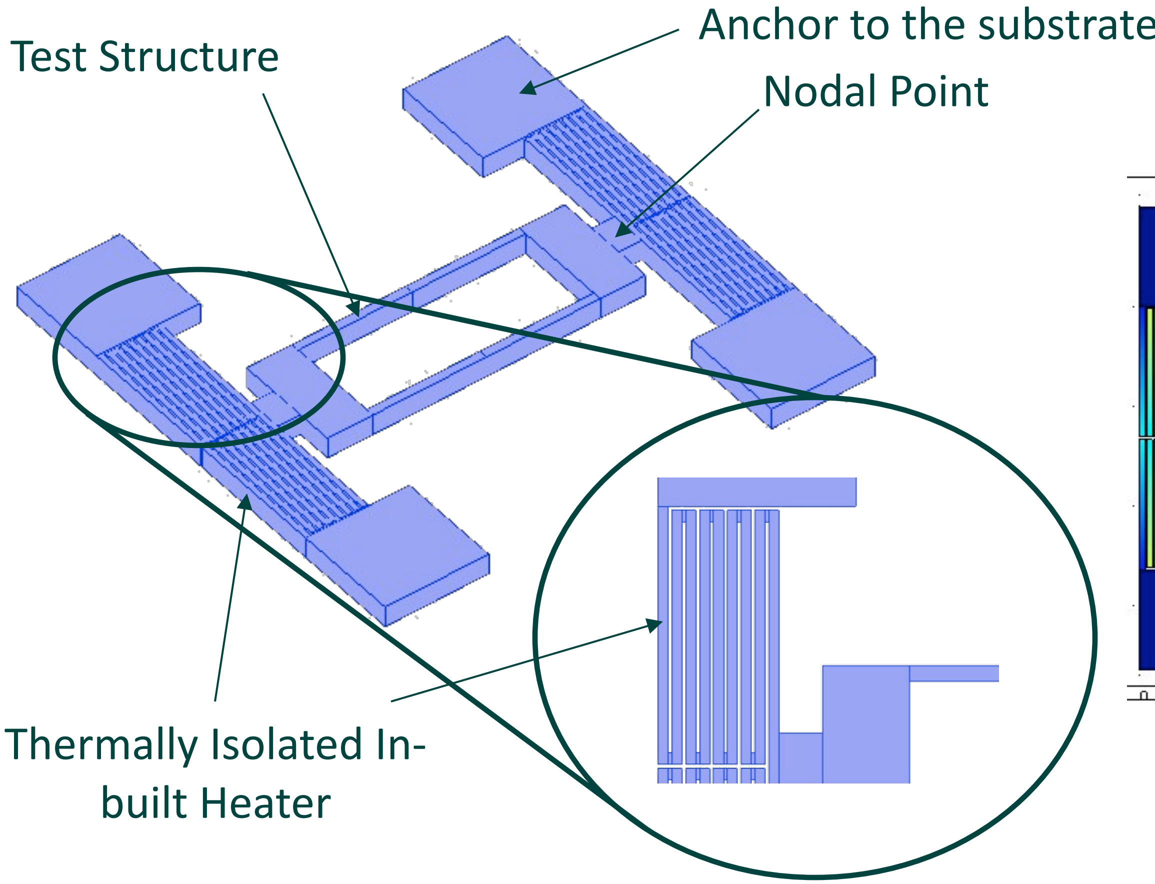
Remaining Problem : Temperature Coefficient of Frequency (TCf) in MEMS.

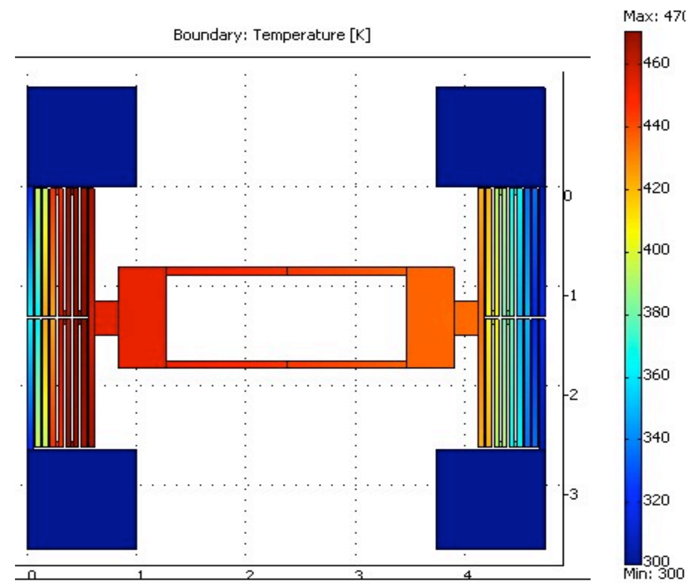
Can encapsulation provide opportunities for dealing with TCf?

No Evidence for Leakge, Drift, Aging, or other fundamental barriers for MEMS references

Bongsang Kim

In-Built Heater for Resonating Structure

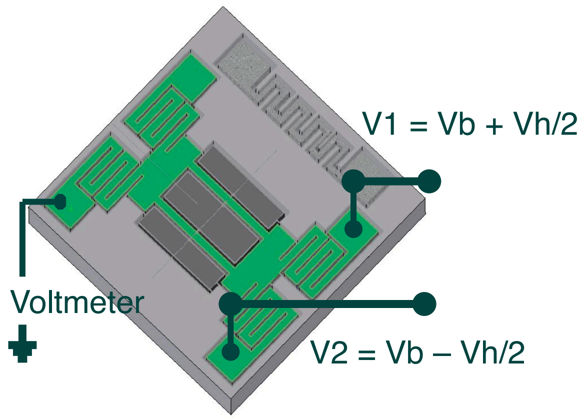




- Serpentine silicon structure is used as an in-built heater.
- Joule heating is used for heater.
- By placing these in-built heaters at nodal points, the fundamental mode vibration of test structure is not affected.

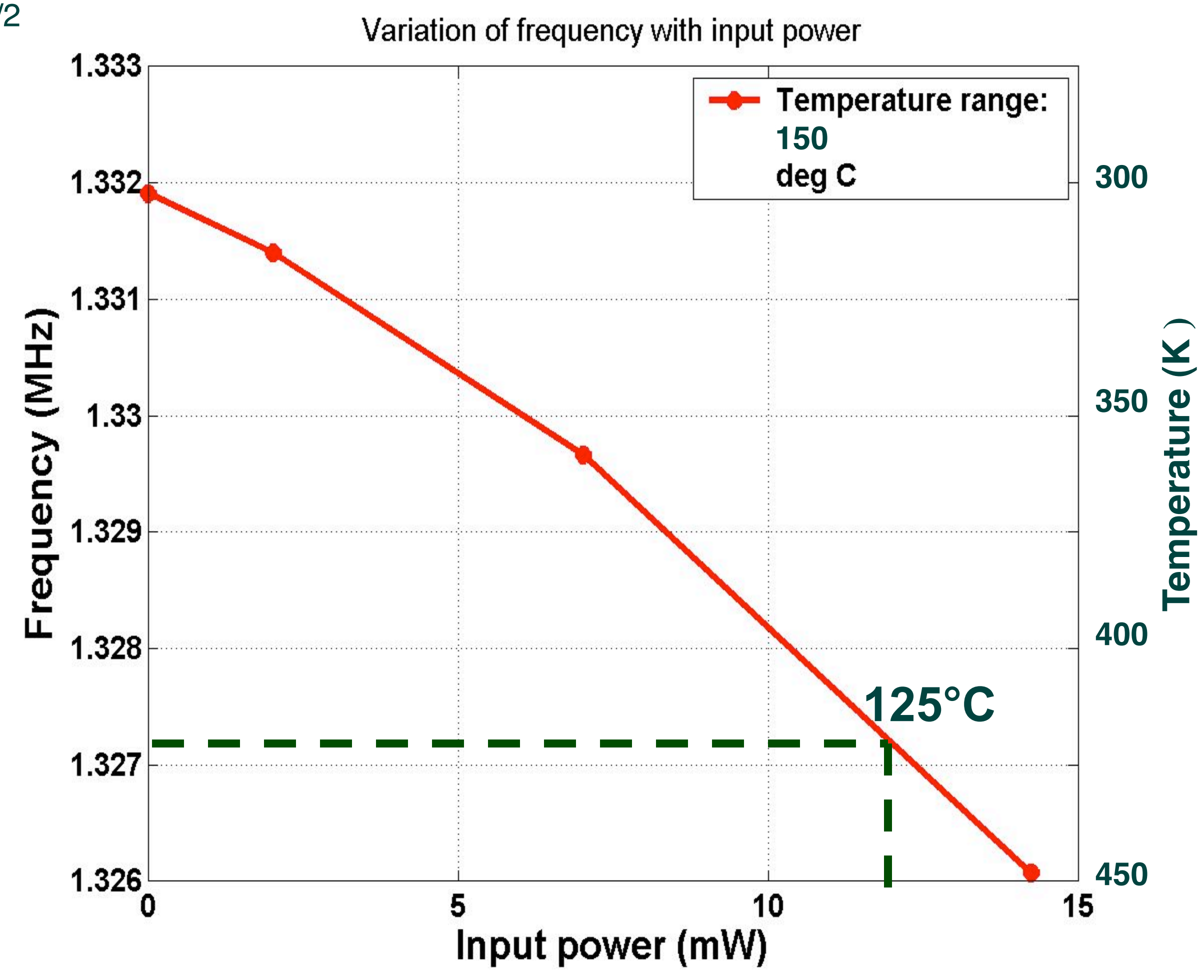
Chandra Jha, Matt Hopcroft

Heating the Resonator within the Encapsulation



We can apply heat to regulate temperature.

Thermal Resistance is high enough to allow 125C heating with only 12 mW.



Chandra Jha

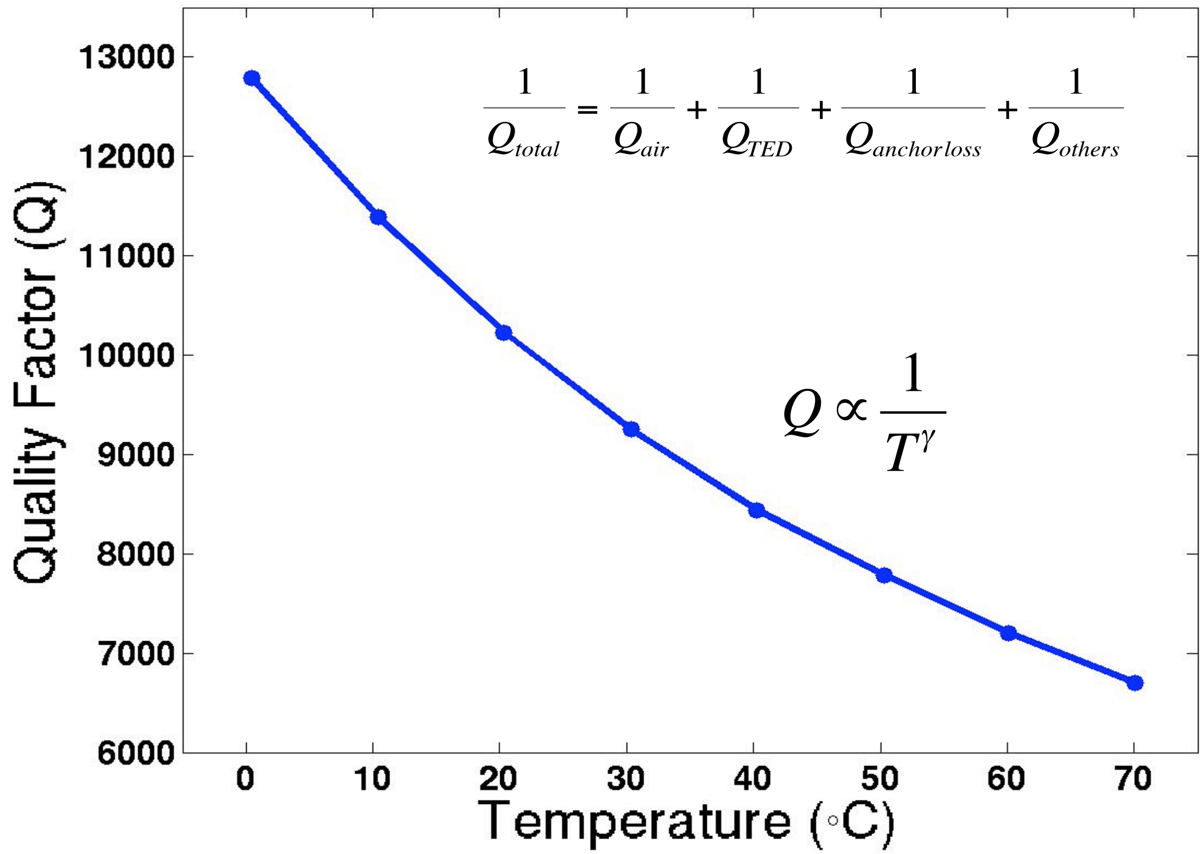
Temperature Control Requires a Thermometer

Q(T) is an interesting candidate thermometer

Measures Temperature at the exact location that matters most

No heating current in measurement

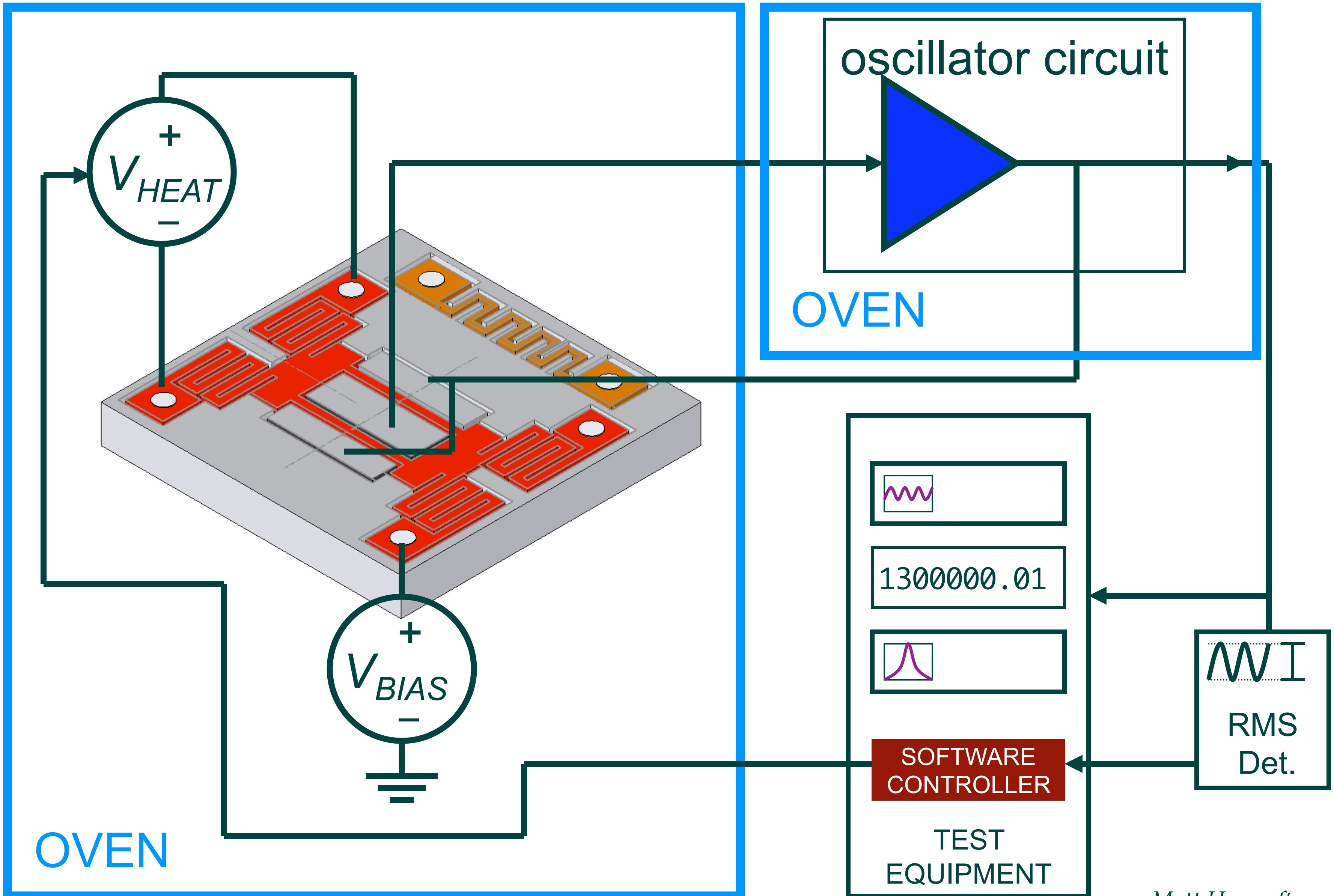
Can be extracted using simple external circuits



About 1% change of quality factor for 1 degree C temperature change.

Bongsang Kim, Matt Hopcroft, Saurabh Chandorkar Rob Candler

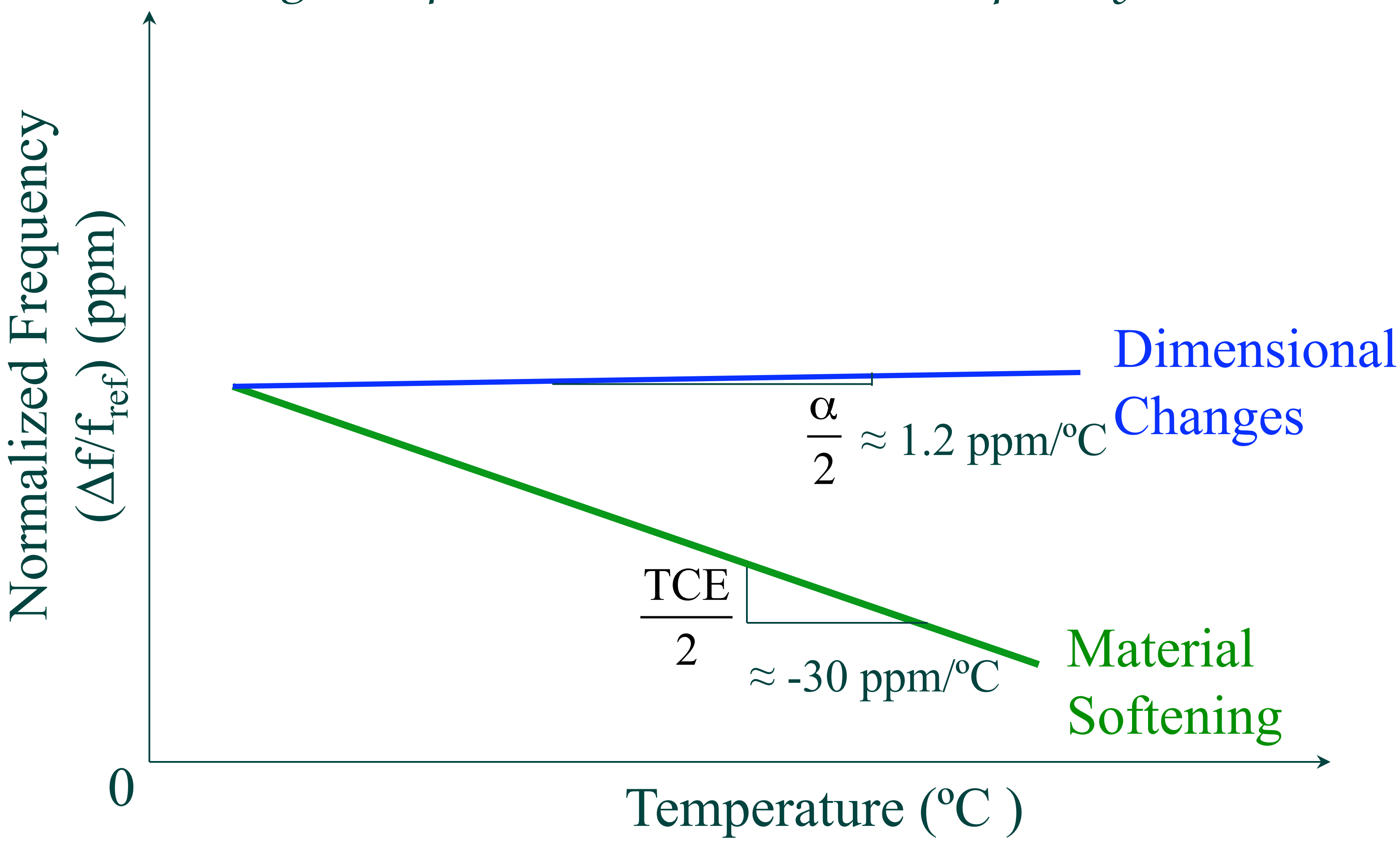
Test Setup - Closed-Loop



Matt Hopcroft

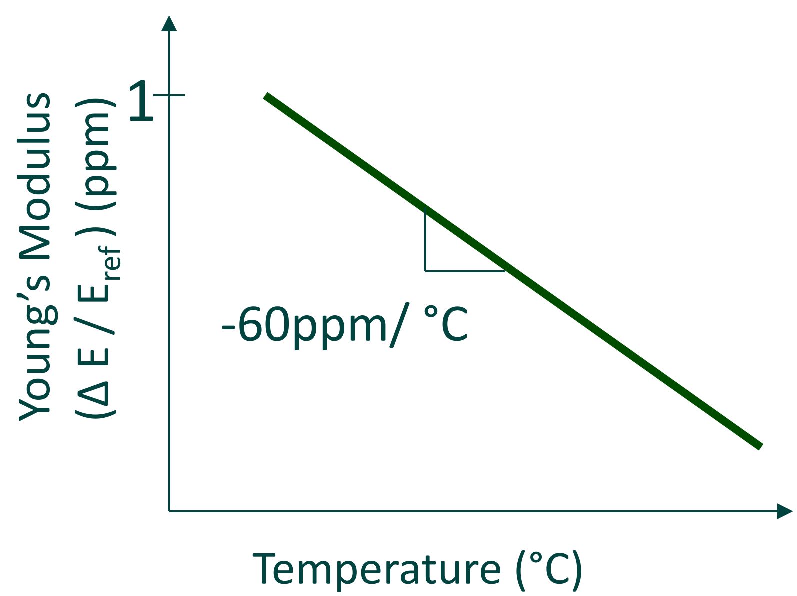
Temperature Dependence of F

Silicon Softens as Temperature Increases -> large temperature variation in Frequency

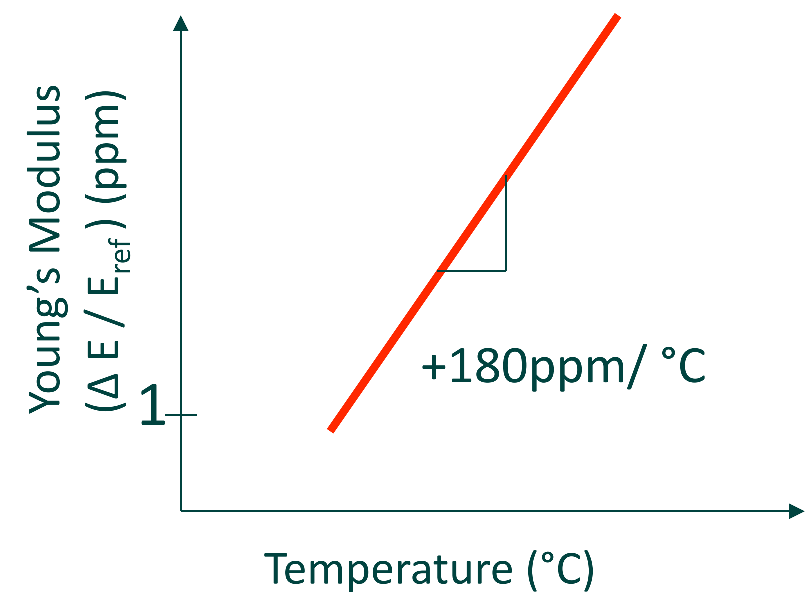


Temperature Stability Strategy

Silicon Young's Modulus



SiO_2 Young's Modulus



- **Silicon becomes softer with increase in temperature**
- **Silicon dioxide (SiO_2) becomes stiffer as temperature increases**
- **Combination of Si and SiO_2 will compensate resonant frequency change due to temperature change**
- **SiO2 can be added to our fabrication sequence.**

Extreme TCf Reduction Strategy

Silicon becomes softer as Temperature increases
TCE = -60ppm/°C

↓

Resonant Frequency Changes
TCf = -30ppm/°C

Active Compensation
- Temperature sense
- Feedback compensation

5000x Improvement

Passive Compensation
- Compensating material
- Reduce TCf

20x Improvement

Combine Active and Passive Compensation
Achieve Very Low TCf

TCf : Temperature coefficient of frequency

TCE : Temperature coefficient of Young's Modulus