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Atomic force microscope lithography using amorphous silicon as a resist and advances in parallel operation

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Lithography on (100) single-crystal silicon and amorphous silicon is performed by electric-field-enhanced local oxidation of silicon using an atomic force microscope (AFM). Amorphous silicon is used as a negative resist to pattern silicon oxide, silicon nitride, and selected metals. Amorphous silicon is used in conjunction with chromium to create a robust etch mask, and with titanium to create a positive AFM resist. All lithographies presented here were patterned in parallel by arrays of two piezoresistive silicon or two silicon-nitride cantilevers. Parallel arrays of five piezoresistive cantilevers were fabricated and used in imaging and lithographic applications. A 400 μm x 100 μm parallel image is obtained in the time it would normally take to obtain a 100 μm x 100 μm image. In our method of parallel operation, it is only possible to image and lithograph in modes that do not require feedback. In imaging, this limits the possible applications of the parallel AFM. During parallel lithography, discrepancies are seen between the tip in the feedback loop and those that are not. To overcome these differences it will be necessary to devise a system where each of the tips in the array are controlled by individual feedback loops. © 1995 American Vacuum Society.

I. INTRODUCTION

Scanning probe lithography (SPL) has recently gained popularity because device feature sizes in integrated circuits are approaching the optical diffraction limit. For SPL to be accepted as a lithographic tool in the deep submicron regime, it must be able to pattern arbitrary surfaces in a manner that is compatible with clean room processes. Using amorphous silicon as a resist provides a way to lithograph general surfaces in both the positive and negative tone. Recently, this type of scanning probe lithography was shown to be compatible with device processing through fabrication of a 0.1 μm metal–oxide–semiconductor field-effect transistor (nMOSFET). 1

Single-tip scanning probe lithography began with Dagata et al. 2 on hydrogen-passivated (111) single-crystal silicon. Becker et al., 3 Lyding et al., 4 Snow and Campbell, 5 and Campbell and Snow 6 have made further advances by using the scanning tunneling microscope (STM) and atomic force microscope (AFM) to pattern other orientations of silicon. The mechanism for this type of lithography is presumed to be that the intense field from the tip desorbs the hydrogen and increases the oxidation rate on the exposed silicon. Kreuzer 7 points out that the electric field strength at the apex of the scanning tip (>0.1 V/Å) is comparable to the field experienced by the electrons orbiting the nucleus. An oxide pattern formed in this manner can serve as an etch mask for transferring the pattern into the silicon substrate.

Lyding has shown that the STM oxidized linewidth can be as small as 15 Å. Scanning probe lithography has been limited in that only certain surfaces can be directly patterned. Song et al., 8 and Sugimura et al., 9 have used the STM to selectively oxidize metal films. Majumdar et al. 10 used the AFM to expose thin layers of PMMA with electrons from a conducting tip, and Mamin and Ruger 11 used the AFM to thermomechanically modify PMMA. Although these techniques are useful in certain applications, it is desirable to pattern arbitrary surfaces. For this reason we prefer the lithography system of selectively oxidizing amorphous silicon as discussed by Kramer et al. 12 Amorphous silicon is advantageous because it is compatible with semiconductor processing, can be deposited in thin films, and it can serve as an etch mask to many materials.

II. LITHOGRAPHY

Snow and Campbell replaced the conducting probe of the STM with a titanium-coated nitride cantilever and performed electric-field-enhanced oxidation with the AFM. In our work we used two types of cantilevers. For lithographies with silicon-nitride cantilevers, we evaporated 300 Å of titanium onto the cantilevers to form the conducting path. Our work with piezoresistive silicon probes uses the technology developed by Tortone et al. 13 at Stanford. Electrical connection to the tip in a piezoresistive cantilever can be easily implemented, the piezoresistor’s duty need only be changed from a sensor to a conducting path. Although the piezoresistors duty can be toggled depending on the mode of operation of the AFM, we dedicated the piezoresistor to lithography and imaged using the Park Scientific Instrument “Universal” commercial laser deflection system. During our fabrication of the piezoresistive cantilevers, a 300 Å protective oxide was grown over the final tip structure. This insulating layer was removed in 10:1 buffered oxide etch for lithographic applications. For all lithographies, we first passivated the sample in a 5:1 DI:HF solution for 4 min and blew it dry with nitrogen. During lithography, we grounded the tips and applied a positive bias to the sample through a conducting clip. All of the lithographies presented in this article were performed in parallel. However, in some cases, only a single pattern is presented to show more detail in the figures.
Figure 1 shows parallel lithography performed directly on (100) silicon with an array of two piezoresistive cantilevers. The lithography was transferred into the silicon surface at room temperature in 11 molar aqueous KOH solution for 1 min. In this lithography, each line within the structure was patterned in the same amount of time. The line lengths were increased such that the tips’ scan rate is increased from 0.1 to 2.0 μm/s at a tip–sample bias of 20 V. The individual lines in this pattern have a width of 0.2 μm. The lithography was performed at a constant force of 600 nN with the tip on the right in the feedback loop. The tip on the left was scanned across the surface at an undetermined force. From Fig. 1 it is clear that the tip in the feedback loop produced high-quality lithography at higher speeds. If we realign and switch the cantilever in the feedback loop, we produce the same pattern in reverse, indicating that this phenomenon is not a tip effect.

Comparing the parallel images of Fig. 1 (force=600 nN, k=4.1 N/m, silicon) and Fig. 2 (force=80 nN, k=0.5 N/m, nitride), we see the same disparity between the lithographies from the tips that are in the feedback loop and those that are out of the feedback loop through a wide range of cantilever geometries. This indicates that the quality of the lithography is related to feedback control, emphasizing the importance of individual z-axis control in future arrays of cantilevers.

Since amorphous silicon (α:Si) can be hydrogen passivated in the same manner as single-crystal silicon, it is possible to perform AFM lithography on thin α:Si films. Combining Kramer’s patterning of α:Si films and Snow’s work on suspended silicon structures, we deposited 1000 Å of low-pressure chemical vapor deposition (LPCVD) α:Si at 400 mTorr, 560 °C, and a 1.24:SiH 4 :H 2 gas ratio onto 5000 Å of thermal oxide. By patterning the α:Si into the shape of a cantilever and using the field-induced oxide as an etch mask, we defined the cantilever structure in α:Si. The α:Si is etched in a 1:1 SF 6 :Freon 115 plasma at 150 mTorr and 0.22 W/cm². By undercutting the cantilever in a 6:1 buffered oxide etch, we fabricated a free-standing amorphous-silicon structure shown in Fig. 3. The cantilever shown is 350 μm long, 0.4 μm wide, and 1000 Å thick. The cantilever pedestal is 5 μm by 5 μm. The gap between the cantilever and the substrate is 1500 Å. The viewing angle is 85°.

A general form of resist for AFM lithography can be implemented by using the α:Si structure as an etch mask instead of the final feature. A 1000 Å α:Si film on 5000 Å of oxide was prepared by the same method described above. Lines were lithographed in parallel by silicon-nitride cantilevers coated with 300 Å of titanium with the AFM at 0.5 μm/s. Each line was created with two passes of the tip (one in each direction). The lithographed pattern was transferred
into the $\alpha$:Si in the same SF$_6$:Freon 115 plasma. The pattern was then transferred into the 5000 Å of oxide by reactive ion etching (RIE). The dielectric etch was performed at a dc bias of $-530$ V, power density of 0.95 W/cm$^2$, gas mixture of 14.2:1 Freon 23:O$_2$, and pressure of 250 mT. Figure 4 shows the resulting lithography on oxide where the line on the left was patterned at 25 V with the voltage decreasing by 1 V for each line to the right. The linewidth decreases from 0.25 μm at 25 V to 0.16 μm at 13 V. Decreasing linewidths with decreasing voltage is in agreement with the work done on single-crystal silicon by Ejiri et al. $^{15}$ Figure 2 shows this method used to pattern 3500 Å of silicon nitride. This lithography was accomplished with an array of two nitride cantilevers. The nitride was deposited by LPCVD at 500 mT, 780 °C, and 6:1 SiCl$_2$H$_2$:NH$_3$ . The 1000 Å $\alpha$:Si mask was deposited, and etched in the same manner. The lithography was performed at 20 V with the scan speed ranging from 0.2 to 2.0 μm/s. The nitride, which was then partially masked by the $\alpha$:Si, was etched in the same dielectric etch that we used to pattern the oxide. Again, in Fig. 2 there is a difference between the parallel patterns due to only one tip being in the feedback loop. The transferred linewidths range from 0.3 (patterned at 0.2 μm/s) to 0.14 μm (patterned at 0.55 μm/s). The decreasing linewidth with increasing scan speed is also in agreement with Ejiri’s work.

The transfer of the patterned lines into the nitride in Fig. 2 is incomplete at higher scan speeds for both images. It is due to limited etch selectivity; if the field-induced oxide is not thick enough to withstand the entire $\alpha$:Si etch, it will not be able to mask the entire thickness of $\alpha$:Si. Likewise, if the remaining $\alpha$:Si is not thick enough to withstand the entire substrate etch, complete pattern transfer will not be obtainable. In general: Max. substrate etch depth = AFM-induced oxide thickness × selectivity of the $\alpha$:Si etch against oxide × selectivity of the substrate etch against $\alpha$:Si.

Etching beyond this limit will provide no further relief to the lithographed pattern because the masking material has been completely etched. This limit can be circumvented by inserting an intermediate layer that has a high selectivity against the substrate etch, and its etch has a high selectivity against $\alpha$:Si. This method of resist enhancement is similar to the work done by Kruger et al. $^{16}$ on multilayered e-beam resists. Inserting such a material makes complete pattern transfer easily obtainable using an $\alpha$:Si mask.

AFM lithography using a chromium intermediate layer is shown in Fig. 5. On (100) silicon wafer 9500 Å of thermal oxide, 3500 Å of LPCVD nitride, 1500 Å of evaporated chromium, and 3500 Å of evaporated $\alpha$:Si were deposited in sequence. AFM lithography and $\alpha$:Si lithography performed in the same manner as before, leaving the chromium layer partially exposed [Fig. 5(a)]. The chromium was then etched in a commercial chromium wet etch exposing the nitride. The nitride was RIE etched in NF$_3$ (dc bias = $-200$ V, power density = 0.46 W/cm$^2$, and pressure = 60 mT) and oxide below was then etched in the dielectric etch mentioned previously [Figs. 5(b) and 5(c)]. The $\alpha$:Si masking layer was removed in the nitride etch (selectivity = 2:1 $\alpha$:Si:Ni). How-

FIG. 4. 5000 Å of thermal oxide patterned with an amorphous-silicon mask which was lithographed by the AFM. Lithography on the amorphous silicon occurred at 0.5 μm/s. The line on the left was lithographed at 25 V; each line to the right was lithographed at one less volt.

FIG. 5. AFM lithography using a compound amorphous-silicon/chromium resist. (a) Parallel pattern transferred into 3500 Å of amorphous silicon. The material in the background is 1500 Å of chromium. (b) The lithographed pattern transferred into 3500 Å of silicon nitride and 9500 Å of silicon dioxide. The amorphous-silicon masking layer is completely removed, exposing the chromium. (c) Closeup of a 0.3 μm line. (d) The pattern is transferred into 3 μm of the silicon substrate. The chromium masking layer is intact.
ever, because these etches do not significantly attack chromium, the intermediate masking layer remained undisturbed. The pattern was then transferred 3 μm into the silicon in an isotropic silicon etch. Figure 5(d) shows the masking layer still completely intact after transferring through of 4.5 μm chromium, nitride, oxide, and silicon in four different etches.

So far we have only used α:Si as a negative resist, hence what was exposed with the AFM remains during development (etching). In many instances it would be more convenient to have a positive resist, which would result in what was exposed being removed during development (etching). By exploiting the difference in etch rate between α:Si and titanium oxide, titanium/α:Si can be used as a positive resist as it is shown in Fig. 6. On a (100) silicon wafer we deposited 1500 Å of titanium by evaporation, then without breaking vacuum, we immediately deposited 3500 Å of amorphous silicon. When the sample was removed from the evaporator, the α:Si film protected the titanium from oxidizing. AFM lithography was performed and the pattern was transferred into the α:Si in the same manner, partially exposing the titanium surface [Fig. 6(a)]. The exposure of the titanium surface to air formed a native oxide on the titanium in the regions that were not protected by the α:Si pattern. We then etched the surface in a 1:1 SF₆:CF₃Br plasma at 150 mT and 0.81 W/cm². This etch attacked titanium, titanium oxide, and α:Si, but all at different rates. The differential etch rate between titanium oxide and α:Si is such that the entire α:Si layer is etched before the native titanium oxide. Once the α:Si is completely removed, the unoxidized titanium beneath is quickly attacked. The titanium which was not masked by the α:Si was still protected by the native oxide. The resulting titanium pattern was then used as an etch mask to transfer the pattern 400 Å into the silicon substrate [Fig. 6(b)].

III. PARALLEL OPERATION

The AFM might become a competitive tool for lithography if the scan size, image acquisition rate, and exposure rate are improved. At present the scan size is limited to about 100 μm by 100 μm because the piezoelectric tube scanner becomes unwieldy at larger scan sizes. AFMs operate with a single probe, and thus an entire image or lithograph must be obtained by examining each pixel in sequence. This serial process is quite time consuming, even for scan sizes smaller than the 100 μm by 100 μm limit. To address these problems of scan size and speed, we have fabricated and operated AFMs incorporating multiple probes formed by parallel arrays of piezoresistive cantilevers.

Our work with parallel probes extends from the cantilever process developed by TORTONESI et al. He fabricated AFM probes that sensed force by using the piezoresistive property of silicon. Piezoresistive cantilevers with integrated single-crystal tips, require no external sensing or alignment mechanism to obtain images with atomic resolution. This was a key step in the development of parallel arrays of AFM probes. It would be impractical and nearly spatially impossible to operate a large array of closely spaced probes whose sensing mechanism must be individually aligned and maintained.

Large area imaging is one of many applications where arrays of cantilevers could be employed; lithography is another. To increase the throughput of a system based on scanning probes, we believe that it is imperative to use parallel arrays of probes.

We used piezoresistive cantilevers with integrated single-crystal silicon tips for parallel imaging with the AFM. Cantilevers of equal dimensions were fabricated on a die such that their tips were collinear. An array of five cantilevers is shown in Fig. 7. The die containing the cantilevers was fastened to a chip package and the contact pads of the piezoresistors were wire bonded to the output pins. The cantilever assembly was inserted into a lab constructed AFM with the tips at a 15° angle to the sample. For converting the cantilever resistance into a voltage, the leads from the piezoresistors were connected to individual Wheatstone bridges biased at 4 V.

The voltage signals from the cantilevers positioned at the ends of the array were monitored as the cantilevers were brought into contact with the sample. Once one of the end cantilevers made contact with the sample, the approach was stopped, and the distance from the opposite cantilever to the sample was measured. These measurements were used to adjust the approach angle of the array and the process was repeated until the end cantilever was at most 0.5 μm from sample. All the tips were then brought into contact with the surface and each cantilever was operated as a standard AFM.
Figure 8 shows a 400 µm x 100 µm constant height image of oxide on silicon. The spring constant of the cantilevers used in this image is 4.1 N/m, and minimum detectable deflection is 0.4 Å in a 100 Hz to 1 kHz bandwidth.

Figure 8 shows an AFM image acquired with multiple probes to increase the image area for a given scan size and scan time. Alternatively, with parallel probes, we can decrease the scan time for a given image area. Thus, parallel imaging provides a mechanism where either the acquisition time is decreased or the scan size is increased by a factor equal to the number of probes acting in parallel.

The mode of imaging that we used was the constant height mode. Since there is only one z-axis control for the entire array of cantilevers, we could not implement a feedback of the error signal to the individual cantilevers for constant force or noncontact imaging modes. It is possible to feedback to one of the cantilevers in the array, but since each tip experiences a different interaction with the sample, this is not useful in imaging applications. In lithographic applications we have had success at parallel lithography with two probes at slow scan speeds. Again the problem of feedback control to the individual tips prevents us from higher speeds. Experiments involving integrated z-axis cantilever control are planned.

IV. CONCLUSIONS

We have shown the potential of the AFM as a general lithographic system. To address the issue of throughput, we have fabricated parallel AFM probes that require no external alignment and used them for lithography. These probes can also be used in imaging mode to determine the locations to be lithographed, and to monitor the AFM-induced oxide for instant feedback on the quality of the lithography. We have only been able to reliably lithograph surfaces with arrays of two cantilevers. Attempts at lithography with arrays of five cantilevers produce large variation in the quality of the lithography from tip to tip. We believe this is due to the lack of feedback control on each probe. We are currently fabricating arrays with integrated z-axis actuators to address this issue.

We have patterned single-crystal silicon, α-Si, oxide, nitride, and selected metals in parallel by direct writing, or by using amorphous silicon as a resist. By using α-Si in conjunction with chromium we have transferred AFM lithographed patterns 4.5 µm into materials common to the semiconductor industry. We have used α-Si in conjunction with titanium to create a positive AFM lithography resist. In work presented elsewhere, we have shown that AFM lithography is compatible with semiconductor device processing by fabricating a 0.1 µm nMOSFET with reasonable device characteristics.

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