An Inherently Linear Phase-Oversampling Vector Modulator in 90-nm CMOS

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Abstract—A four-antenna vector modulator (VM) beamforming receiver in 90-nm CMOS operating between 2.4 and 4.9 GHz is presented. The VM is based on a phase-oversampling technique that allows the synthesis of inherently linear, high-resolution complex gains without complex variable gain amplifiers. It achieves 360° phase shift programmability with 8-bit digital control, a measured < 4.2° phase error at a back-off of 4 dB from the maximum gain setting, and a complex gain constellation with a mean error vector magnitude of < 2%. The monolithic beamformer also demonstrates an interference cancellation of > 24 dB for interferers impinging from different directions.

I. INTRODUCTION

Beamforming for power gain or interference cancellation in multi-antenna wireless systems enables the exploitation of spatial diversity and increased receiver dynamic range. Beamforming in the analog domain can be performed with vector modulators (VMs), and has been explored using complex RF variable gain amplifiers (RFVGAs) in Cartesian-combining architectures [1–4]. As supply voltages decrease due to CMOS scaling, a trend has emerged in which analog circuit-block complexity is gradually being transferred to the digital backend and/or to the architectural level. Phase oversampling and coarse quantization is one technique that allows the circuit complexity of RFVGAs to be shifted to the architectural level, thus linearizing the receive paths at no loss of complex gain accuracy.

In this paper, a CMOS beamforming IC fabricated in 90-nm CMOS based on phase oversampling and coarse quantization is demonstrated. The chip contains four down-conversion paths, all supplied from 1.2 V. The VM architecture utilizes no RFVGAs and achieves a measured < 4.2° phase error at a back-off of 4 dB from the maximum gain, and a complex gain error vector magnitude (EVM) of 2% over all complex gain points. In an active interference cancellation test, the chip achieves > 24-dB cancellation of interferers, potentially relaxing the dynamic range requirements of subsequent baseband blocks.

II. VECTOR MODULATOR ARCHITECTURE

The presence of large blockers close to the received signal poses numerous challenges for beamformer designs. The use of nonlinear amplifying components after the low noise amplifier in the receive path may allow the blockers to desensitize the receiver or to corrupt a weak desired signal with intermodulation products. If used in an interference cancellation application, the resolution of the VM complex gain should be proportional to the desired cancellation accuracy. For example, to cancel a large interferer with random arrival angle by 20 dB, gain control must be within approximately 10%, and phase resolution must be within 5.7°. This degree of resolution is not needed when the receive paths are utilized mainly for power gain or diversity. Thus to achieve accurate cancellation of large interferers in the analog domain, it is advantageous to have high complex gain resolution as well as high linearity.

A diagram of the implemented direct-conversion phase-oversampling VM architecture is shown in Fig. 1. Each VM consists of a transconductance (Gm) amplifier, a bank of 8 mixers, a bank of cross-coupled NMOS switches, and a set of I-channel and Q-channel transimpedance amplifiers (TIAs). Each mixer is driven by a separate LO phase, and phase-shifts the incoming signal during frequency translation. A complex gain is realized by choosing the correct sign of the LO phases between 0° and 180°, and then splitting the LO terms into the I and Q TIAs. Each LO phase has a separate LO phase, and phase-shifts the incoming signal during frequency translation. A complex gain is realized by choosing the correct sign of the LO phases between 0° and 180°, and then splitting the LO terms into the I and Q TIAs. The b4 terms can be chosen through a brute force search or a Σ∆ algorithm running in the digital domain [5]. In contrast to employing fine resolution RFVGAs in the signal paths, the exploitation of multiphase LO to establish the complex gain decouples the circuit complexity from the signal integrity of the receive paths. In addition, the use of passive mixers for phase shifting avoids any nonlinear amplification in the receive path, further enhancing the linearity of the receiver.

III. CIRCUIT IMPLEMENTATION

The circuit schematic of a single down-conversion path of the VM, highlighted in Fig. 1, is shown in Fig. 2. In each path, the received signal is converted to current through a resistively degenerated cascode Gm amplifier. The current is then split evenly between the passive mixers due to the uniform spacing of the LO phases between 0° and 180°, and then split again between the I and Q TIAs at the outputs of the mixers. A spiral inductor is used at the Gm amplifier output to tune out the parasitic capacitances of the amplifier and the mixer bank. The Gm amplifier input is resistively matched to 50 Ω for simplicity.

A double-balanced passive mixer topology was chosen for...
the mixers due to its high achievable linearity. The high IIP2 of passive mixers is important for direct-conversion architectures such as this one. The lack of static power consumption in passive mixers is notable, given the large number of such as this one. The high achievable linearity of passive mixers is important for direct-conversion architectures due to its high achievable linearity. The high IIP2 of the VM down-conversion paths. It is advantageous for the passive mixers, sum together the outputs from all the mixers in a portion of each LO cycle. In order to properly isolate the summing nodes of the two TIAs, resistors are placed at the outputs of the mixers. The isolation resistors increase the voltage swing at the mixer output nodes, potentially increasing the noise figure of the down-conversion path and possibly limiting the achievable linearity. Extra design care was taken to balance between these conflicting constraints in this prototype.

Signal combining between the different down-conversion paths is performed at baseband to keep each path simple and to minimize any potential coupling between them. To accomplish this, the I and Q TIAs, which also set the bias points for the passive mixers, are biased close to the ground to minimize the on-resistance. To accommodate this, PMOS differential inputs are used in the TIAs. The input differential pairs are biased with low overdrive voltages and resistive loads and are also used in the first stage of the amplifier for a low flicker noise corner, which is found close to 100 kHz in simulation.

A block diagram of the multiphase LO generation circuit is shown in Fig. 3. A pseudo-differential delay-locked loop (DLL), shown in the inset of Fig. 3, splits a reference signal into 8 equally spaced phases. The 8 DLL outputs are buffered and sent into a resistive interpolation network, which averages out the phase errors from the DLL and outputs 16 phases. A two-level resistive interpolation is adapted from folding-and-interpolating ADCs for phase interpolation. The inputs to the interpolator are used to derive extra phases, and the original phases are then discarded, minimizing the amplitude-oriented phase errors between the LO signals [6]. The DLL and the interpolation network run at fLO/2 to maintain high phase accuracy and to save power. The interpolator outputs are edge-combined to produce 8 phases at fLO before being distributed to the mixer bank. All LO signals swing rail-to-rail to minimize the impact of transistor mismatch on LO phase accuracy and to decouple DLL cell delay from the magnitude of its output swing. A dynamic logic phase detector, adapted from [7], is used in the DLL to enable high-speed operation and to avoid systematic phase offsets commonly associated with high-frequency bang-bang phase detectors.

![Fig. 2. Single receive path (highlighted in Fig. 1 as well).](image)

![Fig. 3. LO generation circuit.](image)

![Fig. 4. Chip micrograph (90-nm CMOS, core area 1.92 mm²).](image)

**IV. MEASUREMENT RESULTS**

A test chip was implemented in a 1P8M 90-nm RF CMOS process, and the die photo is shown in Fig. 4. All pads are ESD protected, and all supply voltages are 1.2 V. This section summarizes the experimental results of the prototype.

**A. IQ Imbalance**

Figs. 5a and 5b show the measured IQ imbalance over gain and phase settings for one of the four down-converting VM channels. While the complex gain u scales proportionally to the gain setting, the gain mismatch and LO phase non-uniformity in the individual mixers are relatively constant, resulting in large IQ imbalance at a low gain setting (e.g., Au = 2.4 dB in Fig. 5). In contrast, the same mismatch affects the IQ balance much less significantly when the gain is large (e.g., Au = 15 dB in Fig. 5). IQ imbalance can degrade a receiver’s image rejection ratio (IRR), and the measured results of this prototype are shown in Fig. 5c. While receiver architectures such as Low-
IF and Weaver require high IRR for sufficient image rejection, an IRR of 20 dB is typically acceptable for direct-conversion receivers because the image is itself the signal mirrored. In this prototype, a > 20-dB IRR is achieved except for the lowest gain setting shown in Fig. 5, which is still useful in interference cancellation scenarios since a large interferer needs to be simply removed instead of demodulated.

B. Complex Gain Performance

The measured complex gain constellation of one VM channel is shown in Fig. 6. Measured and ideal data points are shown as filled and empty circles, respectively. Effects of IQ imbalance are averaged out to avoid any potential misinterpretation of the gain accuracy. Most of the complex gain errors are caused by the static offsets in the LO phases (the standard deviation of the LO phase offset was deduced to be approximately 2.8° based on the measured IQ mismatch and complex gain errors). The high resolution of the constellation results in a worst-case measured phase error of < 4.2° in gain setting, which includes both random and systematic errors (due to phase quantization), at a back-off of 4 dB from the maximum gain setting.

We define a metric for the complex gain accuracy, the EVM of the gain constellation, analogous to the EVM of the signal constellation used in communications:

$$\text{EVM} = \sqrt{\frac{\sum (u - u')^2}{\sum u^2}},$$  \hspace{1cm} (1)

where $u$ is the ideal complex gain, and $u'$ is the measured one. For the measured complex gain shown in Fig. 6, the overall EVM of the constellation is 2%, showing good adherence to the ideal constellation.

To further elaborate on the accuracy of the complex gain and phase, $u$ and $u'$ are decomposed into the amplitudes ($A_u$) and phases ($\theta_u$):

$$u = A_u e^{i\theta_u},$$

$$u' = (A_u + \Delta A_u) e^{i(\theta_u + \Delta \theta_u)},$$  \hspace{1cm} (2)

where $\Delta A_u$ and $\Delta \theta_u$ are the gain and phase errors associated with the measured gain $u'$. Fig. 7a shows the root-mean-square error (RMSE) of $u'$ with respect to $u$, and Figs. 7b and 7c show the relative amplitude and phase deviations of $u'$ from $u$ across different gain and phase settings, respectively. Though the RMSE is constant as a function of the gain, the relative gain/phase errors appear larger at small gain settings due to the un-scaling nature of the LO offsets mentioned earlier.
C. System Level Measurements

The measured responses of the four-channel VM receiver in phased-array mode (d = \lambda/2) set to broadside and when steered to a 60° scan angle are shown in Figs. 8a and 8b, respectively. The typical measured peak-to-null ratio is > 20 dB. The accuracy of this measurement was limited by the gain/phase-shifting accuracies of the plug-in, off-chip attenuators/phase shifters used in the experiment.

Figs. 9a and 9b demonstrate the measured interference cancellation of the VMs. An OFDM signal at 4 GHz represents the desired signal and another one placed 20 MHz away represents an interferer in the neighboring channel. Both the OFDM signal and the interferer are phase-shifted with passive off-chip components before being input into the VMs of the down-converter to mimic the effect of an interferer arriving from a different direction than that of the desired signal. The complex gains of two down-conversion paths are then set to actively cancel the interferer. The baseband output with one down-conversion channel on is shown in Fig. 9a. In contrast, when two channels are on, the interferer at the output of the VM is attenuated by 35 dB and the desired signal boosted by 4 dB, as shown in Fig. 9b. A worst-case cancellation of > 24 dB was observed over all tests in this case.

Table I summarizes the experimental results of the prototype chip measured at 4 GHz, which is the frequency of maximum gain. The use of passive mixers results in a high IIP2. At the same time, the IIP3 is eventually limited by the extra signal swing at the passive mixers’ outputs due to the isolation resistors, as pointed out earlier.

V. CONCLUSION

An inherently linear, four-channel beamforming IC with high gain resolution based on phase oversampling and coarse quantization is demonstrated. Accurate phase shifting is enabled by the VM architecture, achieving measured results of < 4.2° phase error at 4-dB gain back-off and > 24-dB interference cancellation without the use of fine resolution RFVGAs in the signal paths. The technique allows potentially more linear beamformers to be implemented in scaled CMOS without linear amplifying components.

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REFERENCES