17.6 A mm-Sized Wirelessly Powered and Remotely Controlled Locomotive Implantable Device

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Fully autonomous implantable systems with locomotion can revolutionize medical technology, and include applications ranging from diagnostics to minimally invasive surgery. However, the extreme power requirements of fluid locomotion impose significant design challenges. Using highly efficient and scalable electromagnetic propulsion systems [1], these locomotive devices become possible. Recent work shows that mm-sized antennas in tissue achieve optimal power transfer efficiency in the low-GHz range [2]. Combining this power transfer method with the highly efficient propulsion, a fully wireless locomotive implant capable of moving at 0.53cm/s has been realized in 65nm CMOS with a 2mm x 2mm receive antenna and a 0.6x1mm^2 die size with a 2W 1.86GHz carrier. The design consists of an RF frontend, bandgap reference, regulator, demodulator, digital control, and configurable high-current drivers for the propulsion system as shown in Fig. 17.6.1.

The fluid propulsion system operates with Lorentz forces on currents in a static magnetic field. Our prior work demonstrates significant advantages of such techniques in terms of power efficiency, scalability, and controllability [1]. There are two implementations: the first drives current directly through the fluid (magnetohydrodynamics or MHD), and the second switches current in a loop of wire to oscillate the device similar to a fin on a fish. The simulated performance of these methods is summarized in Fig. 17.6.2. Force is proportional to current, so maximizing current maximizes speed. There are 6 high-current drivers on-chip to control thrust and steering, and each has 4-bit configurability to accommodate both propulsion methods. Using MHD propulsion, the prototype achieves a speed of 0.53cm/s in 0.06T field while driving approximately 1mA and consuming roughly 300µW. Operating in a stronger magnetic field allows for higher forces and thus higher speeds.

The RF frontend includes an on-chip capacitive matching network and a 4-stage charge-pump connected rectifier. The matching network maximizes voltage at the rectifier input while driving the high-current propulsion system. The L-match consists of three CRTMOM capacitors to provide balanced-to-balanced load matching, and achieves an overall quality factor of Q=39, limited by the bond wires. This implies the capacitive matching network has an impressive Q-factor, outperforming on-chip inductors and transformers while requiring less area [3]. The matching network occupies 0.006mm^2, and is centered at 1.86GHz. Following the matching network, four synchronous self-driven rectifier stages similar to those in [1] produce 1.2V at the output of the last stage, with limiting diodes to prevent over-voltage. Figure 17.6.3 shows the link gain and the regulated output voltage. The propulsion speed increases with higher current, so to minimize power consumption it is driven from a large first rectifier stage, providing 0.5-2mA at 0.2V. However, this load dominates the input impedance, so adaptive loading was implemented to maintain match during both initial startup and normal operation, which is critical as the chip relies on continuous RF energy. The following three rectifier stages supply the 20µA necessary to power the active analog and digital circuits. The overall rectifier efficiency is estimated at 55%, and it occupies 0.3mm^2.

A bandgap reference and regulator provide a stable supply voltage for the chip, used for clock and data recovery as well as biasing for analog blocks. Based on work in [4], the bandgap reference produces a stable 0.3V reference. The design was modified to accommodate additional loading at the reference node, and consumes roughly 5µW. The bandgap reference incorporates large unit devices to minimize random variations and occupies 0.0025mm^2. The regulator employs a low-dropout architecture and relies on the reference voltage to down regulate the rectifier output to 0.7V. Linear regulators have smaller area and power overhead with less complexity than switching regulators, but suffer from lower efficiency. The losses compared to a switching regulator [5] translate to 5µW in this design, less than 2% of the total power budget.

The demodulator provides both the clock signal for the digital controller and decodes incoming data. With asynchronous pulse-width amplitude modulation, the demodulator operates at the highest tested rate of 25Mbps and consumes 0.5pJ/b, significantly outperforming comparable demodulators for implantable devices, consuming 13.2pJ/b [6]. The demodulator includes two rectifiers; the first has a short time constant and serves as the envelope detector, and the second has a long time constant and approximates the average of the envelope. These two signals feed to a comparator to generate the digital clock signal, and this clock is then integrated and compared to a threshold to decode the data signal. As a result, long pulses produce high output and short pulses produce low output. A schematic and description of the circuitry are shown in Fig. 17.6.4. The comparators consist of cascaded differential pairs sized for an input-referred offset of less than 5mV. The output stage of both comparators is a Schmitt-trigger inverter to output a full-swing digital data stream reliably with variation in process, temperature, and voltage. This receiver has robust performance over the entire testable received power range (-10 to +1.5dBm), and operates with as low as 9% modulation depth. Additionally, it functions over a wide range of data rates, reliably operating from 25Mbps down to 2.5Mbps in the current prototype. This robustness with environmental conditions and the wide range of data rates allow for its application in a variety of implantable systems. The entire receiver occupies 0.007mm^2, with 90% of this area occupied by capacitance. The circuit performance is summarized in Fig. 17.6.6.

The digital controller shown in Fig. 17.6.5 receives data and clock signals from the demodulator, and configures the propulsion system drivers. Data transmission begins with a 5-bit prefix that, when received, enables a shift register to begin accepting data. Data consists of 55-bit packets, and while data is being shifted into the register, the prefix detection circuitry is disabled. Once the data packet is received, the shift register pushes all the data to a memory register, which stores it until the next valid transmission. By only enabling the necessary circuitry in each stage of data reception, power consumption is minimized. Because the clock is derived from the data signal, when no data is being received the only current drawn is due to leakage. The estimated average power consumption of the digital controller while receiving data is 2µW, and it occupies 0.009mm^2.

This work has demonstrated a wirelessly powered implantable system capable of remotely controlled motion in fluid. This design achieves extremely low power consumption, and has very robust operation in a variety of environmental conditions in terms of power transmission, data transfer, and antenna separation and alignment. The designed circuits can also be adapted to a variety of implantable systems.

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[6] A. Ghenim, et al., "A full digital low power dpsk demodulator and clock recovery circuit for high data rate neural implants," *IEEE Int. Conf. on Electronics, Circuits, and Systems (ICECS),* pp. 571-574, Dec. 2010.

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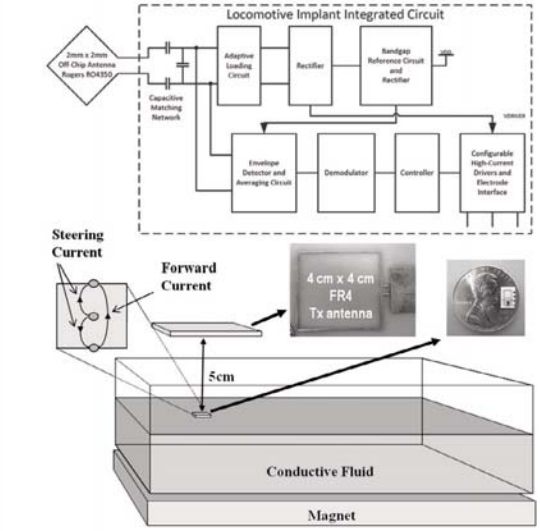

Figure 17.6.1: System-level block diagram of the implantable device, and magnetohydrodynamic propulsion experimental setup.

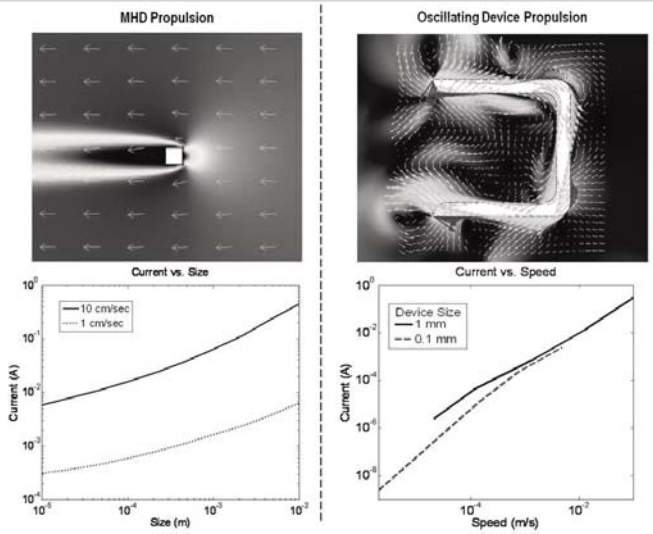

Figure 17.6.2: Performance summary of the electromagnetic propulsion mechanisms determined with numerical fluid simulations.

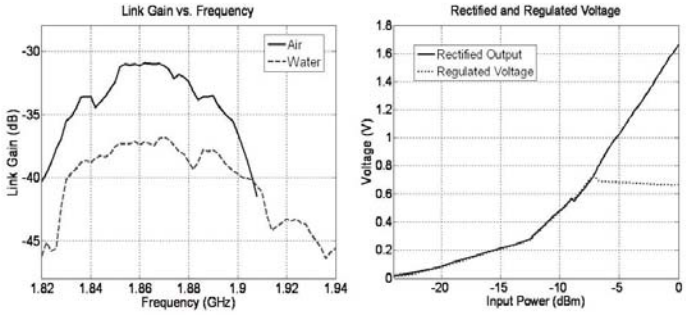

Figure 17.6.3: Measured link gain at the input of the antenna when in air and on top of water, and the rectified and regulated voltage as a function of input power.

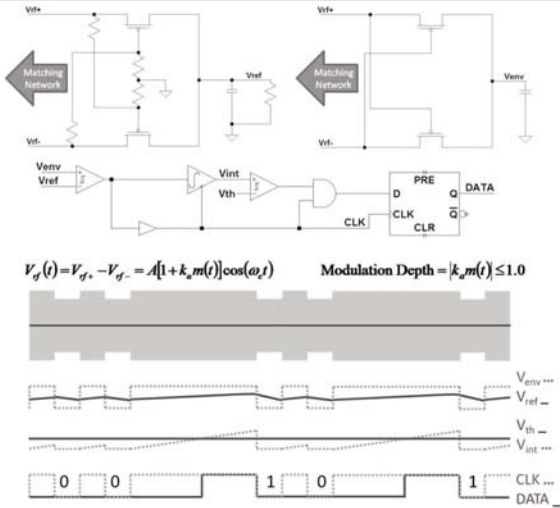

Figure 17.6.4: Demodulator schematic along with the description of the asynchronous pulse-width ASK modulation. The equation describes amplitude modulation, with modulation depth as defined.

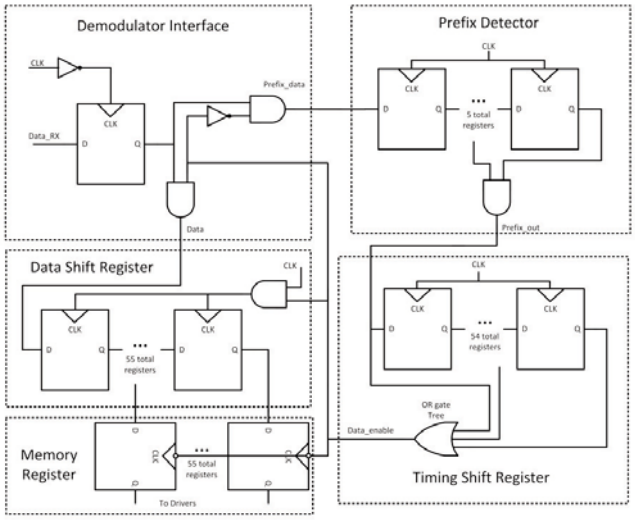

Figure 17.6.5: Digital controller schematic depicting the operation of the data receive circuitry.

Rectifier	
Rectifier Topology	1+3 Asynchronous Self-Driven
Load @ 0dBm	0.5-2mA @ 0.2V (unreg) 20μA @ 0.7V (reg)
Efficiency @ 0dBm	55%
Bandgap Reference and Regulator	
Bandgap Power Consumption	5μW @ 1.2V, 25°C
Regulator Efficiency	60%
PSRR	-20dB (@8.5MHz)
On-chip regulation capacitance	72pF
Bandgap Reference Chip Area	0.0025mm²
Demodulator	
Modulation Type	ASK + PWM
Carrier frequency	1.86GHz
Data Rate	2.5 – 25Mbps
Power Consumption	5μW @ 10Mbps
Sensitivity	-10dBm
Modulation Depth	≥90%
Energy per bit	0.5pJ/bit
Demodulator Chip Area	0.007mm²
Power Breakdown	
Bandgap Reference	5μW
Regulator	5μW
Demodulator	5μW
Digital Controller	2μW
Fluid Propulsion System	250μW*
Total	267μW

*Varies with input power and loading from propulsion

Figure 17.6.6: Measured performance summary of analog circuitry, and a breakdown of power consumption.

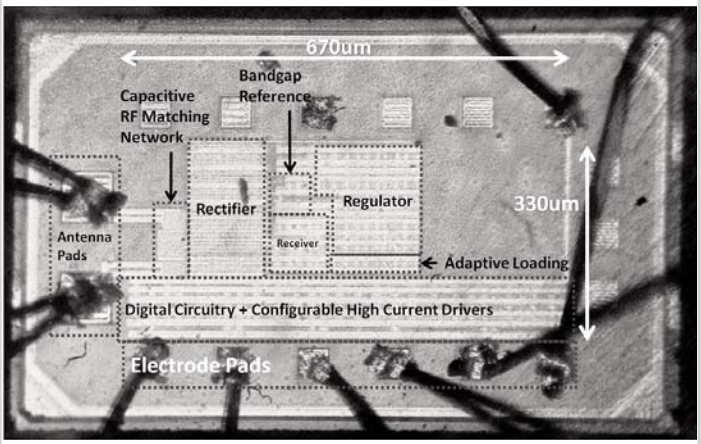

Figure 17.6.7: Chip die photo, total area including pads is 0.6mm^2.

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