A 60-GHz Digitally Controlled RF Beamforming Array in 65-nm CMOS with Off-Chip Antennas

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***Abstract*—An RF-path 60-GHz band 4-element array using proposed phase-oversampling vector modulation is implemented in 65-nm CMOS. Digitally controlled semi-lookup table method is proposed to compensate for non-idealities in circuits, antenna array, and interfaces. Accurate and high resolution control on the gain and phase is demonstrated. The receiver features an NF of 5.6 dB and 3.5^o phase resolution at a backoff of 3 dB. It dissipates 178mW from 1-V supply and obtains 18.5 dB gain for each channel.**

I. Introduction

Millimeter-wave systems can be a viable technology for imaging and multi-gigabit wireless network. Beamforming techniques are usually used to increase the directional antenna gain. There are several ways to do beamforming, including IF-path beamforming [1], LO-path beamforming [2] and RF-path beamforming [3-5]. IF-path beamforming is low loss but it requires LO distribution network and the physical size of passive devices is larger at IF frequency. LO-path beamforming also requires multiple mixers and LO distribution network, which potentially consume more power and larger area. RF-path beamforming, on the other hand, requires a small number of physical circuit elements, and potentially achieves higher SNR and SINR, as compared to IF and other beamforming techniques. Therefore, it provides a more scalable solution for both imaging and communication systems. The major challenge in RF beamforming is the implementation of low-loss, high-resolution, and small RF phase shifters. There are four basic types of RF phase shifters: switched line [3], reflection [4], loaded line, and vector modulation [5]. All can be designed using either distributed or lumped-elements to reduce area. Switched line, reflection, and loaded line suffer from insertion loss, phase error, and large area. Vector modulation is an active approach and consumes more power.

This work aims to provide a power efficient and low cost yet robust solution to the mm-Wave RF beamforming array. It applies the mathematical idea of oversampling and coarse quantization to devise a new phase-shifter architecture that addresses the challenges. The new phase shifters are integrated into a 4-element receiving array in 65-nm CMOS with off-chip patch antennas. Algorithms are developed to utilize the high phase resolution to compensate non-idealities and variations of RF circuits and antenna paths.

The rest of this paper is organized as follows. Section II gives the detailed design of the receiver. Section III presents tested results. Finally, we conclude this paper in Section IV.

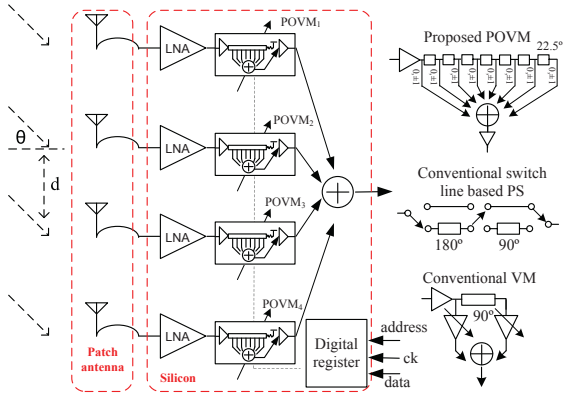

Fig. 1. 4-element beamforming receiver front end architecture based on proposed phase oversampling vector modulator (POVM) technique

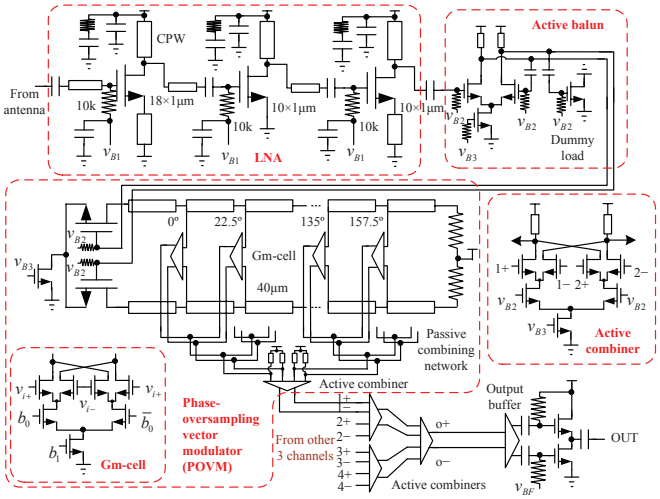

Fig. 2. Schematic of the 4-element receiver front end based on POVM

II. Beamforming Receiver Front End Design

A. The 4-Element Receiver Front End Principle

Fig. 1 shows the architecture of the 4-element beamforming receiver front end. In conventional vector modulation (VM), the complex gain coefficient $B_k\angle -\phi_k$ is achieved by weighted combinations of I/Q paths (Nyquist sampling in phase) using high-resolution VGAs, which are power hungry. Here B_k and $-\phi_k$ are the amplitude and phase settlings of the k-th

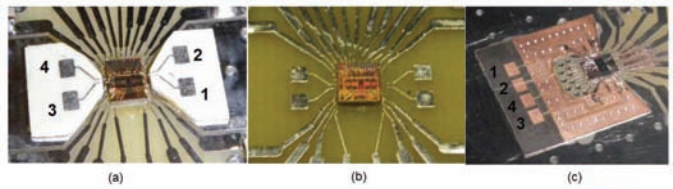

Fig. 3. Antenna design and integration in different substrates:(a)20 mil RO4003 (b)62 mil FR4 (c)5 mil RT5880

branch beamformer. In contrast, we propose to use a bank of low-resolution VGAs taking discrete values of (0, $\pm$1). RF phase shifting is achieved by weighted combinations of phase-oversampling vector paths as illustrated in Fig. 2. The complex gain of the proposed phase-oversampling VM is given by

$$B_k \angle -\phi_k = \sum_{m=0}^{M-1} b_{k,m} e^{j\frac{m\pi}{M}}, \quad b_{k,m} \in \{0, \pm 1\} \qquad (1)$$

where $M/2$ is the phase oversampling rate. Larger M yields higher phase resolution. This work chooses M equal to 8 which yields 3^8 possible complex gains. Due to the use of low-resolution VGAs, the phase-oversampling VM is more power efficient than the conventional VM.

B. Detailed Circuit Design

The phase oversampling VM follows a three-stage common source based LNA. The LNA uses high Q CPW lines with slotted ground and is optimized using NF_{min} current density method [6]. For standalone LNA, MOM capacitive divider is used for output matching.

The delay line in the VM is implemented by differential microstrip line (MSL) with slotted ground. High Z_c of 100 Ω is chosen for high power efficiency. Conventionally CPW has better Q and more design parameters than MSL. However, MSL is more compact and area efficient considering that POVM has eight taps to provide eight discrete phases up to 157.5°. In addition, the MSL ground can be slotted to provide additional design parameters. By increasing the slot width without reducing the signal-line width, Z_c is increased and Q is also increased. Phase coverage of 360° is achieved by using differential operation. In this work, we use 8 vector taps.

The low-resolution VGAs connected to each tap use current commuting topology to reduce the drain parasitic capacitance loss and are controlled by digital registers (Fig. 2). Oversampling vector paths are first combined by MSL-based passive network and the final combining is implemented using active combining network. The four channels are also combined using active combining network. The buffer in the final stage provides output matching and differential to single-ended conversion (D-to-SC).

C. Antenna Array Design

We experimented on several designs of the antenna array (Fig. 3). One of them is a planar array based on 20 mil RO4003 substrate, as shown in Fig. 3(a). Two patch antennas sit at the two sides of the chip. For the patch antennas designed in the 5 mil RT5880 substrate as shown in Fig. 3(c), the patch element

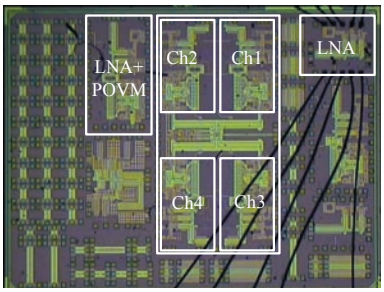

Fig. 4. Die photograph of the receiver chip

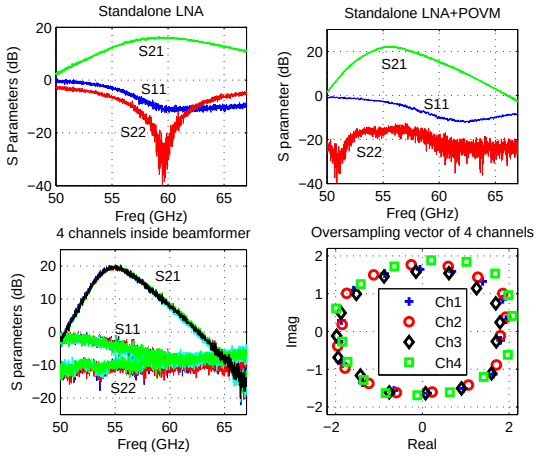

Fig. 5. S parameter measurements

distance is $\lambda_0/2$. It has smaller total gain than RO4003 based antenna due to long feed line effect. FR4 based antenna array is also experimented which has the lowest cost but also the lowest gain, as shown in Fig. 3(b). In the following paper, we only show the measurement results on RO4003 antenna array.

D. Post Correction Algorithm Design

In order to compensate errors caused by the non-ideal effects, algorithms are proposed in this work. The goal is to find the control bits $b_{k,m} \in \{0, \pm 1\}$ that minimize $|P_k - \sum_{m=0}^{M-1} b_{k,m} e^{j\frac{m\pi}{M}}|$, where P_k is the complex gain point we want for the k-th branch. Semi-lookup table method is used in this paper. We store *only* the oversampling vector paths in a table and then we search the best coefficients using (1). Compared to the conventional method, it does not need a big table to store all the constellation points. The effectiveness of this method will be demonstrated in Fig. 8.

III. Circuit Test Results

The receiver is implemented in TSMC 1P9M 65-nm CMOS (Fig. 4). Fig. 5 shows the measured S-parameters for standalone LNA, standalone LNA plus POVM, and one channel of the beamforming receiver. Fig. 6 shows the NF measurement. The test setup for NF measurement comprises of a V-band noise source, isolators, preamplifiers, and a 67-GHz spectrum analyzer (SA). Both Y-factor method and built-in method in the SA are used over several test boards. For the whole receiver including antennas, a rotation arm with 24-dBi horn antenna

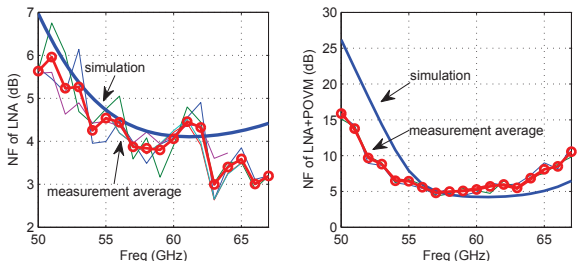

Fig. 6. NF measurements

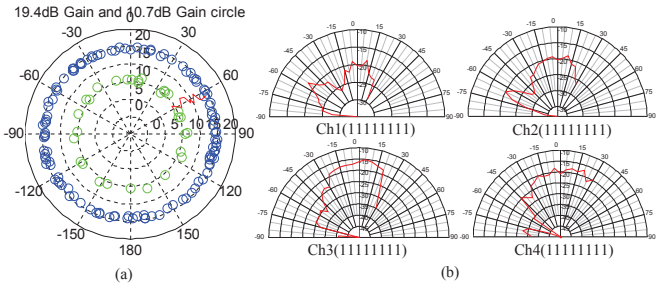

Fig. 7. Constellation and each channel beam pattern in dB

placed 32.5 cm above the receiver is built and mounted directly on the probe station to test the beam pattern. Due to physical constraint, we can only measure the angles from -90^o to 30^o.

A. Standalone Low Noise Amplifiers Tests

At 59 GHz, the gain of the standalone LNA including pads effect is 16.2 dB, the average NF is 3.8 dB, and the power consumption is 8.3 mW with 8.7 GHz 3-dB bandwidth.The S_{11} is -10 dB, and S_{22} is about -23 dB. S_{12} is below -30 dB. Power compression is measured by using the 67-GHz Agilent PNA power sweep function. The Pre-DUT loss is considered and together with the measured gain curve, we find P_{1dB}. The measured OP_{1dB} is -4.85 dBm.

B. LNA plus Phase Oversampling VM Tests

For the standalone LNA plus phase-oversampling VM, S_{11} is -4 dB, S_{21} is 22.2 dB, and S_{22} is -16 dB at 56 GHz when all the 8 oversampling vector paths are on (11111111), as shown Fig. 5. The average NF is 5.6 dB at 56 GHz

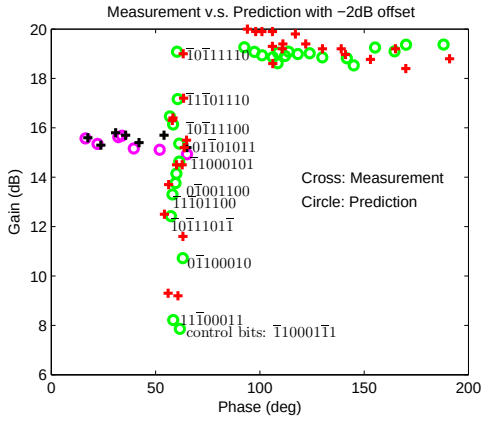

Fig. 8. Measurement constellation and algorithm prediction comparison

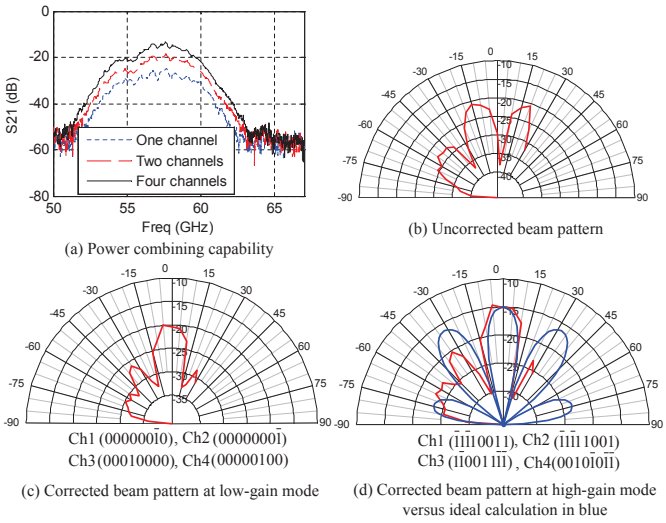

Fig. 9. Power combining and measured beam pattern correction

and 4.9 dB at 57 GHz (Fig. 6). It draws 33.3 mA from 1-V supply with 3-dB bandwidth of 4.2 GHz. The measured OP_{1dB} is -15 dBm. The output D-to-SC buffer is estimated to consume 2.7 mA and has -4.4 dB gain with OP_{1dB} of -3.2 dBm at 56 GHz. After de-embeding the D-to-SC buffer effect, OP_{1dB} is -10.3 dBm. For each oversampling vector path (00000001, 00000010 ... to 10000000), the gain varying from 9.5 dB to 11.2 dB with NF varying from 7.5 dB to 6.8 dB across the 8 vectors at 56 GHz. Phase resolution is derived from the total constellation based on the measured oversampling vector paths. Assuming 5% gain variation, 3.5° phase resolution is achieved at a back-off of 3 dB. Fig. 7 also shows the measured two constant-gain point circles. Only partial constellation points are shown especially for the low-gain circle (green points). The trajectory when we want to move one gain circle to another without changing the phase is also shown (red curve). Fine tuning can be used to make the trajectory more smooth in phase. The control bits are obtained based on the proposed algorithms. Fig. 8 shows the comparison of the measured constellation versus the algorithm prediction with -2 dB gain offsets. As shown, the phase is accurate while the gain is lower due to gain compression, especially in the high-gain mode.

For one channel inside the beamformer, the gain is 18.5 dB with 0.5 dB mismatches at 56 GHz across the four channels and OP_{1dB} is about -15 dBm before D-to-SC buffer de-embeding. Fig. 5 also shows the measured complex gain on each oversampling vector path for each channel of the receiver with RF probes. As expected, there are slight variations among the four channels. The bandwidth is 3.4 GHz. The whole beamforming receiver consumes 178 mW of power.

C. 4-Element Receiver Front End Tests

After antenna assembly, the peak frequency is shifted to 57 GHz (see Fig. 9(a)). Fig. 7 shows the beam pattern of each channel at 57 GHz. As shown, there are significant variations due to the difference in patch antennas, feed lines, bond wires,

TABLE I
CHIP PERFORMANCE SUMMARY WITH OUTPUT D-TO-SC BUFFER LOSS DE-EMBEDED

Ref	Tech	Freq (GHz)	Gain (dB)	NF (dB)	V_{dd} (V)	Power (mW)	OP_{1dB} (dBm)	Area (mm^2)	BW (GHz)	Phase Resol.	Topology
One Channel in RF Beamforming Receiver Front End											
This work	65nm CMOS	56	22.9	5.6	1	178, 4 channels	-10.4	3.40	3.4	3.5^o	Active combiner
Intel [3]	90nm CMOS	58	8	7.7	1.3	52, 4 channels	-11	1.04	2.6	90^o	Wilkinson combiner
IBM [4]	0.13um SiGe	60	14	6	2.7	48.6, 2 channels	-9	3.90	n.a.	11.25^o	Wilkinson combiner
NXP [5]	65nm CMOS	61	12	7.2	1.5	156, 2 channels	-5	1.60	5	22.5^o	Active combiner
Standalone LNA											
This work	65nm CMOS	59	16.2	3.8	1	8.3	-4.85	0.38	8.7	–	3-stage CS, CPW
Intel [7]	90nm CMOS	58	15	4.4	1.3	3.9	-4	0.14	6	–	3-stage CS, lumped inductor
RUB [8]	65nm CMOS	59	22.3	6.1	1.2	34.8	2.7	0.21	7.7	–	2-stage cascode, transformer
Phase Shifter Estimated From Standalone LNA+POVM											
This work	65nm CMOS	56	13.4	13	1	25	-10.3	0.13	4.2	3.5°	Phase oversampling vector modulator
Intel [3]	90nm CMOS	58	6.5	n.a.	1.3	n.a.	n.a.	0.032	–	90^o	Switched delay, HP/LP config
IBM [9]	0.13um SiGe	60	-5.5	16	2.7	16.2	-8	0.25	–	11.25^o	RTPS + balun + PIVGA
NXP [5]	65nm CMOS	61	0	n.a.	1.5	19.5	-9	0.043	–	22.5^o	IQ vector modulator

and placement of the horn antenna. Spatial power combining is demonstrated by turning on one, two, and four channels respectively, as shown in Fig. 9(a). We use the algorithm to select the control bits so that each channel gain and phase is equalized. At 56 GHz, the measured S_{21} is -28.17 dB, -22.89 dB, and -18.18 dB respectively for the four cases. The increments are 5.28 dB and 9.99 dB respectively relative to single channel gain.

Fig. 9(b)(c)(d) show examples on the beamforming pattern before and after algorithmic correction. It illustrates that the effectiveness of beamforming is greatly limited by the variations across channels. The measured uncorrected beam pattern has a null in the 0-degree direction. An important advantage of our architecture is using the algorithm to select the correct control bits to finely adjust both the phase shift and gain of individual channel, and hence compensate for the differences across channels. After correction, the beam pattern has a peak at the 0 degree. We also capture the side lobes in the measurement which is due to the non ideal ($> 0.5\lambda_0$) RO4003 patch antenna placement. Fig. 9(d) also includes the ideal pattern (the blue curve).

Different gain modes are also experimented. As already shown in Fig. 7, we can select the same phase at different gain circles. In Fig. 9(c)(d), two beam patterns are obtained based on the algorithm. As shown, they have similar shapes on the beam pattern but different gains.

IV. CONCLUSIONS

Table 1 summaries the chip performance of this work. New architectures and new design techniques are proposed. Compared with state-of-the-art implementations, this work achieves high power efficiency, low NF with high gain, and good phase resolution in CMOS. Algorithms are proposed to select the control digital bits, making it suitable to compensate the non-ideal effects of chip-to-antenna interfaces adaptively. The proposed techniques can be applied to other mm-Wave applications.

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