# EE114/EE214A, Autumn 2017

## Course Information

**General Information**
Course: EE114/EE214A, Fundamentals of Analog Integrated Circuit Design
Lectures: Tue & Thu, 10:30–11:50am, Gates B01
Review Session: Fri, 12:30 pm – 1:20 pm, Gates B03
Units: 3-4 (Undergraduates must take EE114 for 4 units)
Prerequisite: EE101B
Website: https://canvas.stanford.edu/courses/68820

Check website for updated information regarding office hours, review sessions etc. We will use this website for posting lecture notes, homeworks, and grades. Major announcements will be emailed. Please plan ahead and make use of TA office hours in order to resolve other issues and use TA emails mainly for simple and quick questions with "EE114/EE214A" in the email's subject. Piazza will also be available for student-to-student assistance although it won't replace office hours since the teaching staff will sparingly review the activity on Piazza. However, this doesn't mean you can use Piazza in order to "check" answers to homework questions, as we expect everyone to abide by Stanford's honor code.

**Course Description**
Analysis and simulation of elementary transistor stages, current mirrors, supply- and temperature-independent bias, and reference circuits. Overview of integrated circuit technologies, circuit components, component variations and practical design paradigms. Differential circuits, frequency response, and feedback will also be covered. Performance evaluation using computer-aided design tools.

**Instructor**
Jayant Charthad
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**Administrator**
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**Teaching Assistants**
Ajay Singhvi (asinghvi@stanford.edu)
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Office hours: Check course website

**Recommended Texts**
1. B. Murmann, *Analysis and Design of Elementary MOS Amplifier Stages*, National Technology and Science Press, to appear in 2011.
2. P. R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th Edition, Wiley, 2009

**Grading**
1. Homework – 25% (Drop lowest score)
2. Midterm Exam – 25%
3. Project – 20%
4. Final Exam – 30%

**Piazza**
Occasionally we will be using Piazza as our online forum for posting clarifications to assignments. However,

it is meant to be a forum for students to interact among themselves, with minimal participation by the TAs or course instructor. **Extra credit** will be given to the students with the highest participation in answering questions. We highly recommend attending at least one TA office hour session per week in order to clarify any issues you have with assignments.

**Honor Code (*VERY IMPORTANT)**
Please do not treat Piazza as a way of "checking" answers to homework questions, as we expect everyone to abide by Stanford's honor code. Just as a reminder, the honor code applies to all parts of all classes; more information can be found at:
https://communitystandards.stanford.edu/student-conduct-process/honor-code-and-fundamental-standard#honor-code

**Students with Disabilities**
Students with Documented Disabilities: Students who may need an academic accommodation based on the impact of a disability must initiate the request with the Office of Accessible Education (OAE). Professional staff will evaluate the request with required documentation, recommend reasonable accommodations, and prepare an Accommodation Letter for faculty. Unless the student has a temporary disability, Accommodation letters are issued for the entire academic year. Students should contact the OAE as soon as possible since timely notice is needed to coordinate accommodations. The OAE is located at 563 Salvatierra Walk (phone: 723-1066, URL: https://oae.stanford.edu/).

**Homework Submission**
**Homework will be handed out on Thursday and will be due the following Thursday at 11:59pm sharp, unless otherwise stated**. All students (on-campus and SCPD) should submit their homework electronically by uploading it through Canvas. Do not email your homework to the teaching staff.

**Course Schedule – see next page**

**Course Schedule**

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| Week 1 | 9/26, 9/28 | Introduction, IC Technology, Long Channel MOS Model, Common Source Amp, Small Signal Model | HW1 out |
| Week 2 | 10/03, 10/05 | Gain and Bias considerations, Finite Output Resistance, Intrinsic capacitance, Extrinsic Capacitance | HW1 due, HW2 out |
| Week 3 | 10/10, 10/12 | Miller, ZVTC Dominant Pole Approx., Backgate Effect, Common Gate Stage | HW2 due, HW3 out |
| Week 4 | 10/17, 10/19 | Common Drain Amp., PVT Variation and Mismatch, Current Mirrors, Voltage Biasing Considerations | HW3 due, HW4 out |
| Week 5 | 10/24, 10/26 | Differential Pair, Supply Insensitive Bias Current Generation, Introduction to BJTs | HW4 due, HW5 out |
| Week 6 | 10/31, 11/02 | Bandgap References, Multi-stage Amplifiers (I) MIDTERM (11/02, 5:30-7:00pm, 370-370) | Project out |
| Week 7 | 11/07, 11/09 | Multi-stage Amplifiers (II), Intro to Feedback, Ideal Feedback Configurations, Design Problem Examples | HW5 due |
| Week 8 | 11/14, 11/16 | Feedback with 2-port Networks, Practical Feedback, Return Ratio, Port Impedances using Return Ratio | Project Check point, HW6 out |
| Week 9 | 11/21, 11/23 | Thanksgiving Recess (No classes! We recommend getting started on the Project early!) | |
| Week 10 | 11/28, 11/30 | Feedback and Stability, OTA Feedback Circuits, Miller Compensation | HW6 due, Project Netlist due, HW7 out |
| Week 11 | 12/05, 12/07 | Advanced OTA Topologies, Analog Layout Considerations | Project Report due, HW 7 due |
| Week 12 | 12/13 (Wed) | FINAL EXAM (12:15pm-3:15pm, Location TBD) | |