CMOS Op-amp Design and Optimization via Geometric Programming

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CMOS analog amplifier design

problem: choose transistor dimensions, bias currents, component values

- critical part of mixed-mode (digital-analog) ICs
- for typical mixed-mode IC,
  - 1:10 analog:digital area
  - 10:1 analog:digital design time

this talk: a **new method** for CMOS op-amp design, based on **geometric programming**

- **globally optimal** and **extremely fast**
- handles wide variety of practical constraints & specs

Outline

- Geometric programming
- Two-stage op-amp
- MOS models
- Constraints & specs
- Design examples & trade-off curves
- Extensions
- Conclusions

Monomial & posynomial functions

$x = (x_1, \ldots, x_n)$: vector of positive variables

function g of form

$$g(x) = x_1^{\alpha_1} x_2^{\alpha_2} \cdots x_n^{\alpha_n},$$

with $\alpha_i \in \mathbf{R}$, is called **monomial**

function f of form

$$f(x) = \sum_{k=1}^{t} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \cdots x_n^{\alpha_{nk}},$$

with $c_k \geq 0$, $\alpha_{ik} \in \mathbf{R}$, is called **posynomial**

- posynomials closed under sums, products, nonnegative scaling
- monomials closed under products, division, nonnegative scaling
- if $1/f$ is posynomial we say f is **inverse posynomial**

examples:

- $0.1 x_1 x_3^{-0.5} + x_2^{1.5} x_3^{0.7}$ is posynomial
- $1/(1 + x_1 x_2^{1.3})$ is inverse-posynomial
- $2x_3\sqrt{x_1/x_2}$ is monomial (hence also posy. & inv-posy.)

Geometric programming

a special form of optimization problem:

$$\begin{array}{ll} \text{minimize} & f_0(x) \\ \text{subject to} & f_i(x) \le 1, \quad i = 1, \ldots, m \\ & g_i(x) = 1, \quad i = 1, \ldots, p \\ & x_i > 0, \qquad i = 1, \ldots, n \end{array}$$

where f_i are posynomial and g_i are monomial more generally with geometric programming we can

- **minimize** any posynomial or monomial function, or
- **maximize** any inverse-posynomial or monomial function

subject to any combination of

- **upper bounds** on posynomial or monomial functions
- **lower bounds** on inverse-posynomial or monomial functions
- **equality constraints** between monomial functions

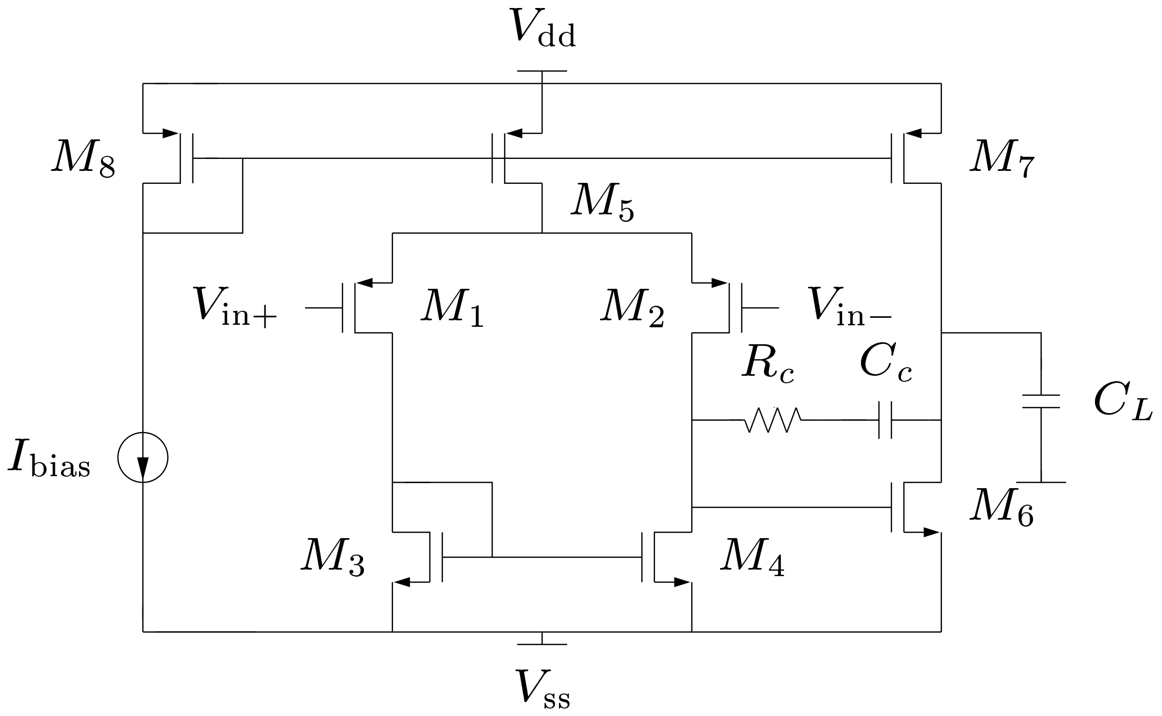
Geometric programming: history & methods

- used in engineering since 1967 (Duffin, Peterson, Zener)
- used for digital circuit transistor sizing with Elmore delay since 1980 (Fishburn & Dunlap's TILOS)

new (interior-point) methods for GP ($e.g.$, Kortanek et al)

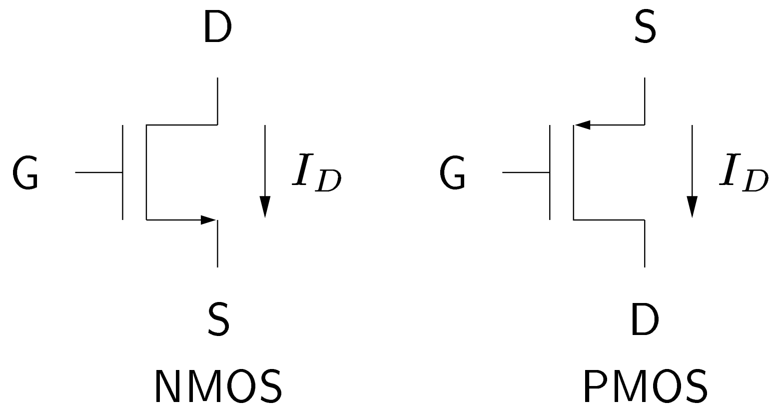
- are **extremely fast**
- handle medium and large-scale problems
(100s vbles, 1000s constraints easily solved on PC in minutes)
- either find **global optimal** solution, or provide **proof of infeasibility**

Two-stage op-amp



- common op-amp architecture
- 19 **design variables:** $W_1, \ldots, W_8$, $L_1, \ldots, L_8$, R_c, C_c, I_{bias}

Large signal MOS model



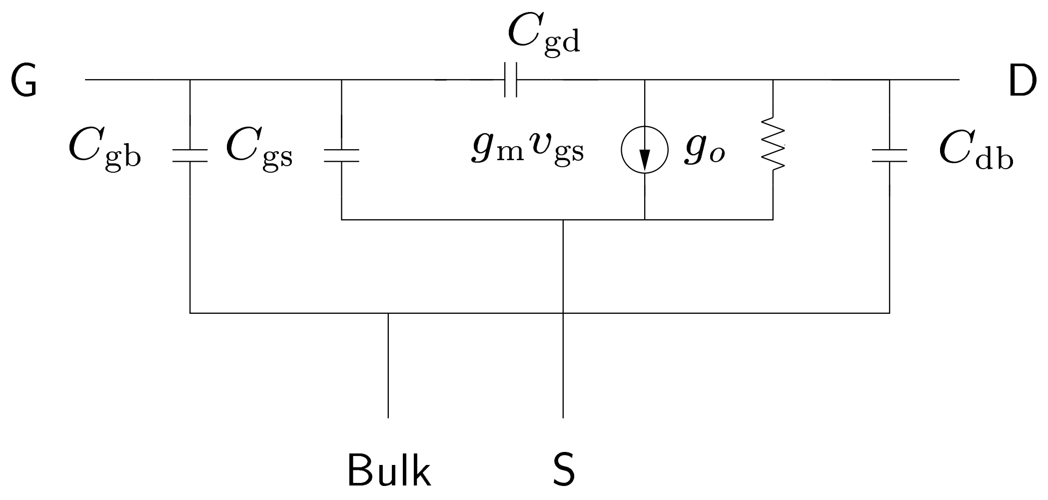
NMOS **saturation condition:** $V_{\mathrm{DS}} \geq V_{\mathrm{GS}} - V_{\mathrm{TN}}$

square-law model $I_D = k_1(W/L)(V_{\mathrm{GS}} - V_{\mathrm{TN}})^2$

similar condition & model for PMOS

(more accurate model possible, *e.g.*, for short channel)

Small signal dynamic MOS model



transconductance and output conductance,

$$g_m = k_2 \sqrt{I_D W/L}, \qquad g_o = k_3 I_D$$

are **monomial** in W, L, I_D

capacitances are all (approximately) posynomial in W, L, I_D

Dimension constraints

limits on device sizes:

$$L_{\min} \leq L_i \leq L_{\max}, \qquad W_{\min} \leq W_i \leq W_{\max}$$

(express as $L_i/L_{\max} \leq 1$, etc.)

symmetry constraints: $W_1 = W_2$, $L_1 = L_2$, $W_3 = W_4$, $L_3 = L_4$

bias transistor matching: $L_5 = L_7 = L_8$

to reduce systematic input offset voltage:

$$\frac{W_3/L_3}{W_6/L_6} = \frac{W_4/L_4}{W_6/L_6} = \frac{W_5/L_5}{2W_7/L_7}$$

area $= \alpha_1 C_{\mathrm{c}} + \alpha_2 \sum_i W_i L_i$ is posynomial, hence can impose upper limit

Bias constraints

each transistor must remain in saturation over specified

- common-mode input range $[V_{\rm cm,min}, V_{\rm cm,max}]$
- output voltage swing $[V_{\rm out,min}, V_{\rm out,max}]$

leads to four **posynomial inequalities**

$e.g.$, for M_5 we get

$$k_4\sqrt{\frac{I_1L_1}{W_1}} + k_5\sqrt{\frac{I_5L_5}{W_1}} \leq V_{\rm dd} - V_{\rm cm,max} + V_{\rm TP}$$

(every drain current is monomial in the design variables)

Quiescent power & slew rate specs

quiescent power is posynomial:

$$P = (V_{\mathrm{dd}} - V_{\mathrm{ss}})(I_{\mathrm{bias}} + I_5 + I_7)$$

hence can impose upper limit on power (or minimize it)

slew rate is

$$\min\left\{\frac{2I_1}{C_{\mathrm{c}}},\ \frac{I_7}{C_{\mathrm{c}} + C_{\mathrm{L}}}\right\}$$

min slew rate spec can be expressed as posynomial inequalities

$$\frac{C_{\mathrm{c}}\mathrm{SR}_{\mathrm{min}}}{2I_1} \leq 1, \qquad \frac{(C_{\mathrm{c}} + C_{\mathrm{L}})\mathrm{SR}_{\mathrm{min}}}{I_7} \leq 1$$

Transfer function

with standard value $R_c = 1/g_{\rm m6}$, TF is accurately given by

$$H(s) = \frac{A_v}{(1+s/p_1)(1+s/p_2)(1+s/p_3)(1+s/p_4)}$$

- open-loop gain is **monomial**: $A_v = k_6\sqrt{W_2W_6/L_2L_6I_1I_7}$
- dominant pole p_1 is **monomial**: $p_1 = g_{\rm m1}/A_vC_c$
- parasitic poles $p_2,\ p_3,\ p_4$ are **inverse posynomial**

hence can fix the open-loop gain and dominant pole, and lower bound the parasitic poles

3 dB bandwidth and unity gain crossover specs

- **bandwidth constraints:** $|H(j\omega)| \geq a$ for $\omega \leq \Omega$

$$\Leftrightarrow \; |H(j\Omega)|^2 = \frac{A_v^2}{(1+\Omega^2/p_1^2)(1+\Omega^2/p_2^2)(1+\Omega^2/p_3^2)(1+\Omega^2/p_4^2)} \geq a^2$$

$$\Leftrightarrow \; (a^2/A_v^2)(1+\Omega^2/p_1^2)(1+\Omega^2/p_2^2)(1+\Omega^2/p_3^2)(1+\Omega^2/p_4^2) \leq 1$$

. . . a posynomial inequality (since p_i are inv.-pos.)

- **unity gain crossover** is (very accurately) monomial: $\omega_{\rm c} = g_{\rm m1}/C_{\rm c}$
- hence can fix (or upper or lower bound) crossover frequency

Phase margin specs

min phase margin spec is:

$$-\angle H(j\omega_c) = \sum_{i=1}^{4} \arctan(\omega_c/p_i) \leq \pi - \mathrm{PM}_{\min}$$

extremely good approximation:

$$\sum_{i=2}^{4} \omega_c/p_i \leq \pi/2 - \mathrm{PM}_{\min}$$

(since p_1 contributes 90°, and $\arctan(x) \approx x$ for $x \leq 50^\circ$)

. . . a **posynomial inequality** since parasitic poles are **inverse posynomial**

Other specs

- min common-mode rejection ratio
- min (pos. & neg.) power supply rejection ratios
- max spot noise at any frequency
- max total RMS noise over any frequency band
- min gate overdrive

can all be handled by geometric programming

Summary

using **geometric programming** we can **globally optimize** a design involving all the specs described above:

- dimension constraints, area
- bias constraints, power, slew rate
- bandwidth, crossover frequencies, phase margin
- CMRR, nPSRR, pPSRR
- spot & total noise

typical problem:

- approx 20 vbles, 10 equality & 20 inequality constraints
- solution time ≈ 1 sec (inefficient Matlab implementation!)

(Globally) optimal trade-off curves

- fix all specs except one ($e.g.$, power)
- optimize objective ($e.g.$, maximize crossover frequency) for different values of spec
- yields **globally optimal** trade-off curve between objective and spec (with others fixed)

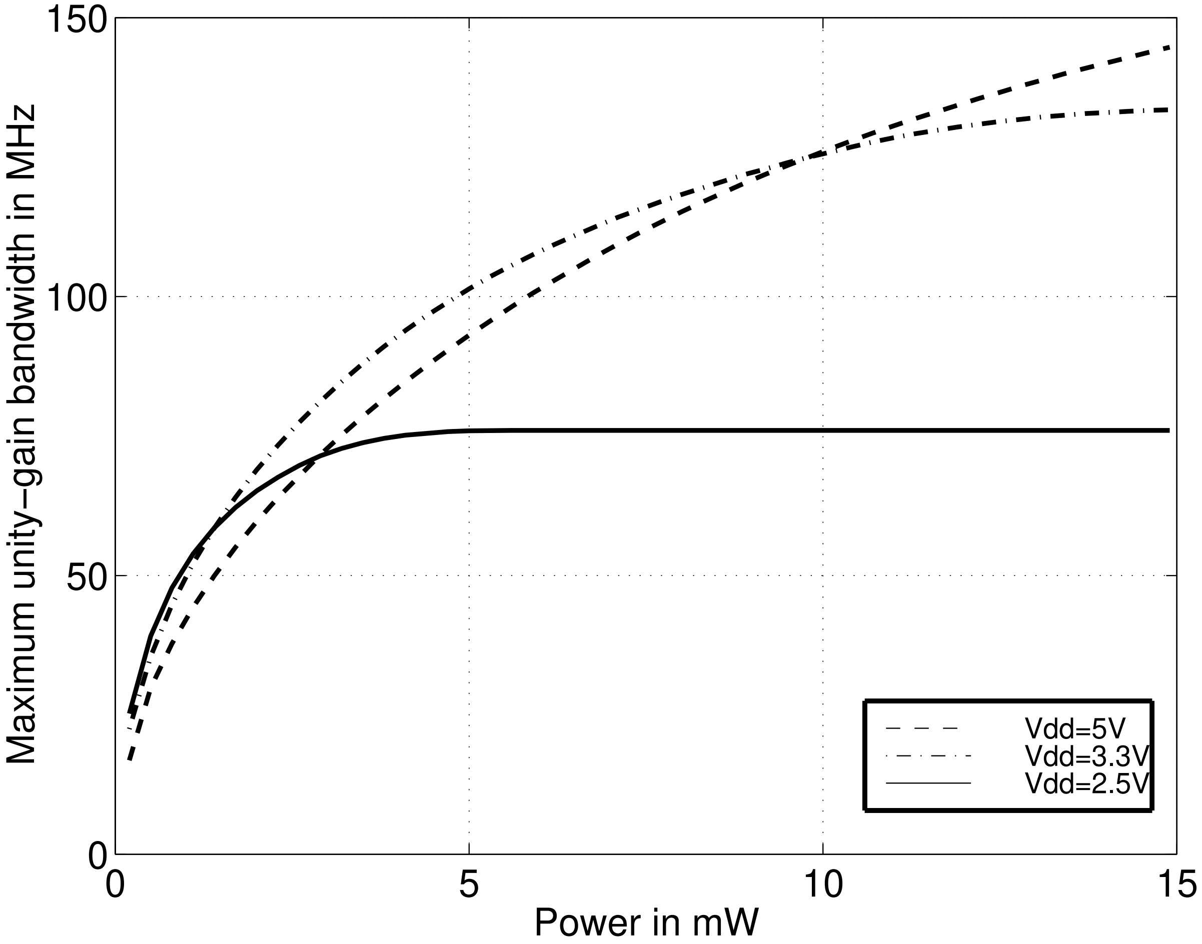
Default specs

our examples will maximize crossover BW with default specs

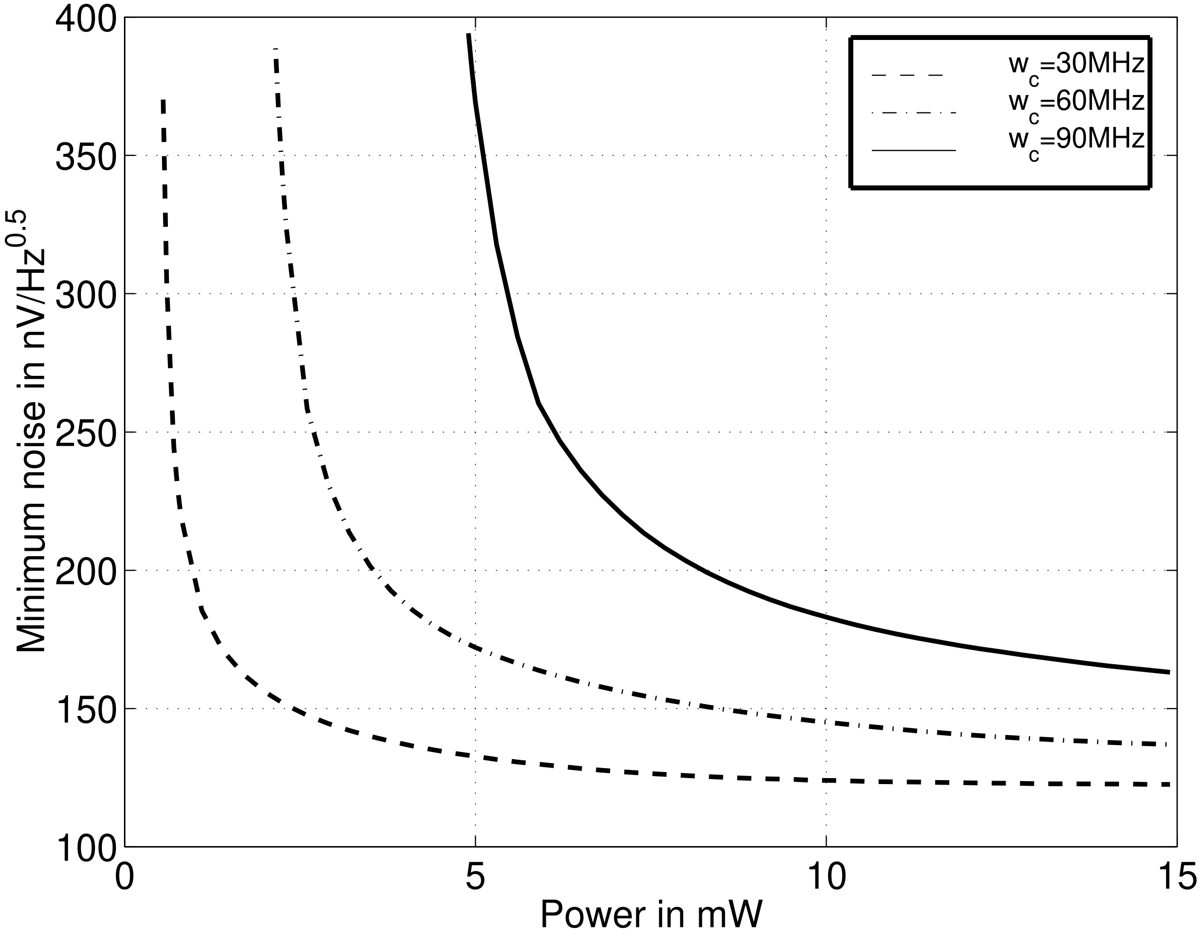
- $V_{\mathrm{dd}} = 5$V, $V_{\mathrm{ss}} = 0$V, 1.2μm process
- $L_i \geq 0.8\mu\mathrm{m}$, $W_i \geq 2\mu\mathrm{m}$, area $\leq 10000\mu\mathrm{m}^2$
- CM input fixed at mid-supply; output range is 10%–90% of supply
- power $\leq 5\mathrm{mW}$
- open-loop gain ≥ 80dB, PM $\geq 60^\circ$
- slew rate $\geq 10\mathrm{V}/\mu\mathrm{sec}$
- CMRR ≥ 60dB
- input-referred spot noise $(1$kHz$)$ $\leq 300\mathrm{nV}/\sqrt{\mathrm{Hz}}$

(we'll vary one or more to get trade-off curves)

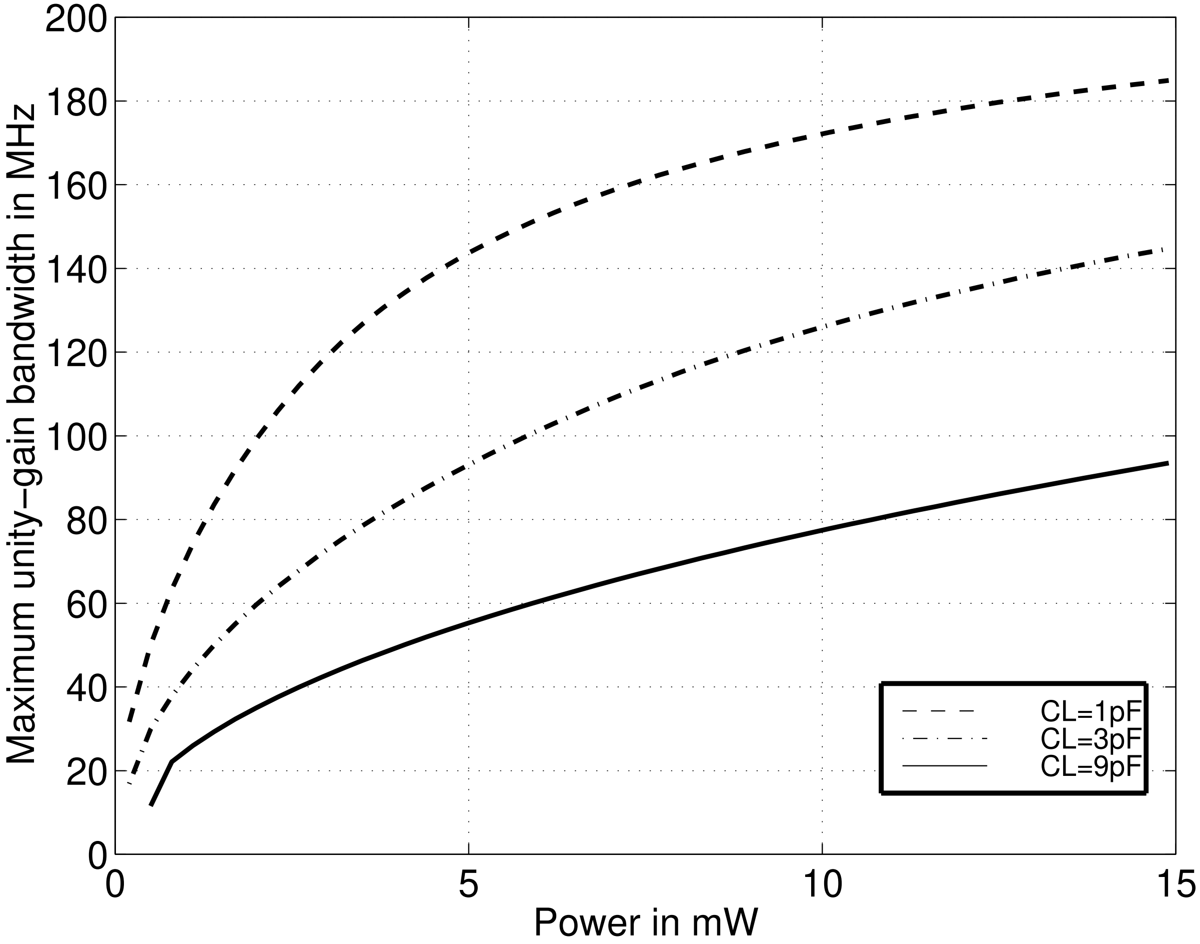
Maximum BW versus power & supply voltage



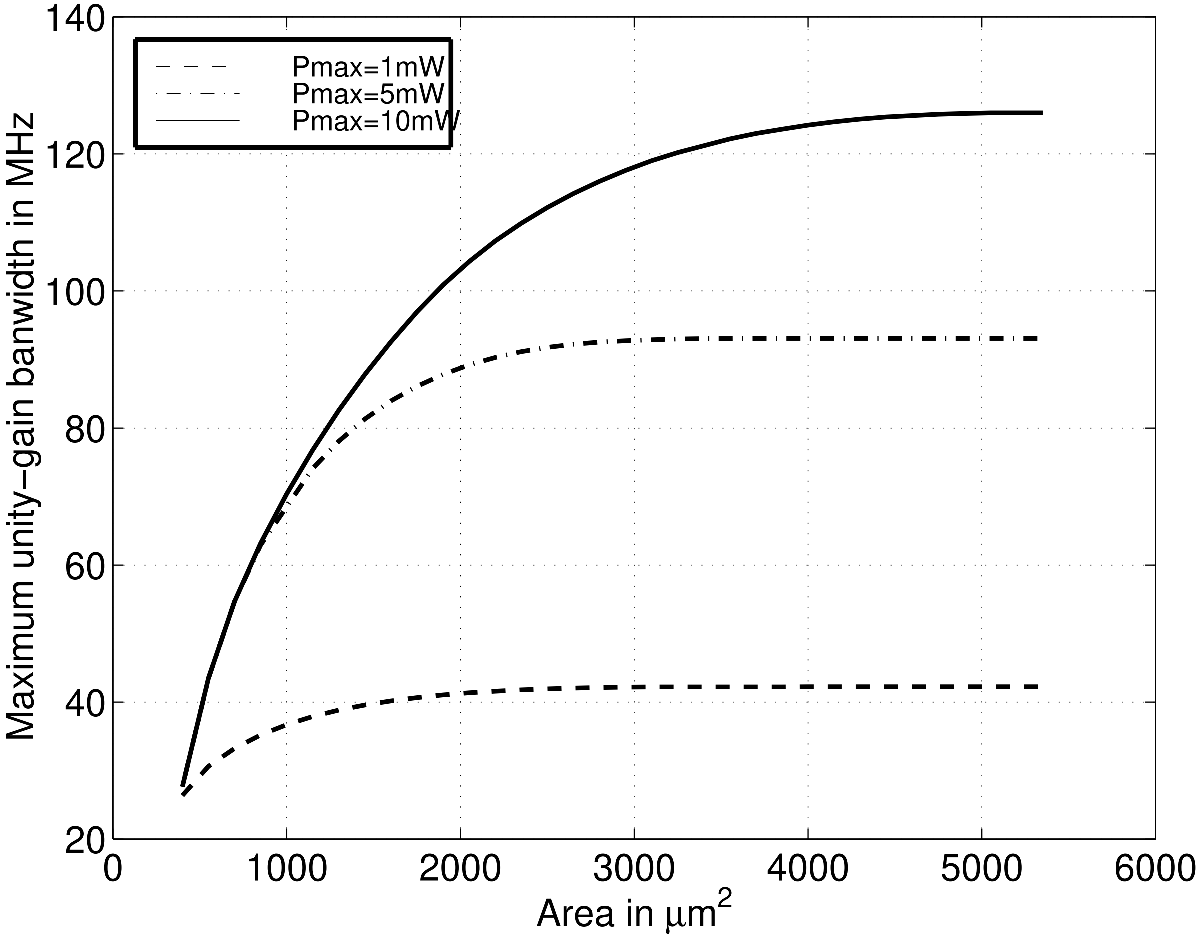
Minimum noise versus power & BW



Maximum BW versus power & load capacitance



Maximum BW versus area & power



Extensions

- can solve large coupled problems
  ($e.g.$, total area, power for IC with 100 op-amps)
- can do **robust design** that works with several process conditions
- get sensitivities for free
- method extends to wide variety of amplifier architectures, BJTs, etc.
- can use far better (monomial) MOS models, $e.g.$, for short-channel designs

Conclusions

- using **geometric programming** we can **globally** and **efficiently** solve CMOS op-amp design problems
- allows designer to spend more time **designing**, $i.e.$, exploring trade-offs between competing objectives (power, area, bandwidth, . . .)
- yields **completely automated** synthesis of CMOS op-amps **directly from specifications**
- huge reduction in analog design time

(cf. methods based on simulated annealing, expert systems, general nonlinear programming, . . .)