Stanford University

Silicon Devices at the “End of Scaling” – Opportunities and Challenges

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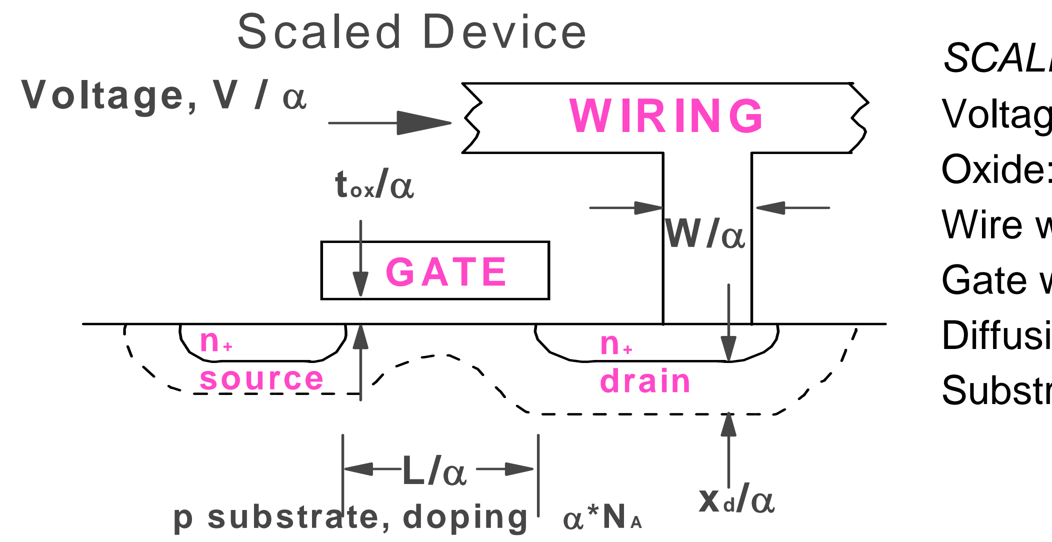
Elements of an Electronic System

- Logic
  - **execution units, bus, drivers, glue logic**
- Memory
  - **memory hierarchy - cache, data bank, NVRAM, storage**
- Communication
  - **on-chip, chip-to-chip, board-to-board...**
- User Interface
  - **sensors, input devices, output devices**

What is Classical Scaling?

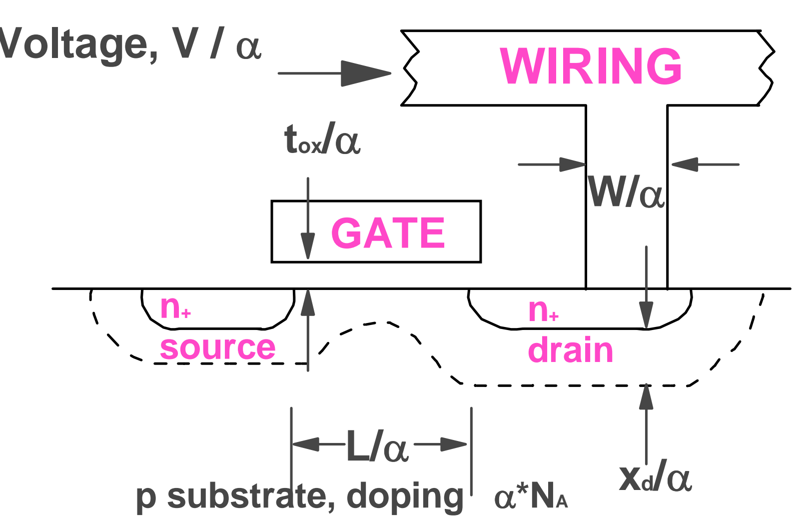
- **Scaling is the** synchronous **reduction, year on year, of technology dimensions governing the performance of silicon technology. Scaling;**
  - Improves device performance at ever lower power per function.
  - Enables increased chip functionality through added density.
  - Improves business financials through die size reduction.
- **Why would the end of classical scaling be a highly disruptive event?**
  - Scaling and progress in silicon technology have been synonymous for decades.

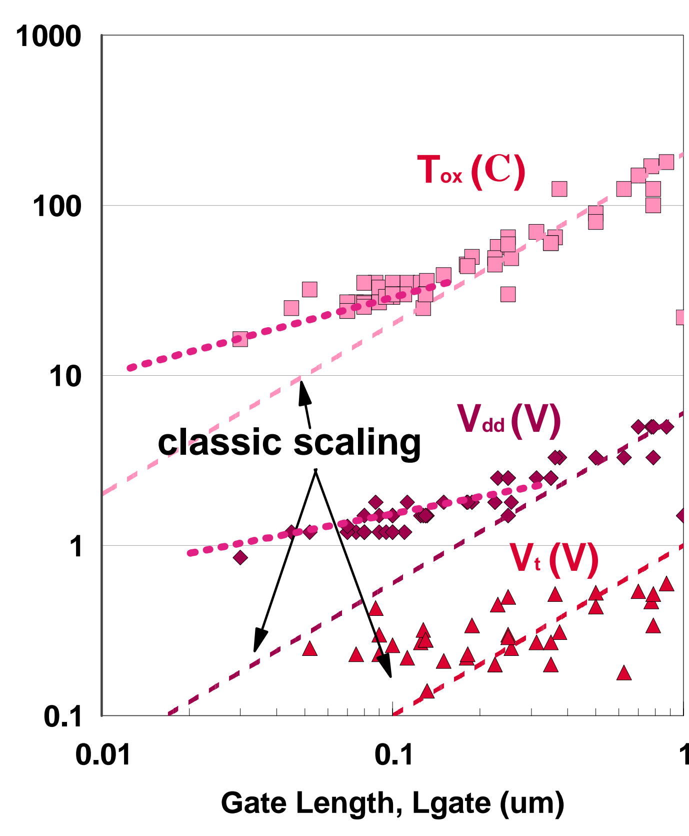


SCALING:		*RESULTS:*	
Voltage:	V/α	Higher Density:	$\sim\alpha^2$
Oxide:	t_{ox}/α	Higher Speed:	$\sim\alpha$
Wire width:	W/α	Power/ckt:	$\sim 1/\alpha^2$
Gate width:	L/α	Power Density:	~Constant
Diffusion:	x_d/α		
Substrate:	$\alpha * N_A$		

Source: IBM

Some Things do not Scale Exactly…





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Oxide:	t_{ox}/α
Wire width:	W/α
Gate width:	L/α
Diffusion:	x_d/α
Substrate:	$\alpha * N_A$

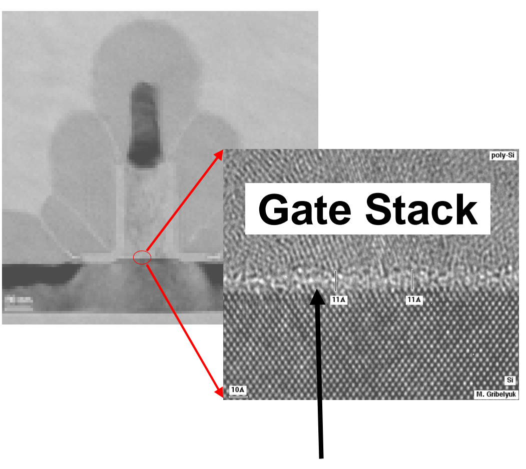
RESULTS:	
Higher Density:	$\sim\alpha^2$
Higher Speed:	$\sim\alpha$
Power/ckt:	$\sim 1/\alpha^2$
Power Density:	~Constant

Source: IBM

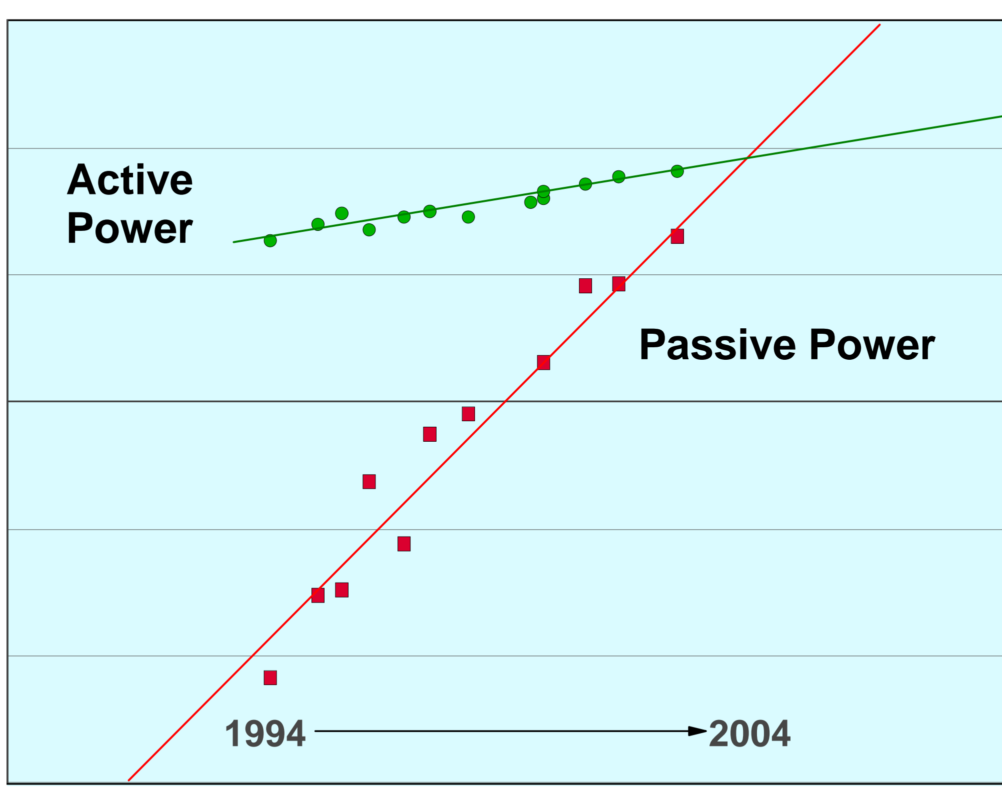
- Why deviate from "ideal" scaling
  - unacceptable gate leakage/reliability
  - additional performance at higher voltages
- What is the consequence of this deviation?
  - **a dramatic rise in power density**

Active vs. Passive Power

- **Power components:**
  - Active power
  - Passive power
    - Gate leakage
    - Sub-threshold leakage (source-drain leakage)



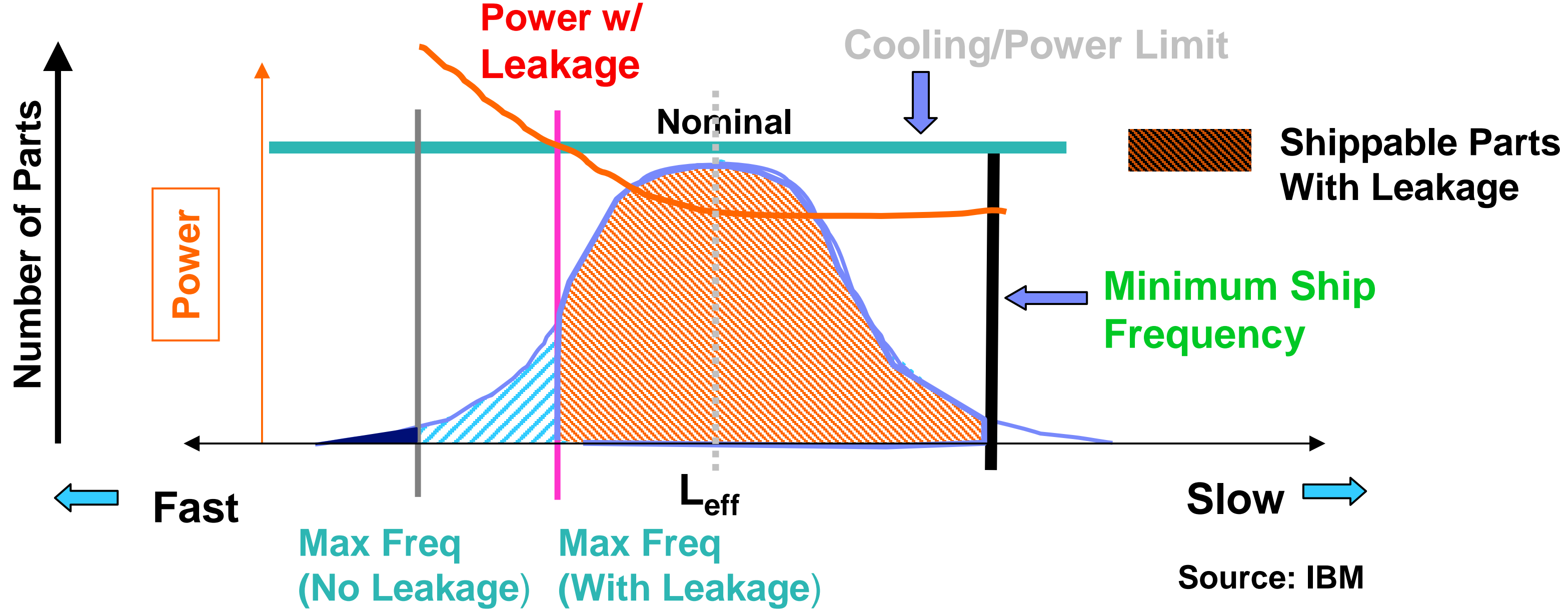
Gate dielectric approaching a fundamental limit (a few atomic layers)



Source: IBM

Power is Limiting Microprocessor Frequencies

Server microprocessors cannot simultaneously utilize all their transistors due to power limitations

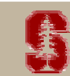


- **Moore's law is continuing with respect to transistor density, although at a reduced pace**
- **Workload demands are highly variable**
- **New methods to utilize silicon density scaling will be developed to accommodate diverse workloads while managing power constraints**

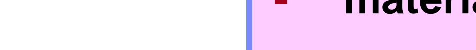
Key Challenges

- **Power / performance improvement and optimization**
- **Variability**
- **Integration**
  - Device, circuit, system

Let’s start with logic devices



Improvement Opportunities



Innovations:

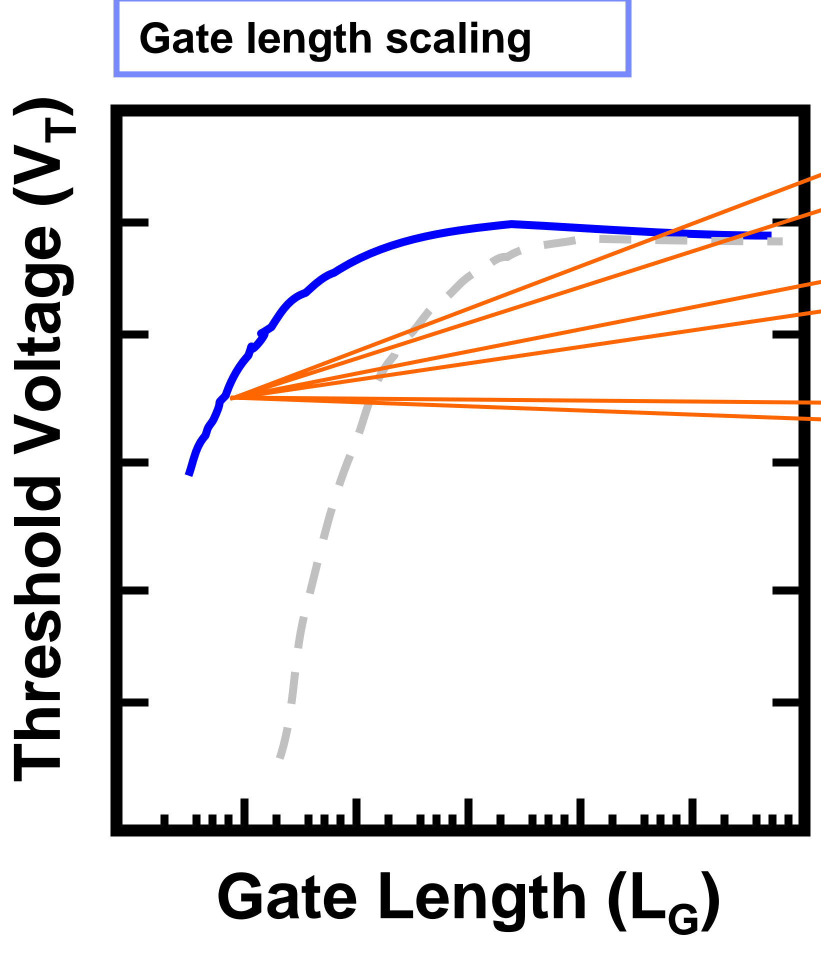
- materials
- device structure

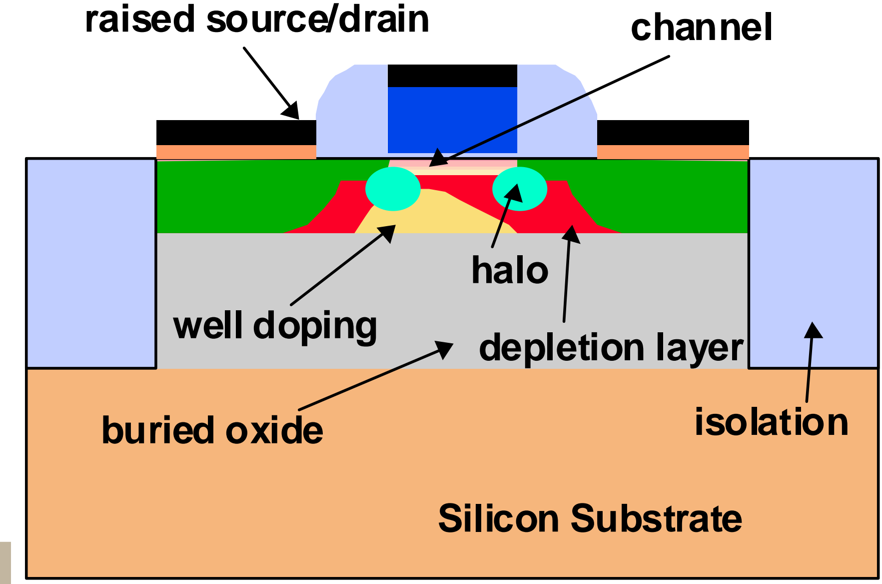
Gate length scaling

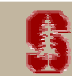
Thin gate dielectric

Doping: sharp halo & junction profiles

Thin silicon body







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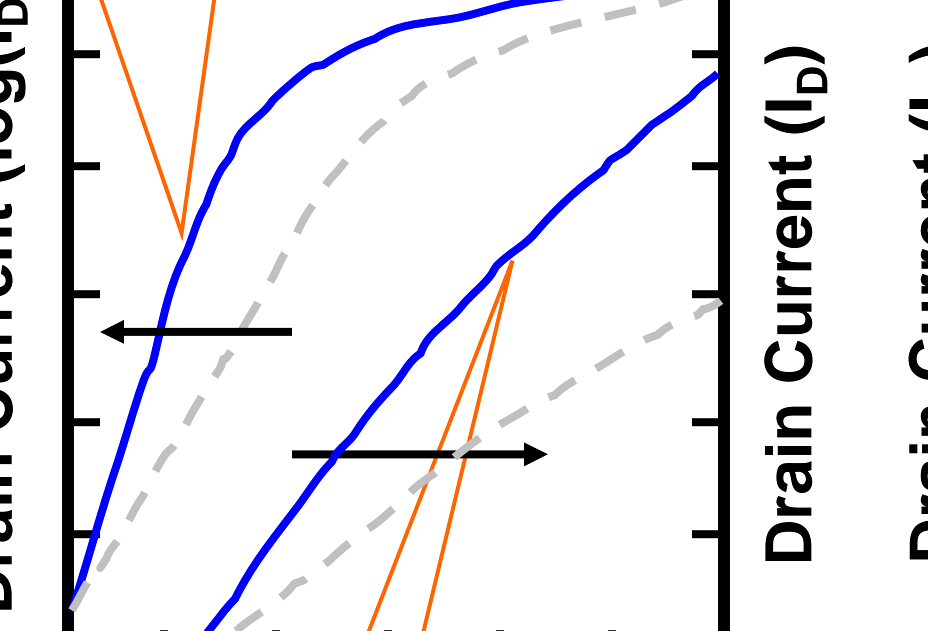
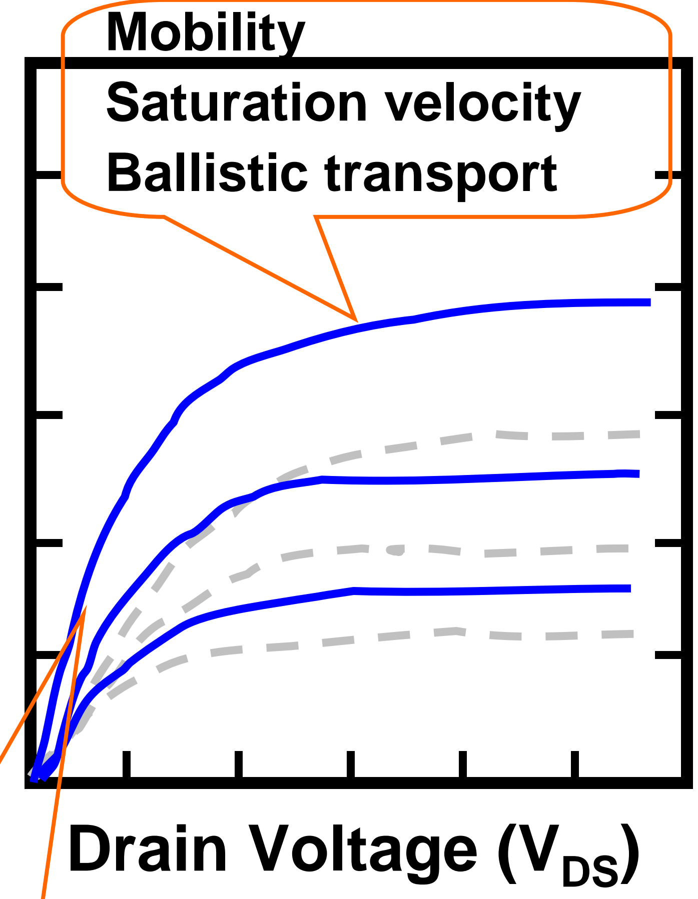




Single Gate Non-classical CMOS

Device	*Transport-enhanced Devices*	*Ultra-thin Body*		*Source/Drain Engineered Devices*	
	Strained Si, Ge, SiGe; buried oxide; isolation; Silicon Substrate	BOX	FD Si film; S; D; Ground Plane; BOX (<20nm); Bulk wafer	Bias; silicide; Gate; nFET; pFET; Silicon; Schottky barrier isolation	S; D; Non-overlapped region
Concept	Strained Si, Ge, SiGe, SiCGe or still other semiconductor; on bulk or SOI	Fully depleted SOI with body thinner than 10 nm	Ultra-thin channel and localized ultra-thin BOX	Schottky source/drain	Non-overlapped SD extensions on bulk, SOI, or DG devices
Application/ Driver	HP CMOS	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	HP CMOS	HP, LOP, and LSTP CMOS

Source: ITRS, J. Hutchby

Multiple Gate Non-classical CMOS

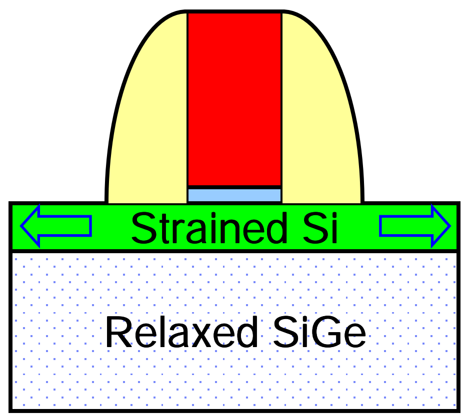
Device	*Multiple Gate FET*				
	N-Gate (N>2) FET	*Double-gate FET*			
Concept	Tied gates (number of channels >2)	Tied gates, side-wall conduction	Tied gates planar conduction	Independently switched gates, planar conduction	Vertical conduction
Application/Driver	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	LOP and LSTP CMOS	HP, LOP, and LSTP CMOS

Source: ITRS, J. Hutchby

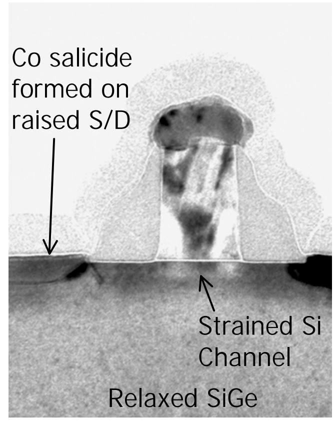
Transport Enhanced Devices

- Wafer-scale strained Si
  - **Strained Si on relaxed SiGe buffer on bulk Si**
  - **Strained Si on relaxed SiGe buffer on insulator**
  - **Strained Si directly on insulator**
- Local strain
  - **Dielectric films**
  - **Isolation (STI), device size dependent structures**
  - **SiGe in recessed source/drain**
- Crystal orientation and current flow direction
- Other materials
  - **Bulk Ge**
  - **Ge on insulator**
  - **Strained Ge**

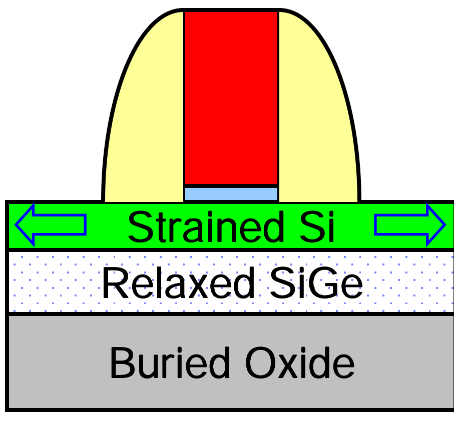
Strained Silicon



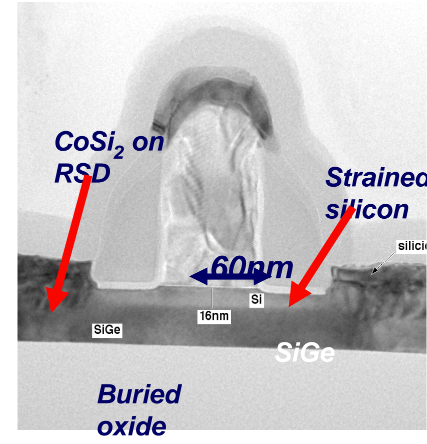
Strained Si/SiGe Bulk MOSFET



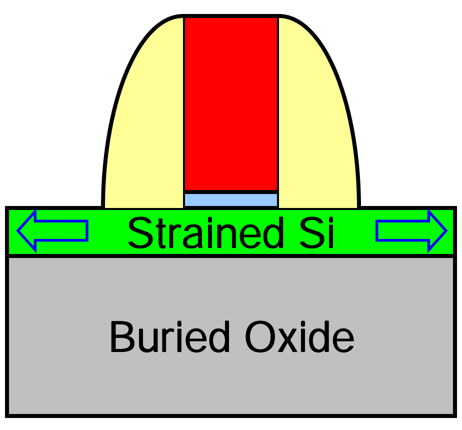
K. Rim et al., *Symp. VLSI Tech.*, p. 59, 2001.
K. Rim et al., *Symp. VLSI Tech.*, p. 98, 2002.



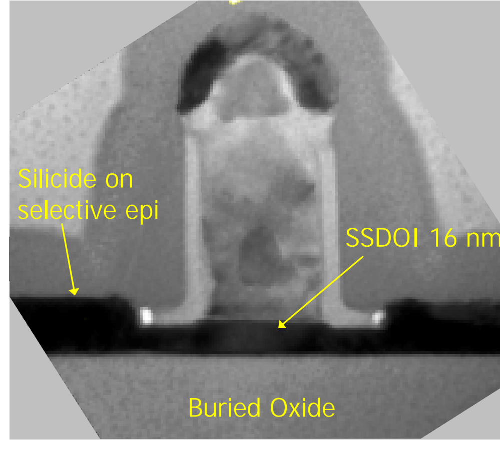
SGOI (SiGe-on-Insulator) MOSFET



B. Lee et al., *IEDM* 2002



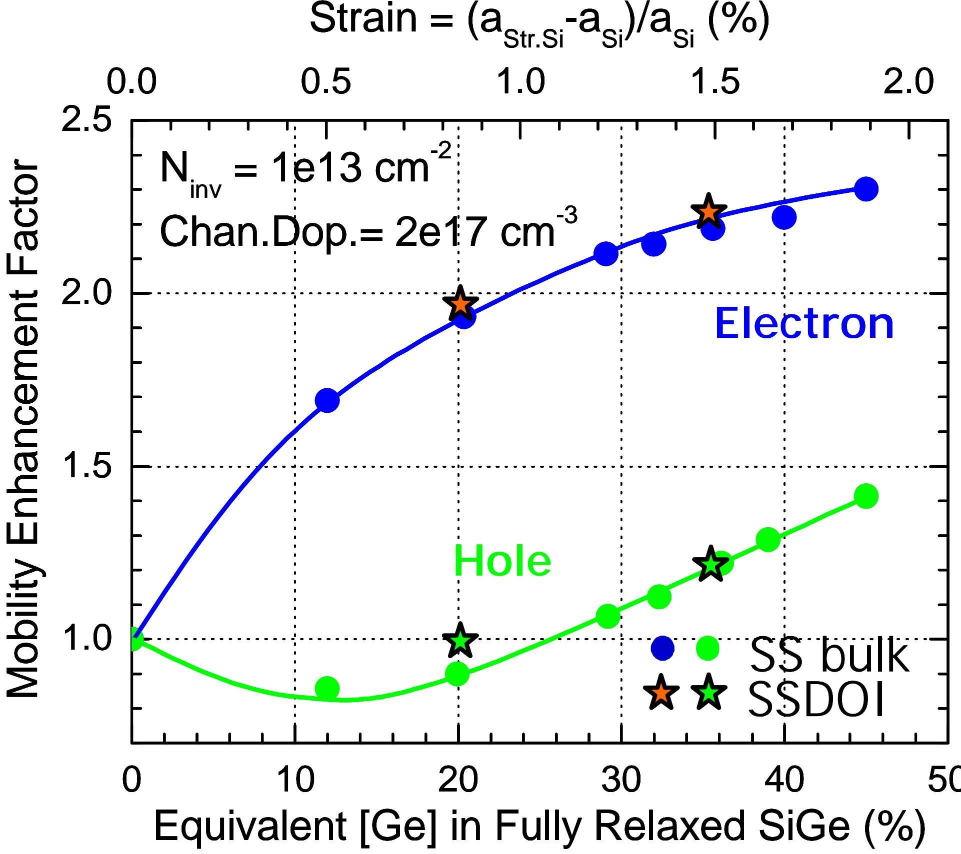
SSDOI MOSFET



K. Rim et al., *IEDM*, 2003.

Strain-Dependence of Mobility

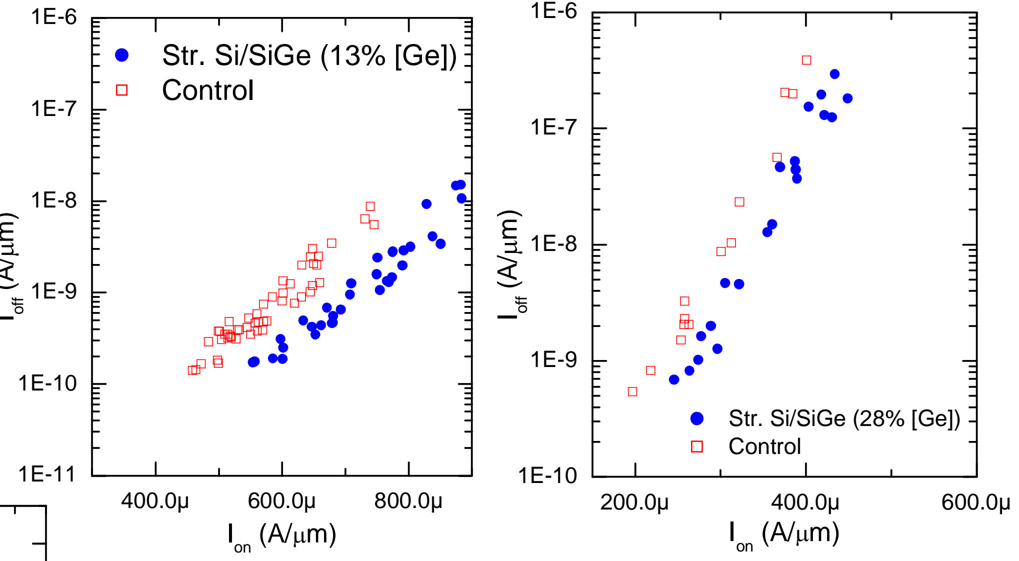
K. Rim et al., *IEDM*, 2003.



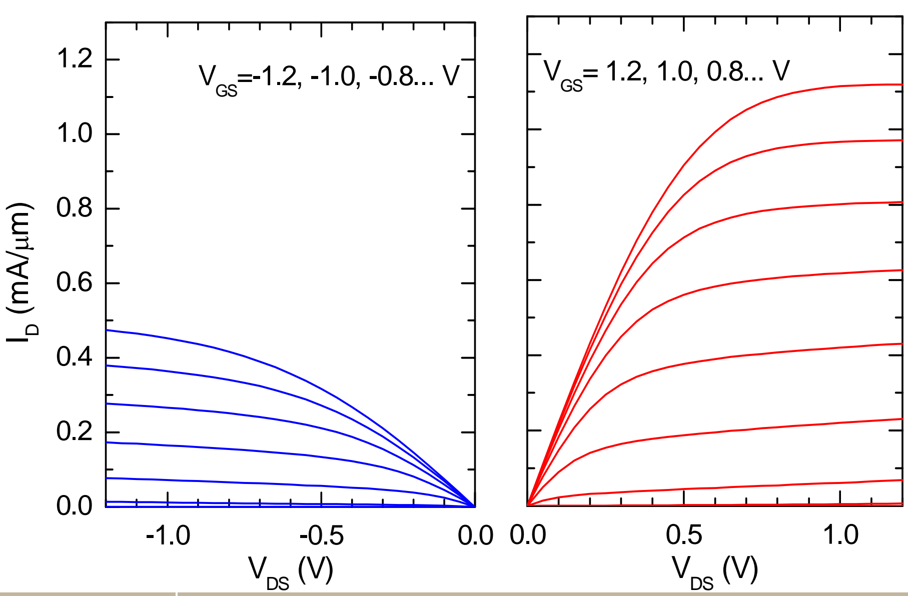
- Mobility enhancements consistent with amount of strain even for strained silicon on insulator

Short Channel Strained Silicon FETs

- **Key challenges:**
  - maintain performance enhancement at short channels under high field transport
  - material defect reduction



K. Rim et al., *Symp. VLSI Tech.*, p. 98, 2002.

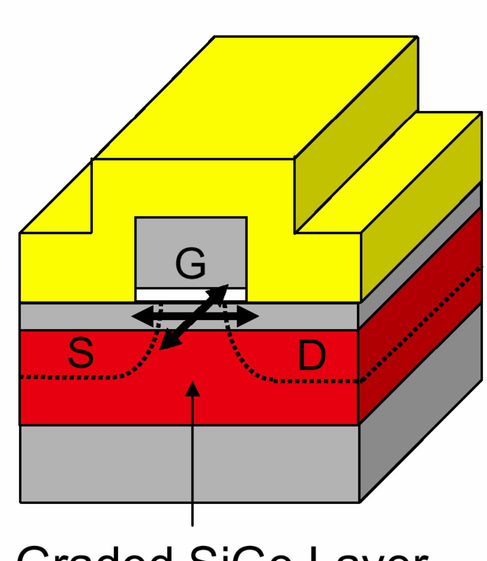


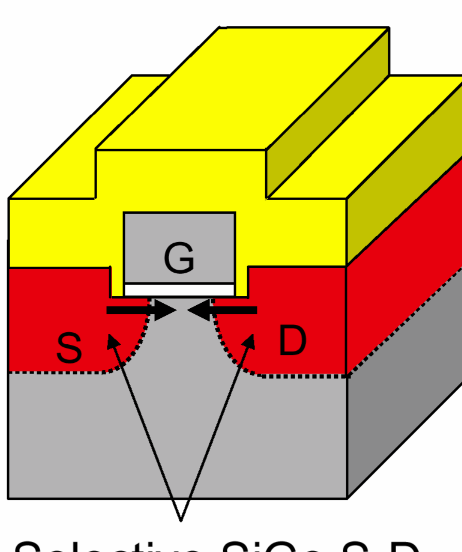
K. Rim et al., *IEDM*, 2003.

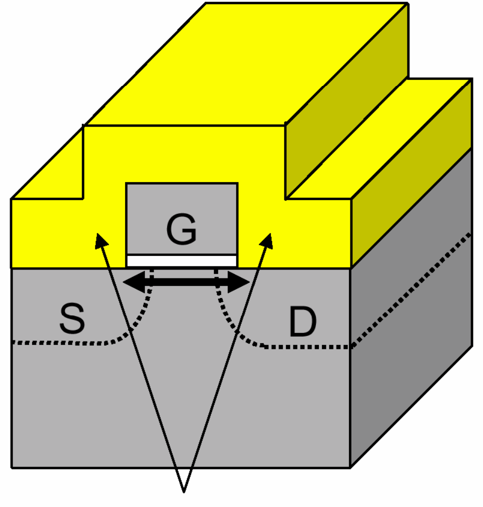
Uniaxial Strain vs Biaxial Strain

Traditional Approach

Intel's 90nm Technology







Graded SiGe Layer

Biaxial Tensile Strain

Selective SiGe S-D

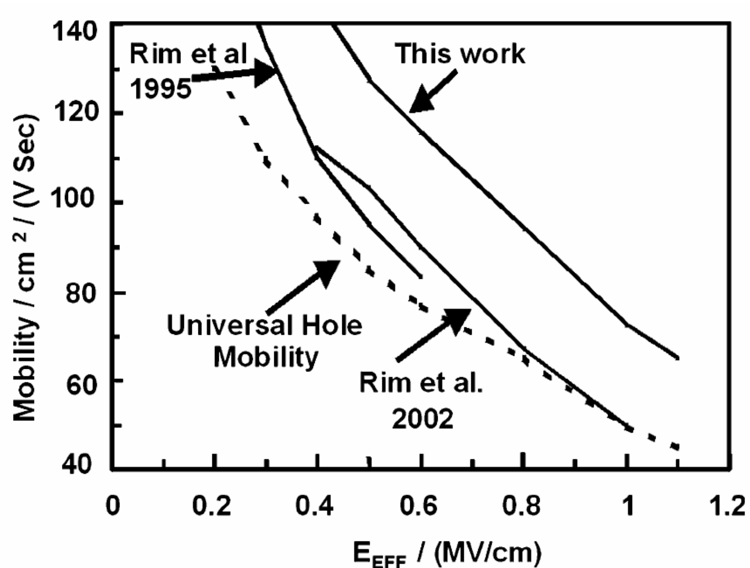
Uniaxial Compressive Strain for PMOS

Tensile Si_3N_4 Cap

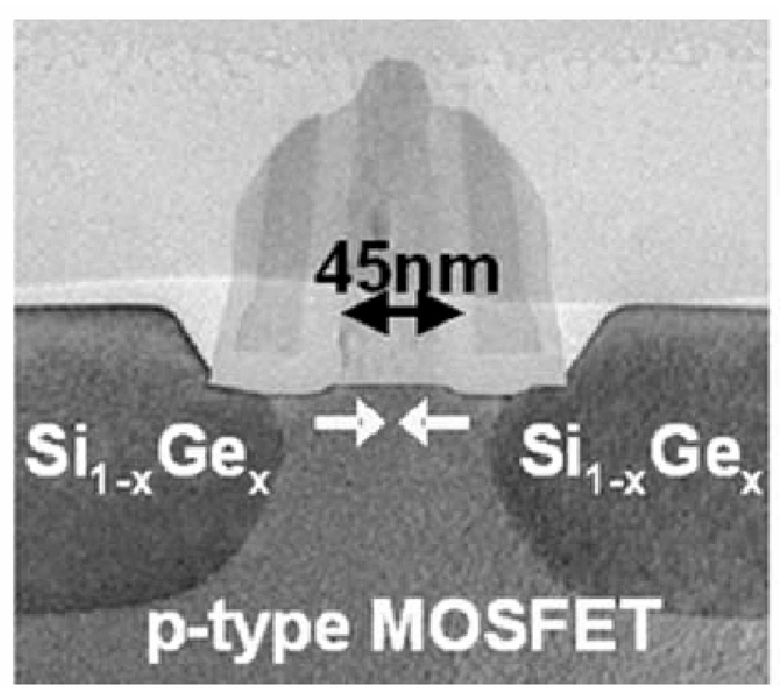
Uniaxial Tensile Strain for NMOS

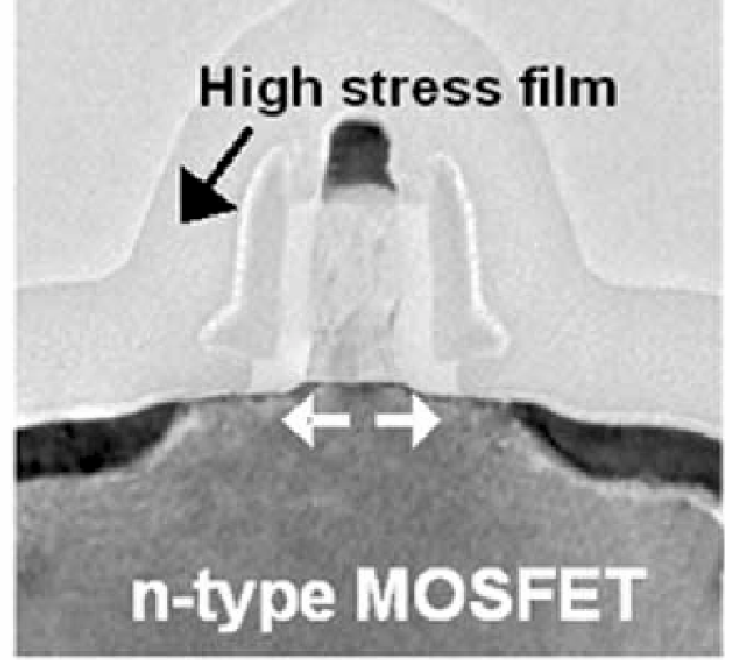
Source: Intel

Uniaxial Strain

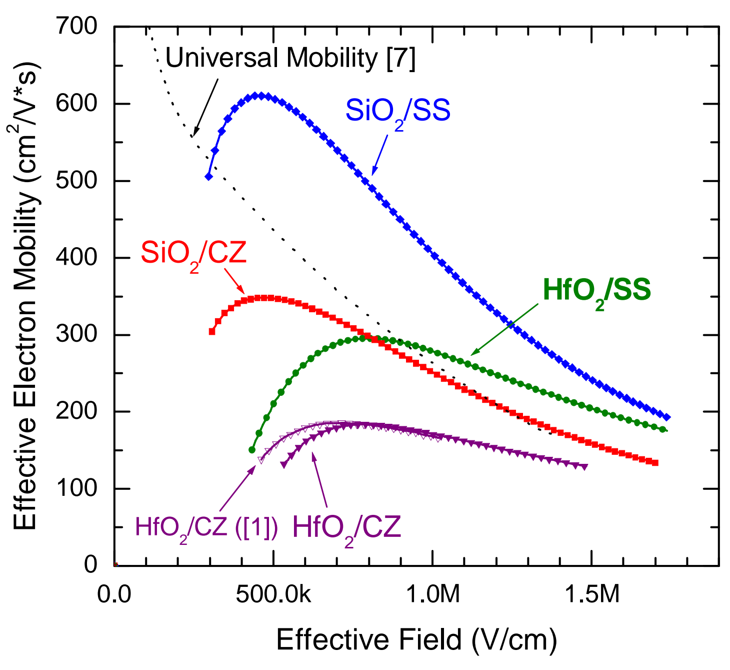


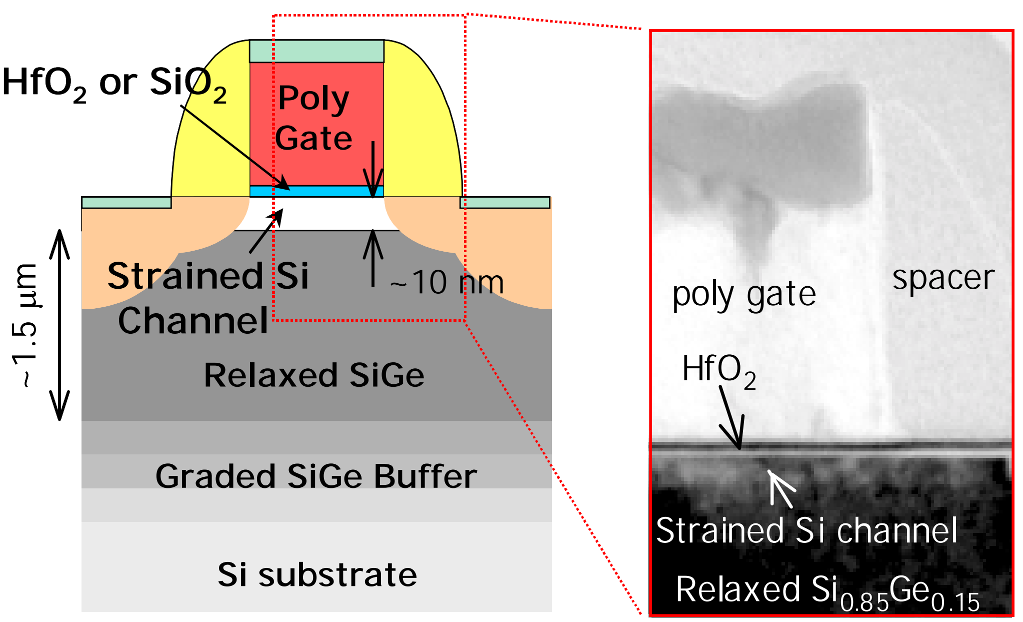
S. Thompson et al., *IEEE EDL*, p. 191, 2004.





Strained Si + High-k





Mobility at E_{eff} = 1.4 MV/cm		Substrate	
		CZ Si	Strained Si
Gate Dielec.	SiO_2	SiO_2/CZ 173	SiO_2/SS 271
	HfO_2	HfO_2/CZ 134	HfO_2/SS 218

K. Rim et al., *Symp. VLSI Tech.*, p. 12, 2002.

Surface Orientation & Current Flow Direction

<0$\bar{1}$1>
<010>
<011>

(100) surface

<001>
<$\bar{1}$10>

(110) surface

S D
G

M. Yang et al., *IEDM* 2003

Hole Mobility ($cm^2V^{-1}s^{-1}$)
150
100
50
(110)/<110>
(111)/<112>
(100)/<110>
0.0
$5.0x10^{12}$
$1.0x10^{13}$
$1.5x10^{13}$
N_{inv} (cm^{-2})

Electron Mobility ($cm^2V^{-1}s^{-1}$)
300
200
100
(100)/<110>
(111)/<112>
(110)/<110>
0.0
$5.0x10^{12}$
$1.0x10^{13}$
$1.5x10^{13}$
N_{inv} (cm^{-2})

M. Yang et al., *IEDM* 2003

Hybrid Orientation Technology (HOT)

pFET Performance Enhancement for HOT

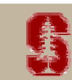
V_{gs}=-1.0V, -0.8V, -0.6V ..
W=5μm
L_{poly}=80nm
(100)
(110)
Drain Current (mA)
V_{ds} (V)

W=5μm
V_{ds}=-1.0V
L_{poly}=80nm
V_{ds}=-50mV
(100)
(110)
Drain Current (A)
V_{gs} (V)

V_{dd}=-1.0V
I_{off} (A/μm)
I_{on} (μA/μm)

	I_{on}	I_{dlin}
I_{off}=100nA/μm	+33%	+45%
I_{off}=10nA/μm	+44%	+58%

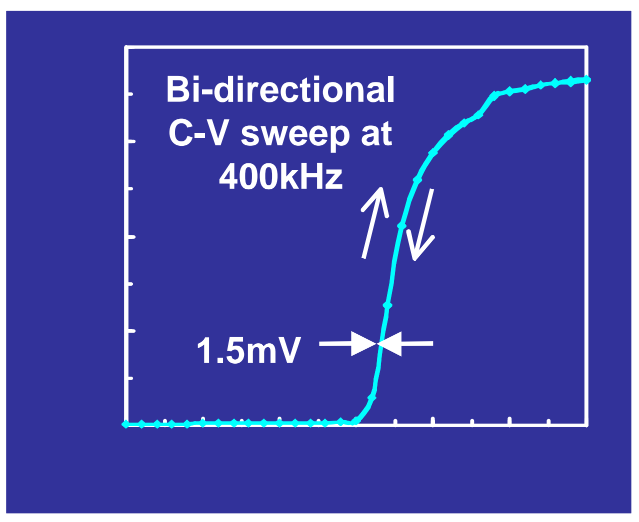
M. Yang et al., *IEDM* 2003

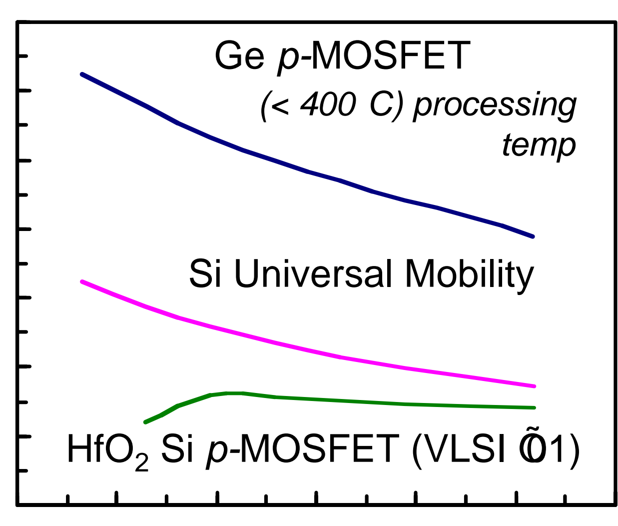


Germanium FET

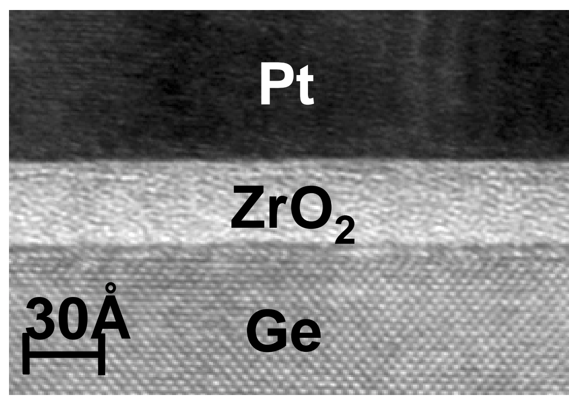
H. Shang et al., *IEDM*, p. 441, 2002.
H. Shang et al., *IEEE EDL*, p. 135, 2004.

High Mobility Ge PMOSFETs with ZrO_2 Gate Dielectric





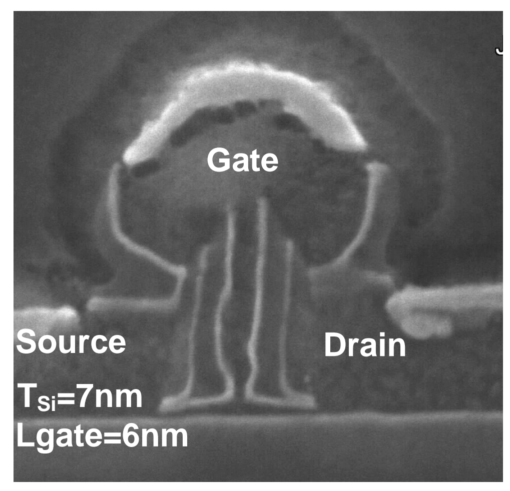
HR-XTEM

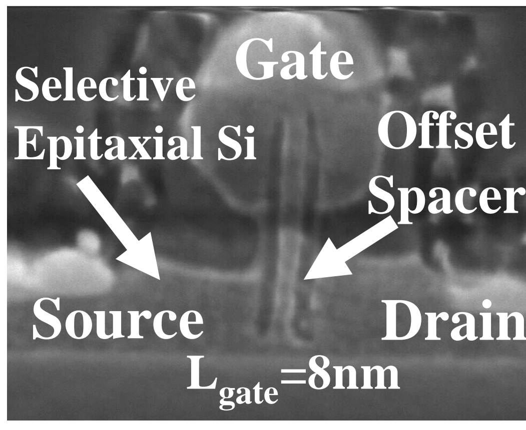


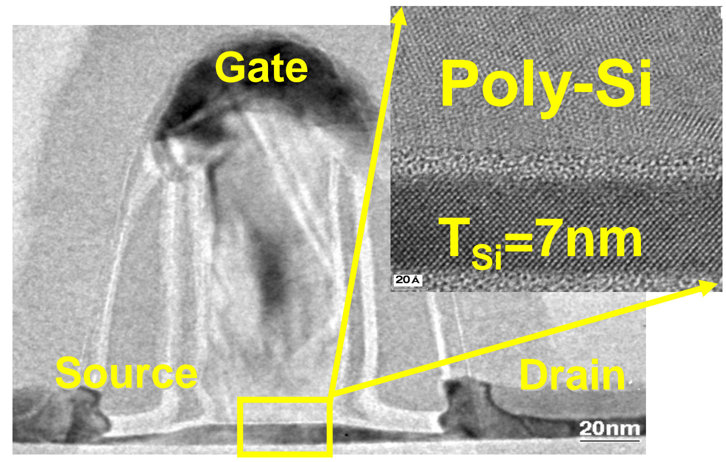
- 1st demo of metal gate and hi-κ on Ge MOSFETs
- EOT upto 0.5 nm demonstrated
- 3× mobility vs. Hi-k Si *p*-MOSFETs
- 400°C maximum temperature process
- Work on VLSI CMOS structures in progress

Chui, Kim, McIntyre, Saraswat, IEDM 2002

Nanoscale Si FET (Gate Length = 6 – 8 nm)

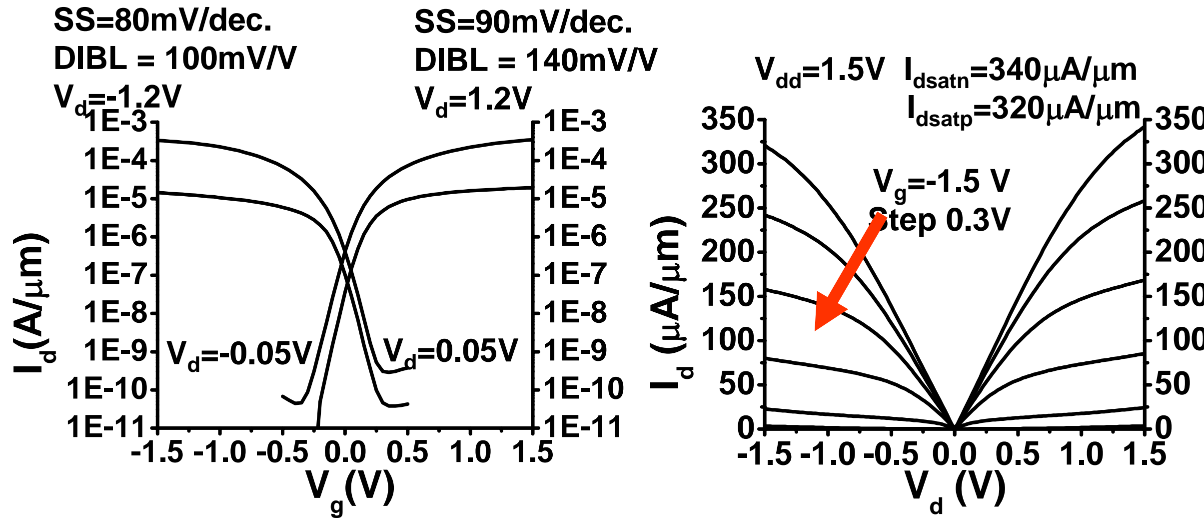






B. Doris et al., *IEDM*, p. 267, 2002.

B. Doris et al., *IEDM*, 2003.

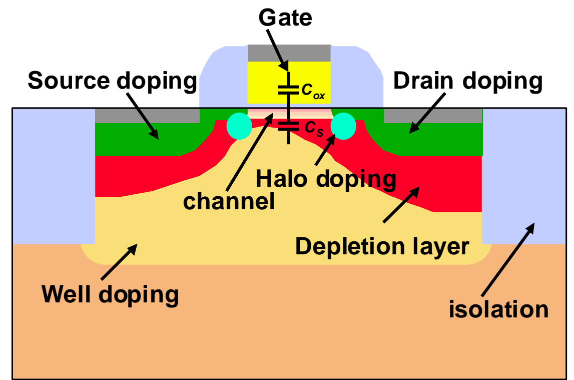


Key Issues for Ultra-Thin Body FETs

- Raised source/drain
- Thin gate dielectric
- Uniform, thin (< 10 nm) channel thickness
- Minimize surface roughness
- External resistance in extremely thin Si
- Carrier mobility in thin channels

From Bulk to Double-Gate FET

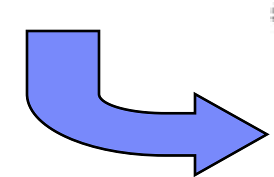
- M. Ieong et al., *MRS Spring Meeting*, 2003.
- M. Ieong et al., *IEDM*, p. 441, 2001.
- M. Ieong, H.-S. P. Wong et al., *SISPAD,* p. 147, 2000.
- H.-S. P. Wong, D. Frank, P. Solomon, *IEDM,* p. 407, 1998.

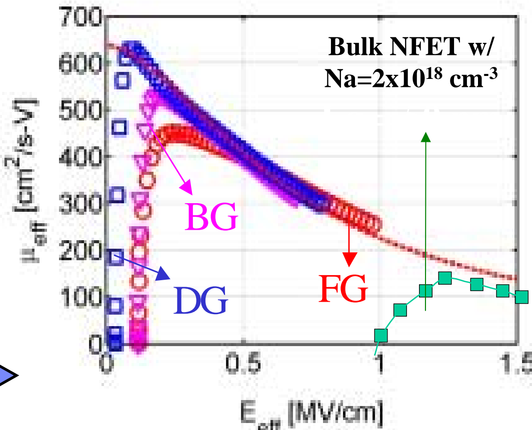


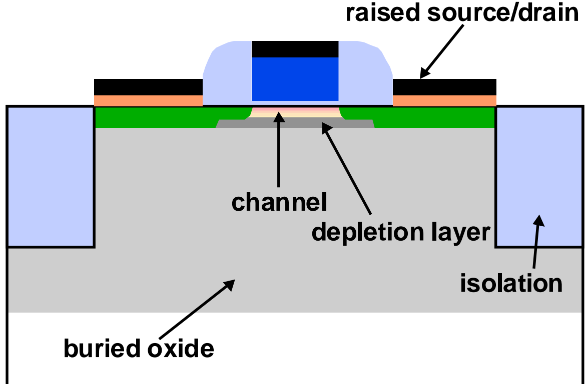
Bulk FET

Improves:

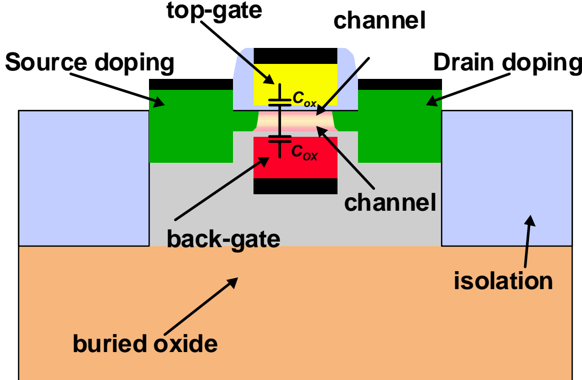
- **Short-channel control**
- **Subthreshold slope**
- **Mobility**



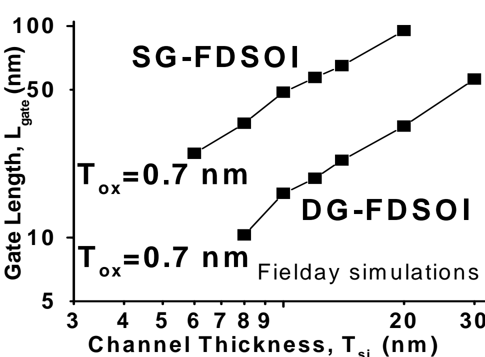




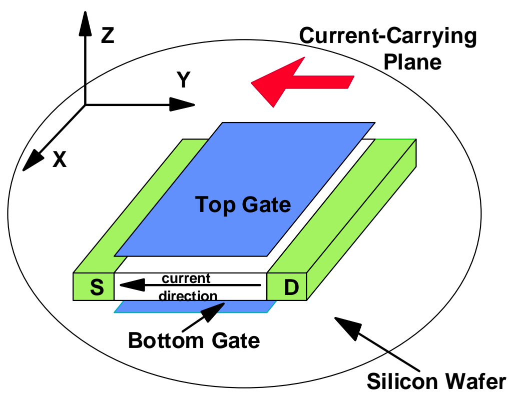
Ultra-thin body SOI FET

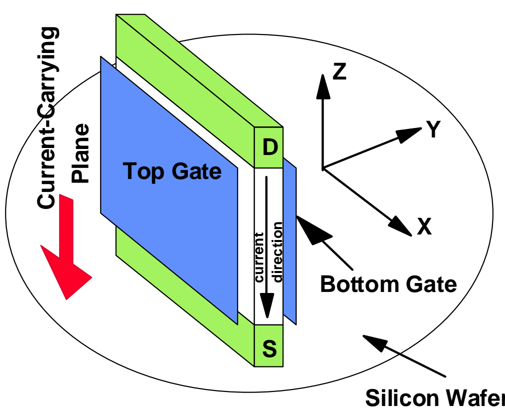


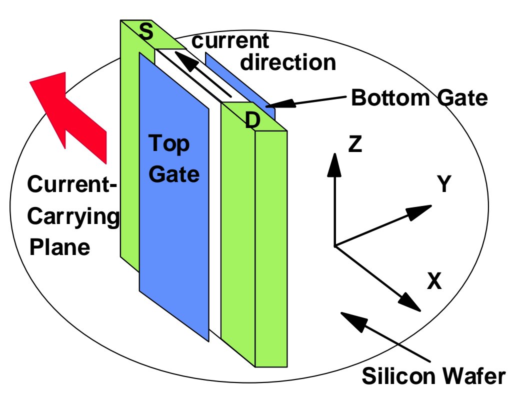
Double-Gate FET



Double-Gate FET Fabrication







Horizontal channel:

- Bury back-gate under single crystal channel
  - wafer bonding
  - selective epitaxial Si growth
- Back-gate not easily accessible

Vertical channel:

- Lithography and patterning 3-4x more stringent (5-10 nm required)
  - e-beam litho
  - sidewall techniques
- Gates accessible from the side

- Self-aligned gates required

H.-S. P. Wong, D. Frank, Y. Taur, J. Stork, IEDM, p. 747, 1994.

H.-S. P. Wong, D. Frank, P. Solomon, C. Wann, J. Welser, *IEEE Proceedings,* p. 537, April, 1999.

FinFET Fabrication

Source Pad

Fin

Gate

Drain Pad

Poly-Si

Crystalline-Si

J. Kedzierski et al., *IEDM*, p. 437, 2001.

Pa 1 = 55 nm
Pb 1 = 52.1 Deg
<100>
<110>
Pa R1
Pa 1
Drain Pad
Pa 2 = 781 nm
Pb 2 = 323.6 Deg
Source Pad
Pa R2
Mag = 150.00 K X
100nm
EHT = 5.00 kV
WD = 5 mm
Date :3 Apr 2001
File Name = PreEpi4_3Dna.tif

Gate
Source
Drain
Source
Conventional FET

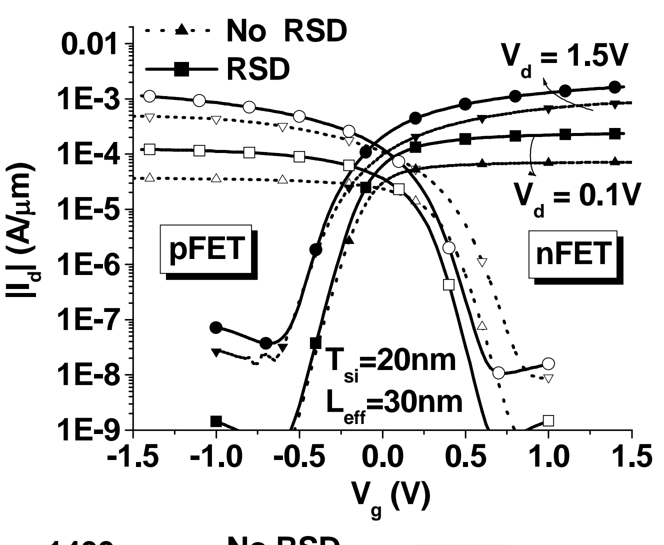
Gate
Source
Drain
Source
FinFET

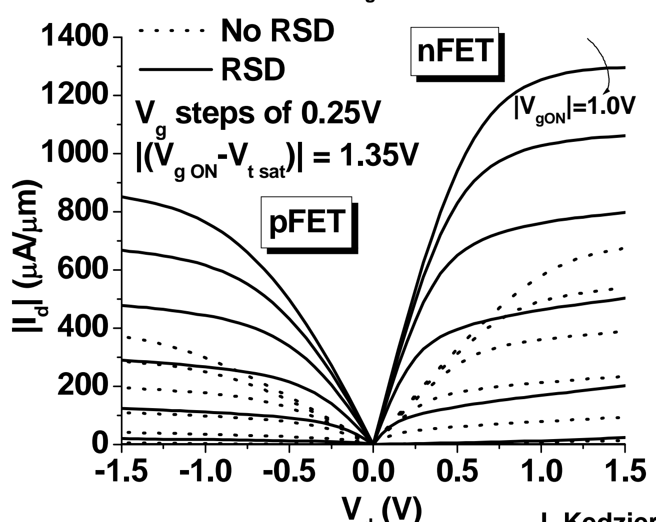
Poly-Si
Si

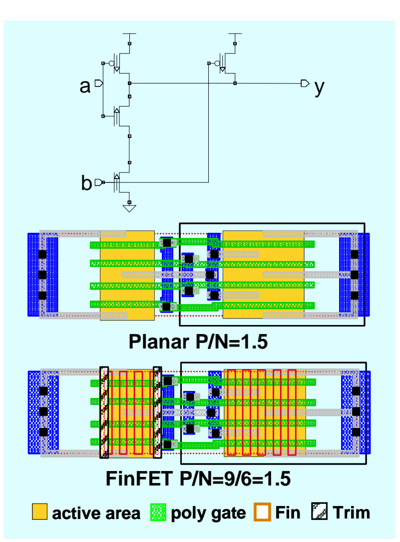
TEOS
T_{si}=20nm
T_{ox}=1.6nm
H=65nm
Poly-Si
H
T_{si}
BOX
SEM

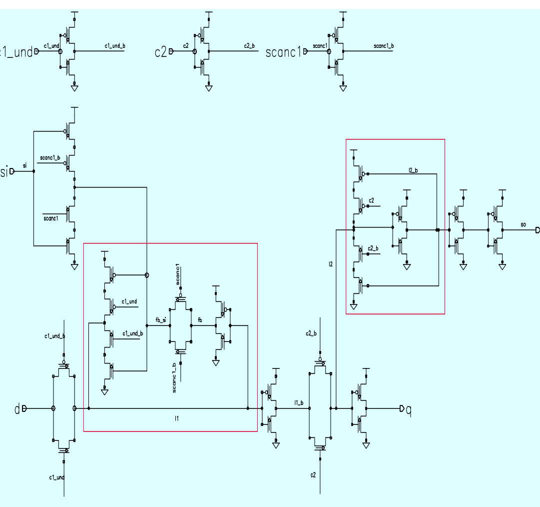
T_{ox} = 1.6nm
TEM

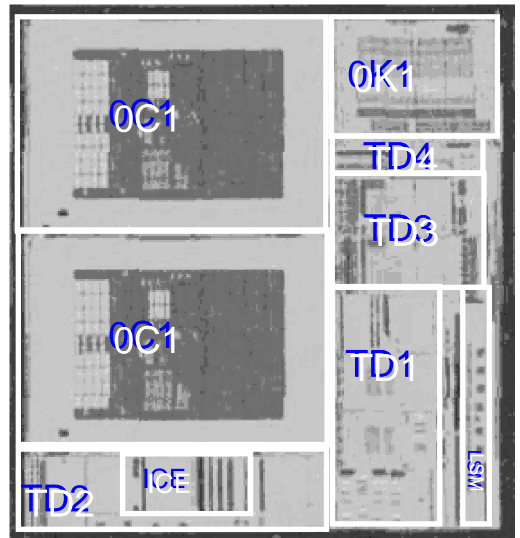
FinFET Double-Gate FET

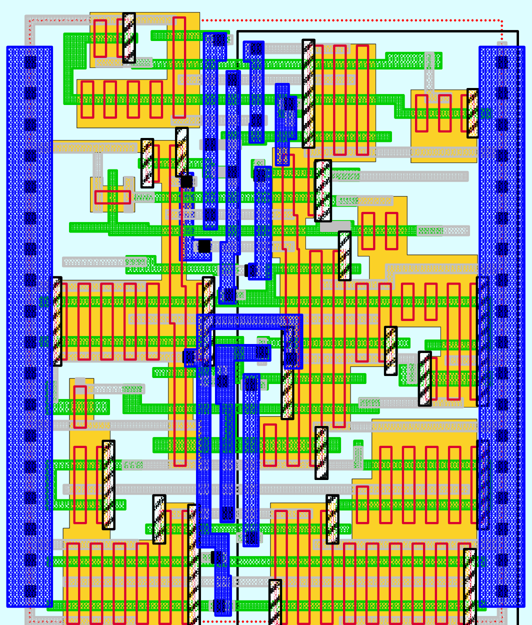






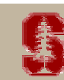






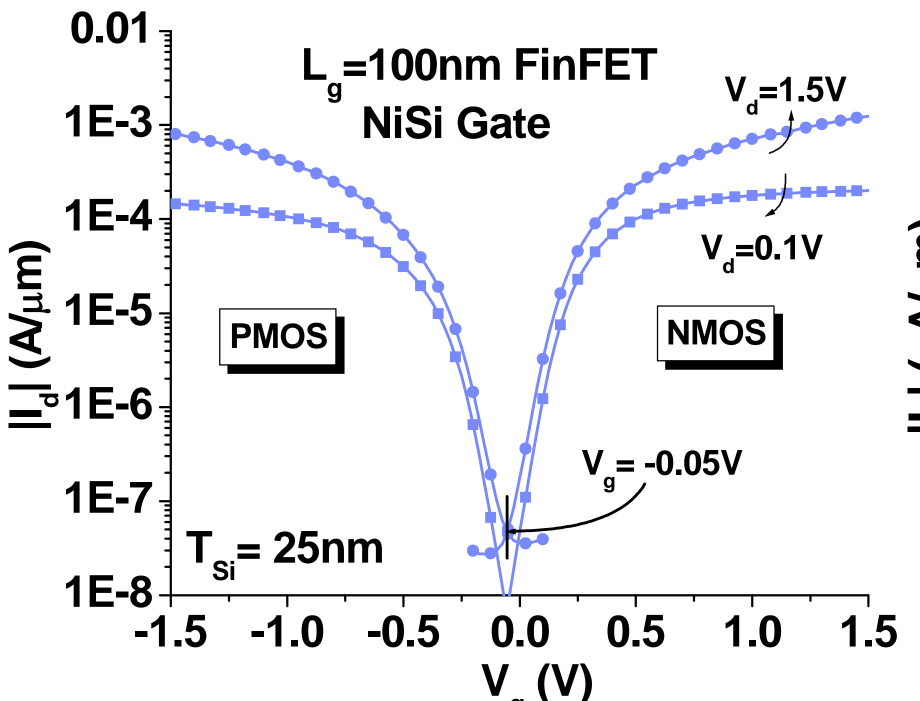
I. Aller et al., *IEEE SOI Conf.*, paper 3.2, 2003.

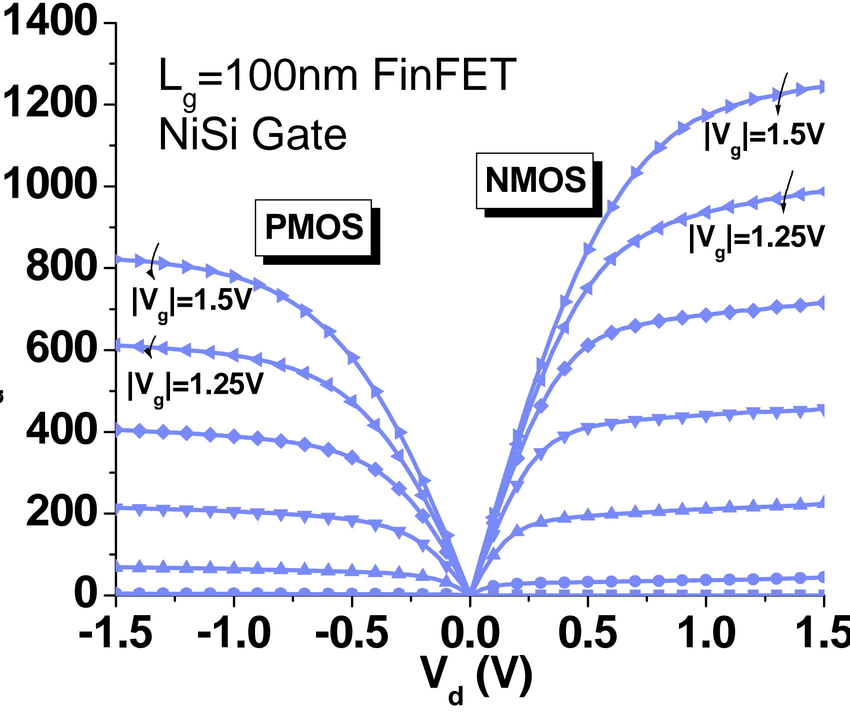
J. Kedzierski et al., *IEDM*, p. 437, 2001.



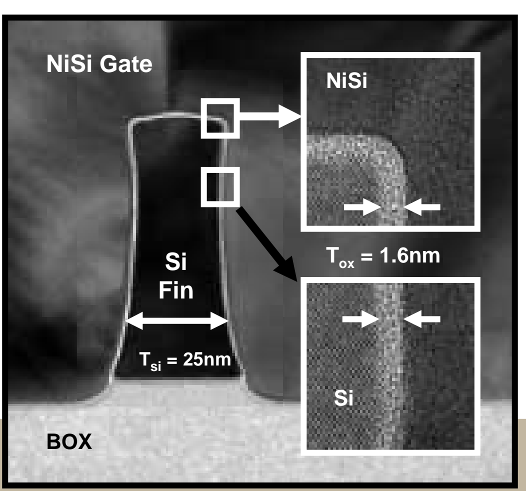
NiSi Gated Double-Gate FinFET

J. Kedzierski et al., *IEDM*, p. 247, 2002.

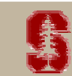




- Undoped Body
- Epitaxy RSD
- No body doping
- Metal gates



- $W=2H_{fin}$
  - nFET 1.3mA/um (at V_{dd}=1.5V)
  - pFET 0.8mA/um (at V_{dd}=1.5V)
- nFET V_t= 0.1V
- pFET V_t= -0.23V
- S = 70mV/dec



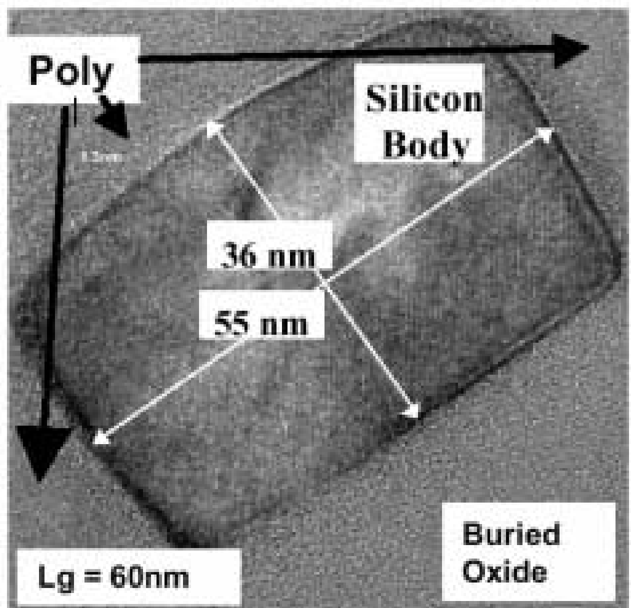
2-Gates, 3-Gates, 4-Gates ...Multi-Gate FETs

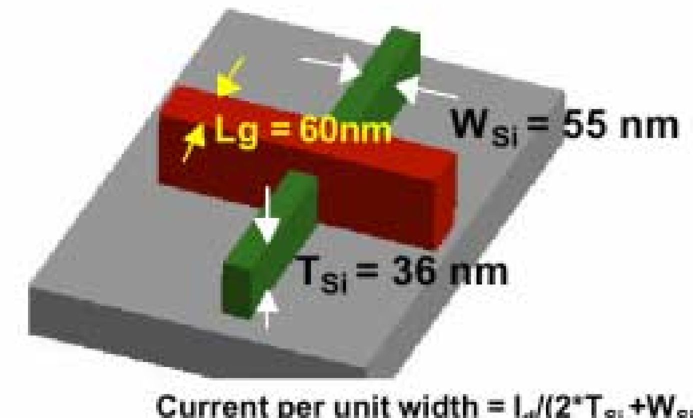
- **Put gates closer to channel**
- **Control short-channel effects better**

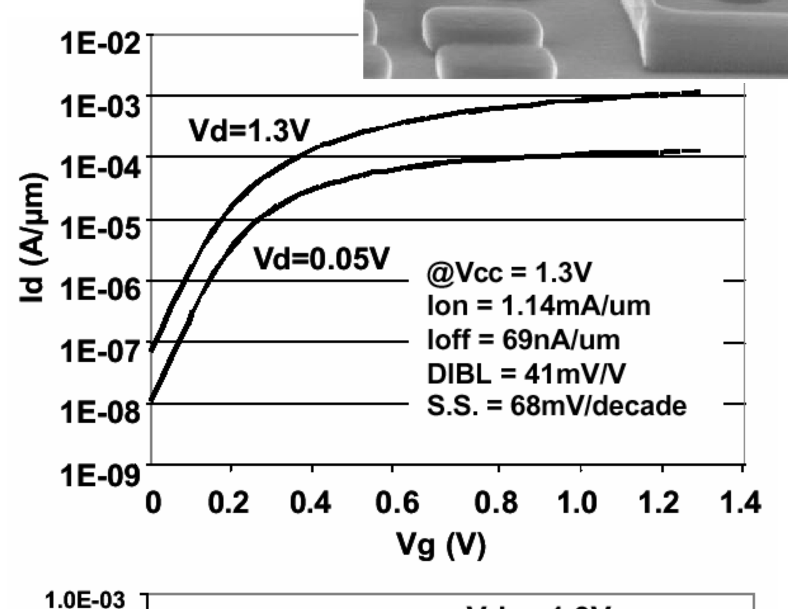
R. Chau et al., *SSDM*, 2002.

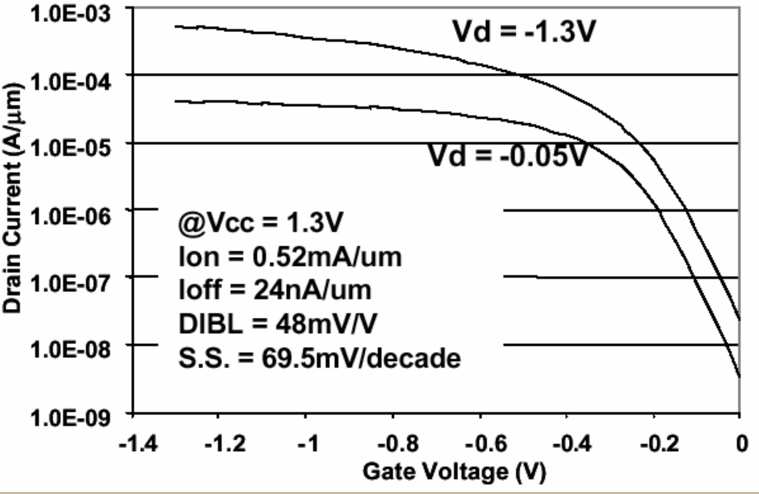
E. Leobandung et al., *J. Vac. Sci. Tech., B* 15(6), p. 2791, 1997.

Triple-Gate FET









Multiple Fins

Optical or e-beam lithography pitch

$W_{fin,\ Litho}$

Optical or e-beam lithography pitch

Removal of dummy and Si-fin etch

Fin pitch

$W_{fin,\ Spacer}$

Resist

Si Fin

Dummy

Spacer

Si Fin

Spacer

Conventional lithography

Spacer lithography

W_{fin}

Gate

X'

Oxide hard mask: 100nm

$Si_{0.6}Ge_{0.4}$: 400nm

Spacer-defined fins

Source

Drain

X

Nitride : 50nm

Oxide : 4nm

Si-fin height : 50nm (T_{si})

L_g

Source

Gate

Drain

Source

FinFET

Photo Resist

PSG spacer

Source

Drain

Photo Resist

Gate

Planarized gate

6 fins

Drain

Source

S_1

S_2

Source

Gate

Drain

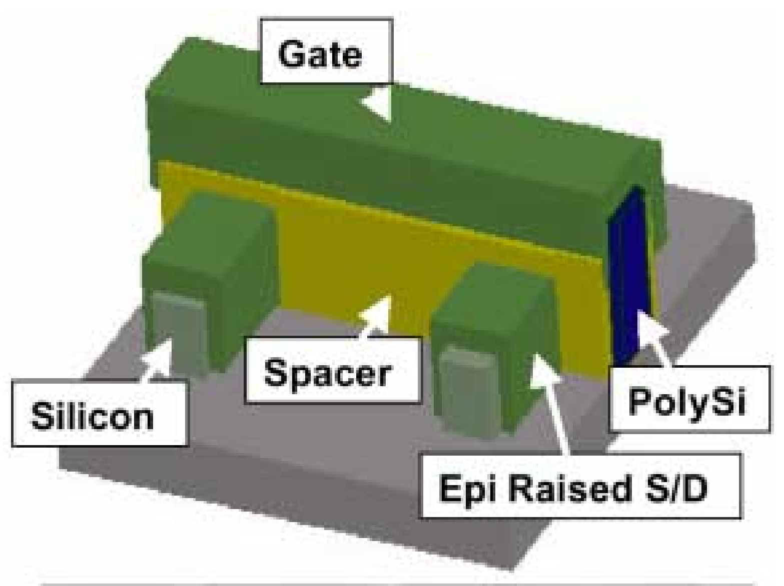
Source

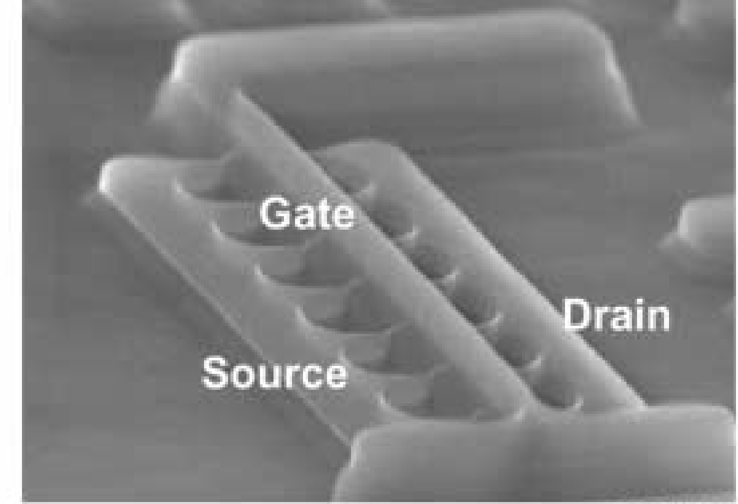
Conventional MOSFET

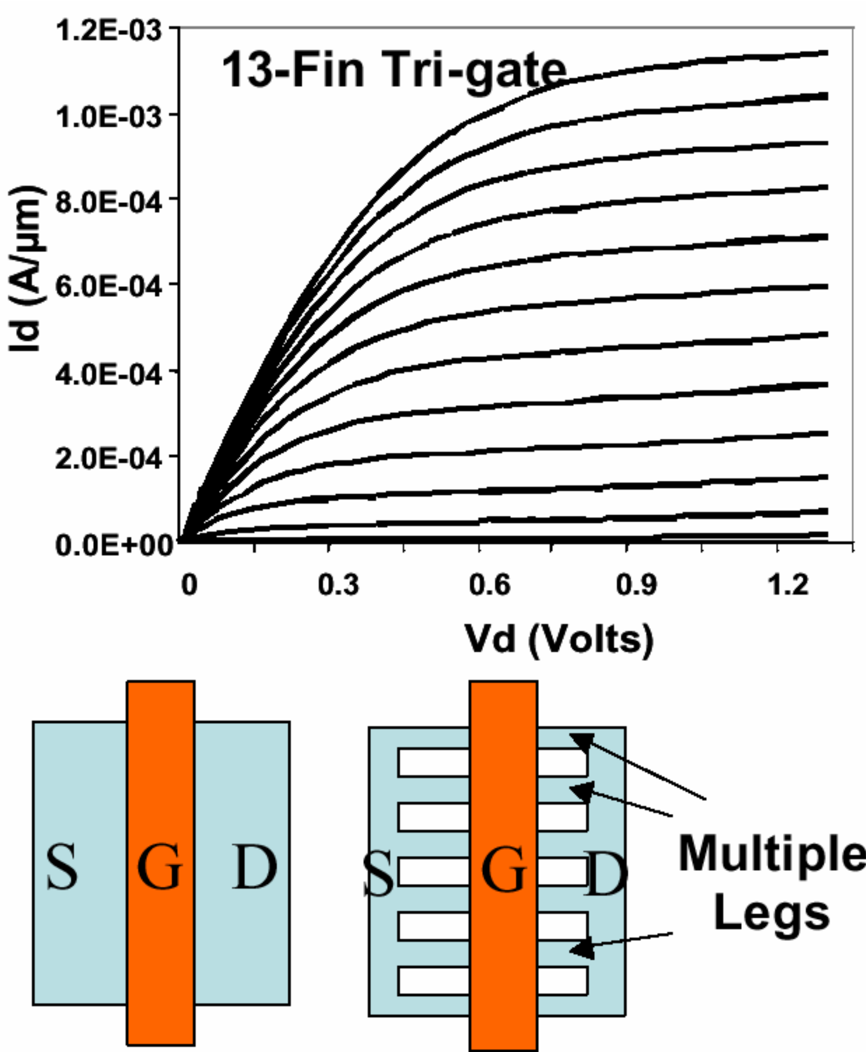
Y. Choi et al., *IEDM*, p. 421, 2001.

Multiple Fins: Triple-gate

R. Chau et al., *SSDM*, 2002.

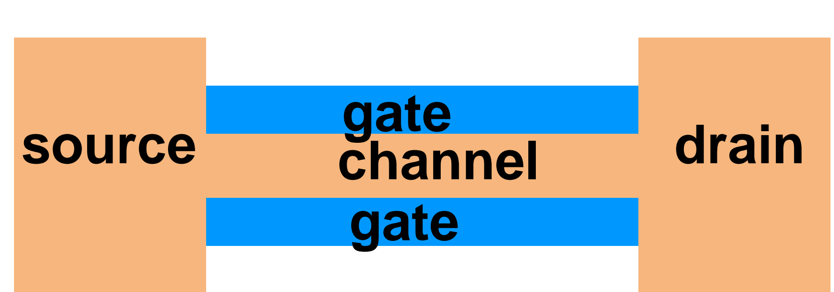


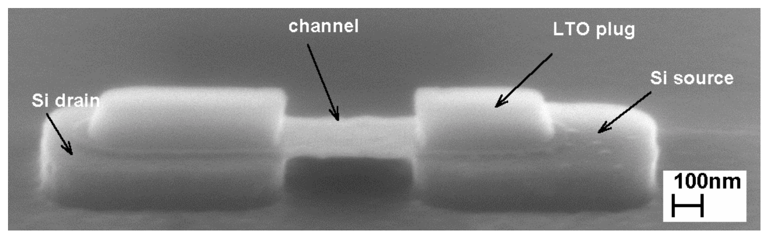


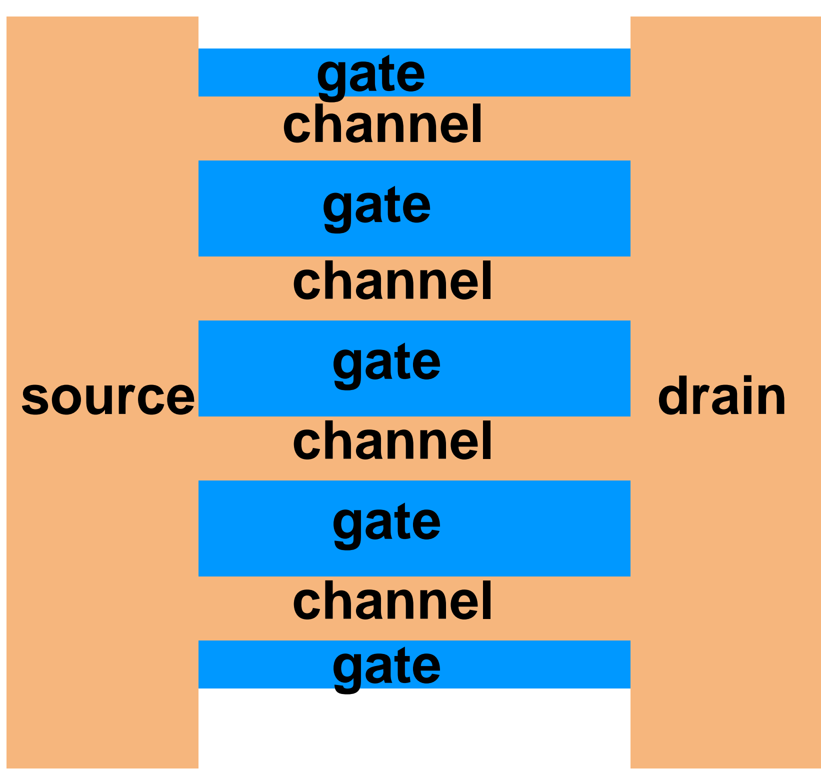


Multiple Channels

- **Can be vertical and horizontal**







Double-Gate FET – Outstanding Issues

- **Threshold voltage setting**
  - Gate workfunction? Doped silicon channel?
- **Multiple threshold voltage on-chip**
  - Variable gate workfunction? Doped silicon channel?
- **Transport of carriers in thin silicon channels**
- **Layout design tools**
  - automatic design migration from conventional CMOS
- **FinFET**
  - fin thickness tolerance
  - device width quantization
- **Planar double-gate**
  - self-aligned integration scheme
- **Yet to be demonstrated**
  - CMOS, SRAM and ring oscillator - optimized parasitic capacitances
  - device density
- **Back-gate FET (4th terminal device) may be key to solving standby power problem - needs circuit level study**

Fully silicided gates with tunable workfunction (IEDM 2003)

IEDM 2003, SSDM 2003

SOI Conf. 2003

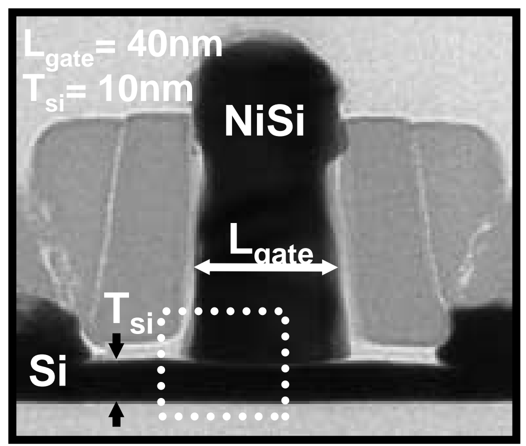
Spacer lithography

IEDM 2003

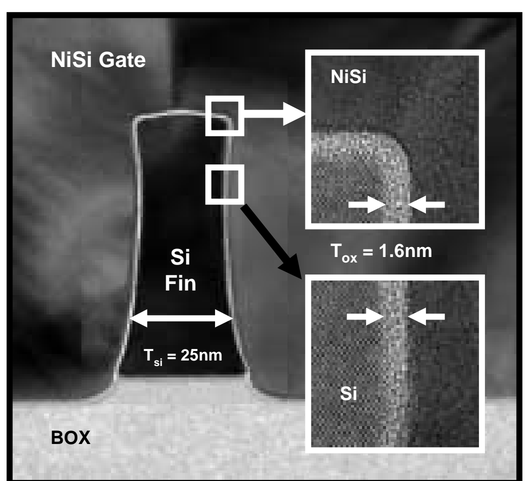
Technology Features Should be Additive

- **New materials and new device structures**
  - (a) Ultra-thin body FET
  - (b) Double- (or Multi-) gate FET
  - (c) Strained Si (bulk, on insulator)
  - (d) Ge (bulk, on insulator)
  - (e) High-k gate dielectrics
  - (f) Metal gates
  - (g) Crystal orientation

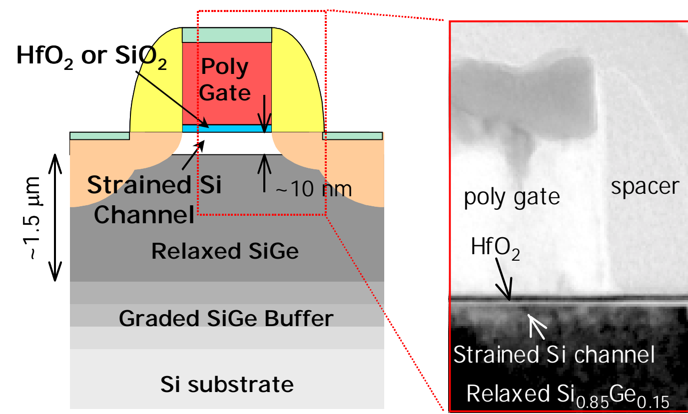
Demonstrated:
(a)+(c), (a)+(d), (a)+(e), (a)+(f)
(b)+(a) (b)+(f), (b)+(g),
(c)+(e), (c)+(d)
(d)+(e), (d)+(f), (d)+(e)+(f)
(e)+(f)
(g)



J. Kedzierski et al., *IEDM*, paper 18.4, 2003.

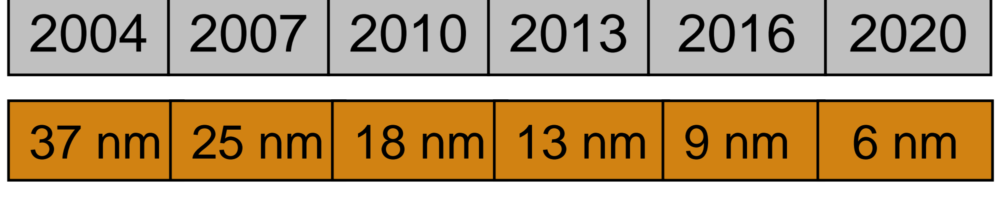


J. Kedzierski et al., *IEDM*, p. 247, 2002.



K. Rim et al., *Symp. VLSI Tech.*, p. 12, 2002.

Time Horizon



	2004	2007	2010	2013	2016	2020
Physical Gate	37 nm	25 nm	18 nm	13 nm	9 nm	6 nm

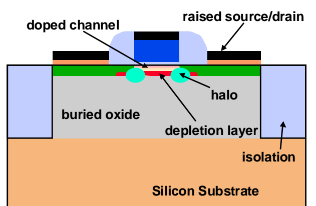
Ultrathin SOI

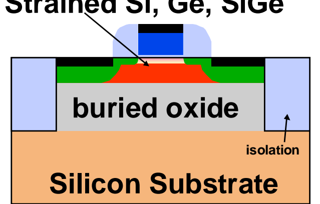
High *k* gate dielectric

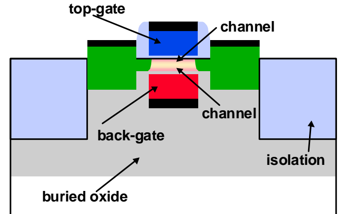
Strained Si, Ge, SiGe

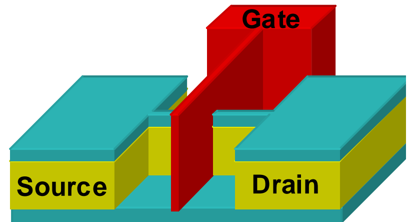
Double-Gate CMOS

FinFET

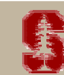








Evolutionary → Revolutionary



A Possible Path

Drain Current (log(I_D))

Gate Voltage (V_{GS})

S < kT/q

Molecular devices

Spintronics

Fine-grain FLA / PLA

Quantum cascade

Nanotube

Nanowire

3D, heterogeneous integration

Double-Gate / FinFET

top-gate
channel
channel
back-gate
isolation
buried oxide

Gate
Source
Drain

Embedded memory

Time

Research Directions

- **Red Zone topics**
  - Transport enhanced FETs: fundamental physics (Ge, III-V)
  - Novel memory technologies – device and fabrication
- **Between Red Zone and Blue Sky**
  - S < kT/q device
  - Carbon nanotubes, semiconductor nanowires: FET and other device applications
  - Nano, Now!
    - Nanotechnology for manufacturing of devices already known today
    - Device application of templated assembly (e.g. di-block co-polymer)
  - 3D integration, large area electronics, focusing on devices
- **Blue Sky**
  - Nanodevice array logic, functional logic array
  - Re-configurable logic – circuits, devices, fabrication
  - Bio-scaffolding, bio-assembly

Questions? Please contact:

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