Silicon Devices at the “End of Scaling” – Opportunities and Challenges

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Center for Integrated Systems 2004.10.05 Department of Electrical Engineering
Elements of an Electronic System

- Logic
  - execution units, bus, drivers, glue logic
- Memory
  - memory hierarchy - cache, data bank, NVRAM, storage
- Communication
  - on-chip, chip-to-chip, board-to-board...
- User Interface
  - sensors, input devices, output devices
What is Classical Scaling?

- **Scaling is the synchronous reduction, year on year, of technology dimensions governing the performance of silicon technology. Scaling:**
  - Improves device performance at ever lower power per function.
  - Enables increased chip functionality through added density.
  - Improves business financials through die size reduction.

- **Why would the end of classical scaling be a highly disruptive event?**
  - Scaling and progress in silicon technology have been synonymous for decades.

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**Scaled Device**

**SCALING:**
- Voltage: \( V/\alpha \)
- Oxide: \( t_{ox}/\alpha \)
- Wire width: \( W/\alpha \)
- Gate width: \( L/\alpha \)
- Diffusion: \( x_d/\alpha \)
- Substrate: \( \alpha \cdot N_A \)

**RESULTS:**
- Higher Density: \( \sim \alpha^2 \)
- Higher Speed: \( \sim \alpha \)
- Power/ckt: \( \sim 1/\alpha^2 \)
- Power Density: \( \sim \text{Constant} \)

Source: IBM
Some Things do not Scale Exactly…

**SCALING:**
- Voltage: $V/\alpha$
- Oxide: $t_{ox}/\alpha$
- Wire width: $W/\alpha$
- Gate width: $L/\alpha$
- Diffusion: $x_{d}/\alpha$
- Substrate: $\alpha * N_A$

**RESULTS:**
- Higher Density: $\sim \alpha^2$
- Higher Speed: $\sim \alpha$
- Power/ckt: $\sim 1/\alpha^2$
- Power Density: $\sim$Constant

Why deviate from "ideal" scaling?
- unacceptable gate leakage/reliability
- additional performance at higher voltages

What is the consequence of this deviation?
- a dramatic rise in power density

Source: IBM
Active vs. Passive Power

- **Power components:**
  - Active power
  - Passive power
    - Gate leakage
    - Sub-threshold leakage (source-drain leakage)

Power components:
- Active power
- Passive power

![Gate Stack](image)

Gate dielectric approaching a fundamental limit (a few atomic layers)

![Power Density](chart)

Power Density (W/cm²)

Active Power

Passive Power

1994 → 2004

Source: IBM

Stanford University
Department of Electrical Engineering

H.-S. Philip Wong

2004.10.05
Power is Limiting Microprocessor Frequencies

Server microprocessors cannot simultaneously utilize all their transistors due to power limitations.

- Moore’s law is continuing with respect to transistor density, although at a reduced pace.
- Workload demands are highly variable.
- New methods to utilize silicon density scaling will be developed to accommodate diverse workloads while managing power constraints.

Source: IBM
Key Challenges

- Power / performance improvement and optimization
- Variability
- Integration
  - Device, circuit, system
Let’s start with logic devices
Improvement Opportunities

- Threshold Voltage ($V_T$)
- Gate Length Scaling

Innovations:
- materials
- device structure

- Thin gate dielectric
- Doping: sharp halo & junction profiles
- Thin silicon body

Gate length scaling

Threshold Voltage ($V_T$)

Gate Length ($L_G$)

- Raised source/drain
- Channel
- Well doping
- Depletion layer
- Halo
- Buried oxide
- Isolation

Silicon Substrate
Improvement Opportunities

Charge density: subthreshold slope

Innovations:
- materials
- device structure

Mobility
Saturation velocity
Ballistic transport

Drain Current (V_{DS})
Gate Voltage (V_{GS})

Drain Current (I_D)

Mobility
Contact & series resistance
# Single Gate Non-classical CMOS

<table>
<thead>
<tr>
<th>Device</th>
<th>Transport-enhanced Devices</th>
<th>Ultra-thin Body</th>
<th>Source/Drain Engineered Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Concept</td>
<td>Strained Si, Ge, SiGe or still other semiconductor; on bulk or SOI</td>
<td>Fully depleted SOI with body thinner than 10 nm</td>
<td>Ultra-thin channel and localized ultra-thin BOX</td>
</tr>
<tr>
<td>Application/Driver</td>
<td>HP CMOS</td>
<td>HP, LOP, and LSTP CMOS</td>
<td>HP, LOP, and LSTP CMOS</td>
</tr>
</tbody>
</table>

Source: ITRS, J. Hutchby
# Multiple Gate Non-classical CMOS

<table>
<thead>
<tr>
<th>Device</th>
<th>Multiple Gate FET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N$-Gate ($N&gt;2$) $FET$</td>
<td>Double-gate $FET$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Concept</th>
<th>Tied gates (number of channels &gt;2)</th>
<th>Tied gates, side-wall conduction</th>
<th>Tied gates planar conduction</th>
<th>Independently switched gates, planar conduction</th>
<th>Vertical conduction</th>
</tr>
</thead>
</table>

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<tr>
<th>Application/Driver</th>
<th>HP, LOP, and LSTP CMOS</th>
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</tr>
</thead>
</table>

Source: ITRS, J. Hutchby
Transport Enhanced Devices

- Wafer-scale strained Si
  - Strained Si on relaxed SiGe buffer on bulk Si
  - Strained Si on relaxed SiGe buffer on insulator
  - Strained Si directly on insulator
- Local strain
  - Dielectric films
  - Isolation (STI), device size dependent structures
  - SiGe in recessed source/drain
- Crystal orientation and current flow direction
- Other materials
  - Bulk Ge
  - Ge on insulator
  - Strained Ge
Strained Silicon

Strained Si/SiGe Bulk MOSFET

SGOI (SiGe-on-Insulator) MOSFET

SSDOI MOSFET

B. Lee et al., *IEDM* 2002
Strain-Dependence of Mobility

- Mobility enhancements consistent with amount of strain even for strained silicon on insulator

Short Channel Strained Silicon FETs

- **Key challenges:**
  - maintain performance enhancement at short channels under high field transport
  - material defect reduction


Uniaxial Strain vs Biaxial Strain

Traditional Approach
- Graded SiGe Layer
- Biaxial Tensile Strain

Intel's 90nm Technology
- Selective SiGe S-D
- Uniaxial Compressive Strain for PMOS
- Tensile Si$_3$N$_4$ Cap
- Uniaxial Tensile Strain for NMOS

Source: Intel
Uniaxial Strain

**Strained Si + High-k**

<table>
<thead>
<tr>
<th>Mobility at $E_{\text{eff}} = 1.4$ MV/cm</th>
<th>Substrate</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Dielec.</td>
<td>CZ Si</td>
<td>Strained Si</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>SiO$_2$/CZ</td>
<td>SiO$_2$/SS</td>
</tr>
<tr>
<td></td>
<td>173</td>
<td>271</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>HfO$_2$/CZ</td>
<td>HfO$_2$/SS</td>
</tr>
<tr>
<td></td>
<td>134</td>
<td>218</td>
</tr>
</tbody>
</table>

Surface Orientation & Current Flow Direction

(100) surface

(110) surface

Hole Mobility (cm$^2$V$^{-1}$S$^{-1}$)

Electron Mobility (cm$^2$V$^{-1}$S$^{-1}$)

M. Yang et al., IEDM 2003
Hybrid Orientation Technology (HOT)

- **nFET on (100) epi-Si**
  - (100) SOI
  - STI
  - STI
  - (100) Silicon handle wafer

- **nFET on (100) SOI**
  - (100) SOI
  - STI
  - STI
  - (110) Silicon handle wafer

- **pFET on (110) SOI**
  - (110) SOI
  - Oxide
  - STI
  - STI
  - (100) Silicon handle wafer

- **pFET on (110) epi-Si**
  - (110) SOI
  - Oxide
  - STI
  - STI
  - (100) Silicon handle wafer

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M. Yang et al., *IEDM 2003*
pFET Performance Enhancement for HOT

<table>
<thead>
<tr>
<th>$I_{off} =$</th>
<th>$I_{on}$</th>
<th>$I_{dlin}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>100nA/µm</td>
<td>+33%</td>
<td>+45%</td>
</tr>
<tr>
<td>10nA/µm</td>
<td>+44%</td>
<td>+58%</td>
</tr>
</tbody>
</table>

M. Yang et al., *IEDM* 2003
Germanium FET

High Mobility Ge PMOSFETs with ZrO₂ Gate Dielectric

- 1st demo of metal gate and hi-κ on Ge MOSFETs
- EOT upto 0.5 nm demonstrated
- 3× mobility vs. Hi-k Si p-MOSFETs
- 400°C maximum temperature process
- Work on VLSI CMOS structures in progress

Chui, Kim, McIntyre, Saraswat, IEDM 2002
Nanoscale Si FET (Gate Length = 6 – 8 nm)

Key Issues for Ultra-Thin Body FETs

- Raised source/drain
- Thin gate dielectric
- Uniform, thin (< 10 nm) channel thickness
- Minimize surface roughness
- External resistance in extremely thin Si
- Carrier mobility in thin channels
From Bulk to Double-Gate FET

Improves:
- Short-channel control
- Subthreshold slope
- Mobility

Bulk FET

Ultra-thin body SOI FET

Double-Gate FET

Bulk NFET w/ Na=2x10^{18} cm^{-3}

From: M. Ieong et al., *MRS Spring Meeting*, 2003.
Double-Gate FET Fabrication

Horizontal channel:
- Bury back-gate under single crystal channel
  - wafer bonding
  - selective epitaxial Si growth
- Back-gate not easily accessible
- Self-aligned gates required

Vertical channel:
- Lithography and patterning 3-4x more stringent (5-10 nm required)
  - e-beam litho
  - sidewall techniques
- Gates accessible from the side

FinFET Fabrication

Source Pad → Fin → Gate → Drain Pad

Poly-Si
Crystalline-Si

FinFET Double-Gate FET


NiSi Gated Double-Gate FinFET

- Undoped Body
- Epitaxy RSD
- No body doping
- Metal gates


- $W = 2H_{\text{fin}}$
  - nFET 1.3mA/µm (at $V_{dd}=1.5$V)
  - pFET 0.8mA/µm (at $V_{dd}=1.5$V)
- nFET $V_t = 0.1$V
- pFET $V_t = -0.23$V
- $S = 70$mV/dec
2-Gates, 3-Gates, 4-Gates ... Multi-Gate FETs

- Put gates closer to channel
- Control short-channel effects better

R. Chau et al., SSDM, 2002.

Triple-Gate FET

R. Chau et al., SSDM, 2002.
Multiple Fins

Optical or e-beam lithography pitch

Conventional lithography

Optical or e-beam lithography pitch

Spacer lithography

Removal of dummy and Si-fin etch

Fin pitch

Multiple Fins: Triple-gate

R. Chau et al., SSDM, 2002.
Multiple Channels

- Can be vertical and horizontal
Double-Gate FET – Outstanding Issues

- **Threshold voltage setting**
  - Gate workfunction? Doped silicon channel?
- **Multiple threshold voltage on-chip**
  - Variable gate workfunction? Doped silicon channel?
- **Transport of carriers in thin silicon channels**
- **Layout design tools**
  - automatic design migration from conventional CMOS
- **FinFET**
  - fin thickness tolerance
  - device width quantization
- **Planar double-gate**
  - self-aligned integration scheme
- **Yet to be demonstrated**
  - CMOS, SRAM and ring oscillator - optimized parasitic capacitances
  - device density
- **Back-gate FET (4th terminal device) may be key to solving standby power problem**
  - needs circuit level study

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**Fully silicided gates with tunable workfunction (IEDM 2003)**

**I EDM 2003, SSDM 2003**

**SOI Conf. 2003**

**Spacer lithography**

**IEDM 2003**
Technology Features Should be Additive

- **New materials and new device structures**
  - (a) Ultra-thin body FET
  - (b) Double- (or Multi-) gate FET
  - (c) Strained Si (bulk, on insulator)
  - (d) Ge (bulk, on insulator)
  - (e) High-k gate dielectrics
  - (f) Metal gates
  - (g) Crystal orientation

Demonstrated:
(a)+(c), (a)+(d), (a)+(e), (a)+(f)
(b)+(a) (b)+(f), (b)+(g),
(c)+(e), (c)+(d)
(d)+(e), (d)+(f), (d)+(e)+(f)
(e)+(f)
(g)

Time Horizon

<table>
<thead>
<tr>
<th>Year</th>
<th>Physical Gate</th>
<th>37 nm</th>
<th>25 nm</th>
<th>18 nm</th>
<th>13 nm</th>
<th>9 nm</th>
<th>6 nm</th>
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<tbody>
<tr>
<td>2004</td>
<td>back-gate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2007</td>
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<td></td>
<td></td>
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<tr>
<td>2010</td>
<td>isolation</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>2013</td>
<td>buried oxide</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>2016</td>
<td>halo</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2020</td>
<td>raised source/drain</td>
<td></td>
<td></td>
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<td></td>
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</tr>
</tbody>
</table>

- Ultrathin SOI
- High $k$ gate dielectric
  - Strained Si, Ge, SiGe
- Double-Gate CMOS
  - Strained Si, Ge, SiGe
  - buried oxide
  - Silicon Substrate
- FinFET
  - Gate
  - Source
  - Drain

Evolutionary  Revolutionary
A Possible Path

- **Molecular devices**
- **Spintronics**
- **Quantum cascade**

**Double-Gate / FinFET**

**3D, heterogeneous integration**

**Source**

**Gate**

**Drain**

**Nanowire**

**Nanotube**

**Fine-grain FLA / PLA**

**Embedded memory**

**Time**

- **S < kT/q**
- **Gate Voltage (V_{GS})**
- **Drain Current (log(I_D))**
Research Directions

- **Red Zone topics**
  - Transport enhanced FETs: fundamental physics (Ge, III-V)
  - Novel memory technologies – device and fabrication

- **Between Red Zone and Blue Sky**
  - \( S < kT/q \) device
  - Carbon nanotubes, semiconductor nanowires: FET and other device applications
  - Nano, Now!
    - Nanotechnology for manufacturing of devices already known today
    - Device application of templated assembly (e.g. di-block co-polymer)
  - 3D integration, large area electronics, focusing on devices

- **Blue Sky**
  - Nanodevice array logic, functional logic array
  - Re-configurable logic – circuits, devices, fabrication
  - Bio-scaffolding, bio-assembly
Questions? Please contact:

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