6.012 DP: CMOS Integrated Differential Amplifier

Tony Hyun Kim

Contents

1 Introduction

This brief report accompanies my solution to the Spring 2008 6.012 project concerning the design of a CMOS integrated differential amplifier. For an organized presentation of the results, please consult the attached solution worksheet. Instead, the intent of this report is to informally describe the intuition behind my approach.

The circuit is operated from ±1.5V supplies, and must meet the following performance criteria:

1. Small-signal gains:
   (a) Differential-mode voltage gain, $A_{vd} \geq 500,000$.
   (b) Common-mode voltage gain, $A_{vc} \leq 0.005$.
2. Common-mode rejection ratio, $A_{vd}/A_{vc} \geq 10^8$.
3. Small-signal output resistance, $r_{out} \leq 100\,\Omega$.
4. Maximum output voltage swing into a $300\,\Omega$ load, $|v_{OUT}|_{max} \geq 0.6$ V.
5. Minimum common-mode input voltage range, $|v_{IC}|_{min} \geq 0.8$ V.
6. Total quiescent power dissipation not to exceed 1.5 mW.

7. Value of $|V_{ID}| = |V_{IN1} - V_{IN2}|$ required to make $V_{OUT} = 0$ V must be less than 5 microvolts.

Over the course of this document, I will verify that all of these conditions are met by my design.

My general approach was to take, for almost every transistor, the minimum gate-to-source voltage of $|V_{GS}| = 0.6$ V. This is motivated by two reasons. First, with the bias current fixed, many of the performance characteristics are improved as we take the smallest possible bias. Secondly, the narrow power supply rails do not offer much room for experimentation. In fact, in some cases the minimal bias of 0.6 V is literally forced upon us by the performance requirements (in particular, the voltage ranges (4) and (5) of the previous list) in conjuction with the power supply limitations.

In addition, I was able to halve the amount of work involved, by maximizing the symmetry of the circuit. For instance, in the two vertical chains that constitute the current mirror stage (Figure 2), I saw no reason to complicate the design by choosing a different set of device parameters for each chain.

The project document provided by 6.012 staff characterizes the overall circuit as consisting of several stages: the Lee-load gain stage, the current-mirror cascode gain stage, and the output stage. I will follow this framework in my discussion of the circuit. Brief comments regarding the biasing circuitry are relegated to the end.

2 Common-source gain stage with Lee load

This gain stage involves transistors Q_9, Q_{10}, Q_{11}, Q_{12}, Q_{13}, Q_{14}, Q_{15} as shown in Figure 1.

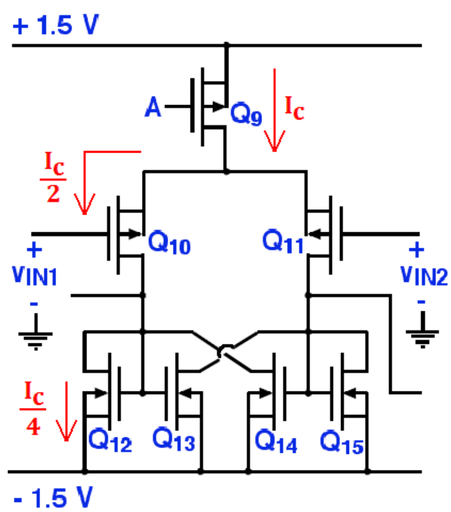

Figure 1: Common-source gain stage with Lee load. The current through the bias transistor Q_9 is denoted I_C. Note how this current splits among the branches downstream.

Let I_C denote the bias current set up by Q_9. From our work in PS #10 on the small-signal gains of the Lee load, we know the differential-mode and common-mode gains to be:

$$A_{vd} = \frac{g_{m10}}{g_{o10} + 2g_{o12}} = \frac{\frac{-2(I_C/2)}{|V_{GS}-V_T|_{10}}}{\lambda_{10}(I_C/2) + 2\lambda_{12}(I_C/4)} = \frac{-1}{\frac{\lambda_{10}+\lambda_{12}}{2}(V_{GS} - V_T)_{10}} \tag{1}$$

$$A_{vc} \approx \frac{-g_{o9}}{4g_{m12}} = \frac{-\lambda_9 I_C}{4 \cdot \frac{2\cdot(I_C/4)}{(V_{GS}-V_T)_{12}}} = -\frac{1}{2}\lambda_9(V_{GS}-V_T)_{12} \quad (2)$$

Hence, as indicated earlier, both characteristics are improved if we take the minimum allowed bias of 0.6V. Furthermore, Eqs. 1 and 2 show that we also should take Q_9, Q_{10} and Q_{12} (thereby all of the transistors in this stage, by symmetry) to be double-length devices. This halves $\lambda = \frac{1}{V_A} \propto \frac{1}{L}$ as to give the optimum characteristics.

By choosing $(V_{GS} - V_T)_{12} = 0.6V$, we are setting the quiescent output of this stage at -0.9V. This output node is also the drain of Q_{10} and Q_{11}. It is then clear that Q_{10} and Q_{11} definitely will not go out of saturation at the negative common mode input of -0.8V.

In addition, we must also make sure that all transistors are in saturation for a positive common-mode input of 0.8V. For such inputs, the source tails of Q_{10} and Q_{11} are pushed up to 1.4V at the least, since the very minimum allowed gate-to-source bias is 0.6V. This then forces node A to take on 0.9V. If A were any higher, we would violate the necessary V_{SG} bias for Q_9. If instead node A were lower than 0.9V, Q_9 would not be operating in saturation at the extreme common-mode input of 0.8V. With these voltage biases, the circuit successfully accomodates the common-mode input range specified by (5).

Finally, to determine the device sizes, we minimize I_C. In this task, we only need to recognize that the n-channel transistors in the Lee load are the limiting devices, since they constitute the branch carrying the smallest current. Absolute minimum K-factor for the n-channel device Q_{12} is $K_{12} = 1$ mA/V^2, yielding $I_{D12} = I_C/4 = \frac{1}{2}(1mA/V^2)(0.1V)^2 = 0.005mA$.

In summary, the gains and the current consumption of this stage are $A_{vd} = 100$, $A_{vc} = 0.005$ and $I_C = 0.02mA$.

3 Cascode current mirror gain stage

In the analysis of this second gain stage, I have relied upon Prof. Fonstad's results rather than conducting the small-signal network analysis myself. On the other hand, I have decided to make the two branches symmetric. Hence, they each carry a bias current of I_D. (See Figure 2.) The small-signal differential gain is:

$$\begin{aligned} A_{vd} &= \frac{2g_{m23}}{g_{o17}g_{o19}/g_{m19} + g_{o23}g_{o21}/g_{m21}} \\ &= \frac{8}{(V_{GS}-V_T)_{23}(\lambda_{17}\lambda_{19}(V_{SG}-|V_T|)_{19} + \lambda_{21}\lambda_{23}(V_{GS}-V_T)_{21})} \\ &= \frac{80V^{-1}}{\lambda_{17}\lambda_{19}(V_{SG}-|V_T|)_{19} + \lambda_{21}\lambda_{23}(V_{GS}-V_T)_{21}} \end{aligned} \quad (3)$$

where the last line follows after a little algebra, and also after recognizing that $(V_{GS}-V_T)_{23}$ has already been determined by our biasing of the previous Lee-load gain stage. Under quiescent conditions, the outputs of the first stage sit at $-0.9V$, which gives $(V_{GS} - V_T)_{23} = 0.1V$.

We continue on with Eq. 3 by setting the remaining biases to 0.6V as well. This can be consistently achieved by setting the voltage bias points C and D to the appropriate level. In particular, C: 0.8V and D: -0.8V work nicely, without putting neighboring transistors out of saturation. These levels for C and D also provide a large voltage range for the output node as illustrated in Figure 2. For the task at hand, these choices yield:

$$A_{vd} = \frac{800V^{-2}}{\lambda_{17}\lambda_{19} + \lambda_{21}\lambda_{23}} \quad (4)$$

At first sight, Eq. 4 suggests that we choose all devices to be double-length, in order to maximize the differential gain. However, it can easily be shown that the CMRR can be improved, if we let $\lambda_{17} = 0.2V^{-1}$ instead. With the remaining transistors (Q_{19}, Q_{21}, Q_{23}) as double-length devices, we obtain the following small-signal differential gain:

$$A_{vd} = 2.67 \times 10^4 \tag{5}$$

We also have the expression for common-mode gain, courtesy Prof. Fonstad:

$$A_{vc} = -\frac{g_{m23}}{g_{m17}} = -\frac{\lambda_{23} I_D}{\lambda_{17} I_D} = -\frac{1}{2} \tag{6}$$

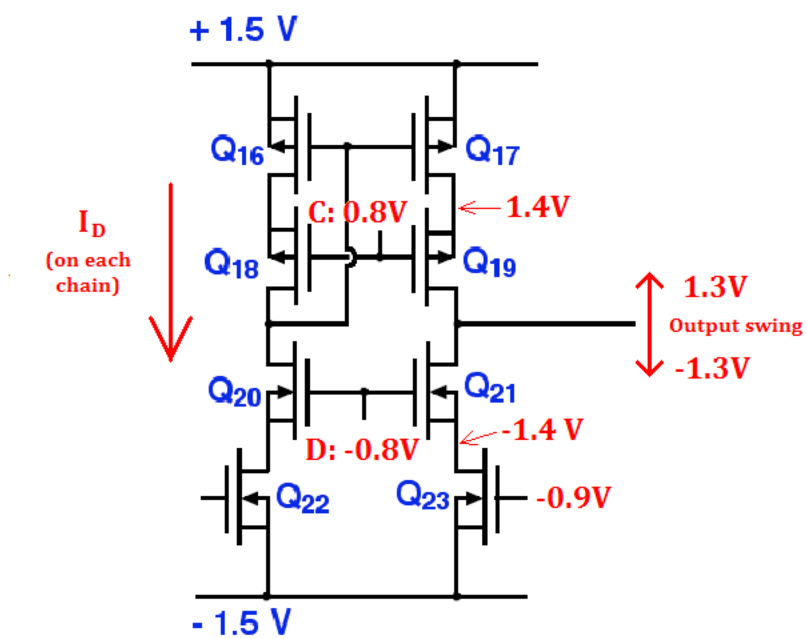

Figure 2: The choice of C: 0.8V and D: -0.8V gives a large voltage range for the output node without knocking any transistor out of saturation. The bias current I_D is also indicated.

The current I_D can be determined by recognizing the n-channel devices Q_{21} and Q_{23} as the devices that limit the minimization of current. We conclude: $I_D = 0.005mA$.

In this discussion, I have specified the sizes and biasing conditions of Q_{17}, Q_{19}, Q_{21} and Q_{23}. The transistors of the opposite branch (Q_{16}, Q_{18}, Q_{20} and Q_{22}) are determined by symmetry.

To conclude, the overall gains are (with an open load):

$$A_{vd}^{overall,open} = A_{vd}^{LL} \times A_{vd}^{CM} = 100 \times 2.67 \times 10^4 = 2.67 \times 10^6 \tag{7}$$

$$A_{vc}^{overall,open} = A_{vc}^{LL} \times A_{vc}^{CM} = 0.005 \times 0.5 = 0.0025 \tag{8}$$

$$CMRR = 1.07 \times 10^9 \tag{9}$$

We have therefore satisfied the gain criteria.

4 Push-pull output stage

In this final stage, the output resistance and voltage swing requirements place somewhat stringent restrictions on the device parameters. We begin by discussing the output resistance.

4.1 Output resistance

From the output port, the equivalent resistance looking into the circuit is that of two parallel source-follower subcircuits. Furthermore, recall that the output conductance of a source-follower increases when the large-signal current through the transistor is increased. It then follows that the worst-case, maximum output resistance will occur when $v_{OUT} \approx 0V$. This is so, because when the output is displaced from zero, either Q_{28} or Q_{29} will be very active, thereby providing at least one low resistance path (of a source-follower with a high bias current).

Let I_H denote the quiescent current through the push-pull (Q_{28} and Q_{29}) when $v_{OUT} \approx 0V$. Then, the output resistance is calculated to be:

$$r_{out} = \frac{1}{g_{m28} + g_{m29}} = \frac{1}{\frac{2I_H}{(V_{GS}-V_T)_{28}} + \frac{2I_H}{(V_{SG}-|V_T|)_{29}}} \tag{10}$$

Again, I choose the two biases to be symmetric:

$$r_{out} = \frac{(V_{GS} - V_T)_{28}}{4I_H} \leq 100\,\Omega \tag{11}$$

We are free to choose $(V_{GS} - V_T)_{28} = 0.1V$, in order to limit quiescent power consumption. Then, the inequality of Eq. 11 becomes:

$$\begin{aligned} I_H &\geq \frac{1}{4} \cdot \frac{|V_{GS} - V_T|}{100\,\Omega} \\ &\geq 0.25\,mA \end{aligned} \tag{12}$$

which takes up half our current budget! Fortunately, because the other parts of the circuit are not so current-hungry, we are able to satisfy this demand without further complications.

In this section, we have specified the gate-to-source bias and the current through Q_{28}. In turn, this then specifies $K_{28} = 50mA/V^2$.

4.2 Output voltage swing

The push-pull must be capable of delivering at least a $0.6V$ high-output when loaded by $300\,\Omega$. By design, at such a high-end swing, only Q_{28} is active (i.e. is “pushing” current) while Q_{29} is in cutoff. This scenario is illustrated in Figure 3.

In Figure 3, the current into the resistor must be provided entirely by Q_{28}, which requires:

$$\begin{aligned} 2mA &= \frac{1}{2}K_{28}(V_{GS} - V_T)^2 = \frac{1}{2}50mA/V^2(V_{GS} - V_T)^2 \\ V_{GS} &= V_T + \sqrt{\frac{4mA}{50mA/V^2}} = 0.783V \end{aligned} \tag{13}$$

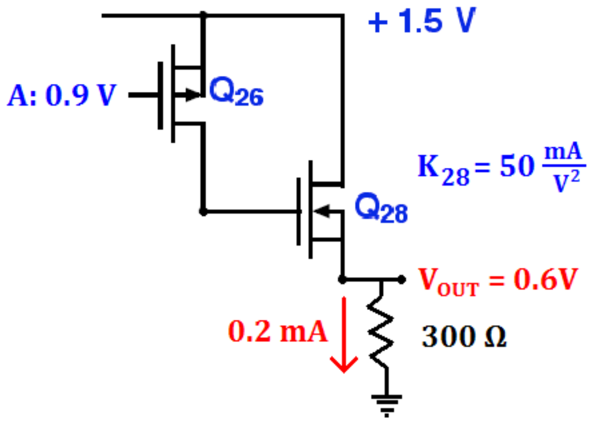

Figure 3: This circuit fragment illustrates the demands imposed on Q_{28} by the $0.6V$ voltage swing requirement when loaded by $300\,\Omega$.

Since $V_S = V_{OUT} = 0.6V$, we have:

$$V_{G28} = V_{GS} + 0.6V = 1.383V \tag{14}$$

which shows that we barely avoided kicking Q_{26} out of saturation. (It is precisely for this reason that I did not conduct a more accurate calculation for the maximum V_{OUT}. We are very close to the limit already with $0.6V$.) Here is a direct tradeoff between power consumption and output voltage swing range. If we were to choose larger K-factors for Q_{28} and Q_{29}, we can extend the output range (in addition to having smaller r_{out}!) but we'll have to settle for a larger quiescent current. My design preference was to minimize power consumption.

A similar analysis can be performed on the negative swing, when Q_{29} is active.

4.3 Push-pull biasing circuitry Q_{24}, Q_{25}, Q_{26}, Q_{27}

In this subsection, we regard the drain nodes of Q_{19} and Q_{21} (the output of the current mirror stage) to be the input of the push-pull. The concern here is to communicate this input voltage to the output of the push-pull, without incurring significant distortions.

It is well-known that directly driving the gates of a push-pull will result in the so-called "crossover distortion," as shown below in Figure 4. In the case of MOSFETs, this undesirable effect arises due to the finite threshold voltage.

The design project circuit addresses this issue by biasing the push-pull (Q_{28} and Q_{29}) by a proper choice of Q_{24}, Q_{25}, Q_{26}, Q_{27}, selected to compensate for the threshold voltage. We note, however, that the solution cannot be perfect, as we have seen previously that the gate-to-source voltages for Q_{28} and Q_{29} are not constant over the operating range. On the other hand, Q_{26} and Q_{27} are configured in a way to provide a constant gate-to-source bias throughout their operation. (This latter claim is only approximately true. It is valid only because we are not taking into account the Early effect in this large-signal analysis.)

Suppose $V_{OUT} > 0V$ so that Q_{28} is active. In other words $V_{GS28} \approx 0.6V$. To compensate for this "intrinsic" 0.6V drop, we bias Q_{27} in a way to provide a boost of $0.6V$. Similarly, we provide a gate-to-source bias of 0.6V on Q_{24} as to offset the $V_{SG} \approx 0.6V$ on Q_{29} during a negative swing.

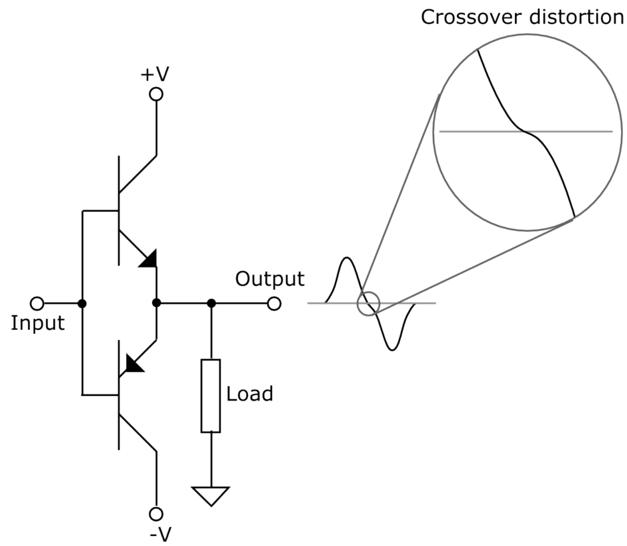

Figure 4: Crossover distortion occurs when driving a push-pull stage directly. Image taken from the Wikipedia article on "Crossover distortion."

Altogether, we are reliably transferring the large-signal voltage from the output of the current mirror to the final output port of the differential amplifer.

Finally, the sizes of transistors Q_{24}, Q_{25}, Q_{26}, Q_{27} are then determined by minimizing the current consumption.

4.4 Small-signal attenuation

In a more detailed small-signal analysis of the push-pull, we find the transfer function to be:

$$v_{out} \approx \frac{R_L}{R_L + \frac{1}{2g_{m28}}} \cdot v_{in} \tag{15}$$

where R_L is the attached load. Using $R_L = 300\Omega$, we find:

$$A_v^{PP} = \frac{300}{300 + \frac{(V_{GS}-V_T)_{28}}{4I_H}} = \frac{3}{4} \tag{16}$$

This gain is compounded on the open-load gains of Eqs. 7 and 8, which give:

$$A_{vd}^{overall} = \frac{3}{4} \cdot A_{vd}^{overall,open} = 2.00 \times 10^6 \tag{17}$$

$$A_{vc}^{overall} = \frac{3}{4} \cdot A_{vc}^{overall,open} = 0.00188 \tag{18}$$

$$CMRR = 1.07 \times 10^9 \tag{19}$$

Hence, our device still satisfies the small-signal gain requirements. (Obviously, the CMRR remains unchanged since the push-pull does not differentiate between differential-mode and common-mode inputs.)

Circuit Description	Current (mA)
Bias chain (A,B)	0.04
Bias chain (C,D)	0.01
Lee-load stage	0.02
Current-mirror stage	$0.01 = 2 \times 0.005$
Push-pull biasing	$0.0075 = 0.005 + 0.0025$
Push-pull	0.25
Total	**0.3375**

Table 1: Current consumption in the differential amplifier circuit.

5 Bias circuitry for voltages A, B, C, D

So far, we have specified the following bias voltages: $A = 0.9V$, $C = 0.8V$, and $D = -0.8V$. It is convenient to set $B = -0.9V$, given the role it plays as a counterpart to A in the output stage.

The determination of the necessary device sizes in the bias chains (Q_1 through Q_8) is a fairly mechanical exercise that we encountered in PS # 10. Needless to say, my design attempts to minimize the quiescent current consumption.

6 Remaining issues

6.1 Quiescent power dissipation

The differential amplifier can consume at most 1.5 mW under quiescent conditions. Because we are operating from $\pm 1.5V$ ideal supplies, this requirement can be reformulated in terms of a current. The device cannot consume more than 0.5 mA at the quiescent point.

Table 1 enumerates the quiescent current consumption through the different branches of the circuit. As can be seen, we are well within the power dissipation requirement.

6.2 Differential input required to make $V_{OUT} = 0V$.

If we short both inputs $V_{IN1} = V_{IN2} = 0V$, the high-impedance node (output of the current-mirror) can be shown to be $0.9V$, upon considering the symmetric structure of the current-mirror subcircuit. It is difficult to say exactly what the overall device's output voltage V_{OUT} will be, since under these conditions, not all transistors are operating in saturation. The most obvious problem area involves Q_{26} and Q_{27}. In any case, we can be certain that the zero-input output will not be zero.

However, a small differential input can be applied to bring the high-impedance node (and hence V_{OUT}) to zero. Because of the large differential gain $A_{vd}^{overall}$ (Eq. 7), the necessary differential input will be minor:

$$|V_{ID}| = \frac{0.9V}{A_{vd}^{overall}} = 0.337\mu V \tag{20}$$

This result exceeds requirement (7) by a significant margin.

References

[1] 6.012 Staff. *Special Problem on Circuit Design.* Spring 2008.

[2] I discussed general design issues with 6.012 classmate Ilan Almog. The collaboration was as sanctioned by the design project guidelines. In particular, final solutions were definitely *not* exchanged nor discussed.