Effects of Testing Parameters in Capacitance-Voltage Profiling of MOS Capacitors

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Abstract—**Small-signal CV curves of MOS capacitors were observed as a function of various test parameters, such as sweep direction and stepping rate of the bias voltage, lighting conditions, and N_2 flow over the device under test. Qualitative differences are found as the bias voltage behavior was changed; in particular, the phenomenon of deep-depletion was observed at faster sweep rates. Furthermore, it is observed that improper lighting conditions and unsintered devices yield CV curves that differ from the direct measurements of the structural properties of the wafer, such as the doping level.**

I. INTRODUCTION

SMALL-SIGNAL capacitance-voltage (CV) measurement is a standard technique for the characterization of semiconductor devices. In this investigation, several square MOS capacitors were fabricated and analyzed under various testing conditions. In particular, the sweep direction and stepping rate of the bias voltage source, lighting conditions, and N_2 flow over the device under test were investigated for their effect on the CV curve of the capacitors.

Based on independent measurements of structural parameters, in particular the doping level of the substrate, the optimal CV testing settings can be discovered.

The experiment was conducted with square $(100\mu m)^2$ and $(500\mu m)^2$ MOS capacitors. This investigation also evaluates electrical consequences of sintering, in which the completed device is annealed in hydrogen gas, neutralizing unbound silicon atoms (i.e. charged impurities) at the oxide interface. It is shown that (lack of) sintering causes a horizontal shift in the CV curve corresponding to a shifted flatband voltage.

II. EXPERIMENT

A. Device Fabrication

MOS capacitors were fabricated on $\rho = 4.3 \pm 1.5\Omega \cdot cm$ n-type Si wafers, corresponding to $N_D \approx 10^{15} cm^{-3}$[1]. The resistivity was obtained by a four-point probe measurement of the sheet resistance, along with the manufacturer's stated wafer thickness of $675 \pm 25\mu m$. Following standard cleans used to remove organic (10 minute, SC-1) and inorganic/metal-ion contaminants (15 minute, SC-2), and HF etch of native oxide, new oxide was grown by a one-hour atmospheric pressure dry oxidation at 1000°C. The thickness of the grown oxide was measured to be $t_{ox} = 483 \pm 43\AA$ by ellipsometry. These reported values are averages over the set of six wafers that were developed for this experiment, hence the relatively large standard deviations.

Subsequently, $2500\AA$ of aluminum was deposited over the oxide by physical vapor deposition. The deposition rate was about $35\AA/s$. The oxide layer on the backside of the wafer was etched by SF_6 gas, in order to open up an electrical contact to the substrate-end of the MOS capacitor.

The capacitors were lithographed as follows: the aluminum-deposited wafer was first treated with hexamethyldisilazane (HMDS) in order to promote photoresist adhesion. Positive photoresist was applied and pre-baked at 95°C for 30 seconds. In the i-Stepper Projection Aligner Wafer Stepper, the wafers were exposed through a mask containing square capacitors of various sizes. The post-exposure bake was at 110°C for 30 seconds. The exposed photoresist regions were dissolved in the development process using TMAH. A gaseous mixture of Cl_2 and BCl_3 was then applied for 30 seconds to the wafers in the reactive ion etching (R.I.E.) metal dry etch system to remove the unprotected aluminum, thereby defining the aluminum gate of the devices.

In order to observe the electrical consequences of sintering, three out of the six wafers were then sintered for 15 minutes at 425°C degrees in 75% flow of forming gas; the other three remained unsintered as controls.

B. CV Measurement

Small-signal capacitance of the MOS capacitor was measured at various bias voltages. The measured capacitances were normalized by the device area to yield capacitance per area, denoted by C^*. At different bias levels, the MOS capacitor behaves in qualitatively different modes (inversion, depletion, accumulation) which have measurable characteristic capacitances, C_{inv} and $C_{acc} = C_{ox}$. The different capacitances can be ascribed to the different charge distributions that arise within the structure at different DC biases. The bias voltage level at which the capacitor transitions between modes is given by the flatband voltage V_{FB}.

These measurements can be utilized to deduce various structural quantities of interest, such as the oxide thickness (t_{ox}), substrate doping level (N_D), and interface impurity charges (Q_f). They are related by the following formulas:

$$t_{ox} = \frac{\epsilon_{ox}}{C^*_{ox}} \tag{1}$$

$$N_D = \frac{4\,|\Phi_F|\,C^{*2}_S}{q\epsilon_s} \tag{2}$$

$$Q_F = -C^*_{ox}\,(V_{FB} - \phi_{MS}) \tag{3}$$

where ϵ are the permittivities and q is the fundamental charge; C_S is the "semiconductor capacitance" which can be deduced from the measured capacitances according to the formula $C^*_{inv} = \frac{C^*_{ox}C^*_S}{C^*_{ox}+C^*_S}$; and finally $\Phi_F = \frac{kT}{q}\log\frac{N_D}{n_i}$ is

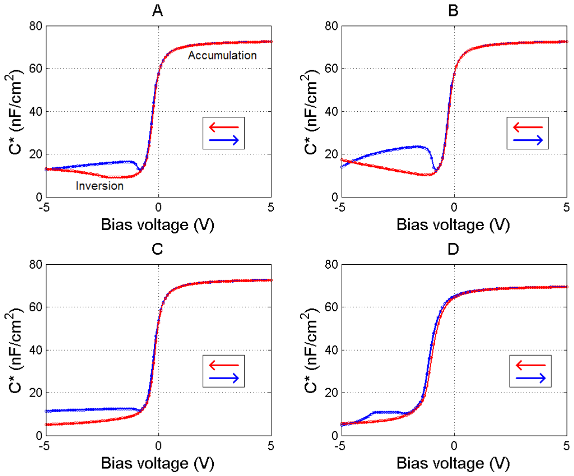

Fig. 1. The CV curves that result from sweeping the bias voltage from -5 to 5 (blue) and from 5 to -5 (red). All other parameters are held constant. (A) $(100\mu m)^2$ capacitor at 3 ms delay; (B) $(100\mu m)^2$ capacitor at 500 ms delay; (C) $(500\mu m)^2$ capacitor at 3 ms delay; (D) $(500\mu m)^2$ non-sintered capacitor at 3 ms delay.

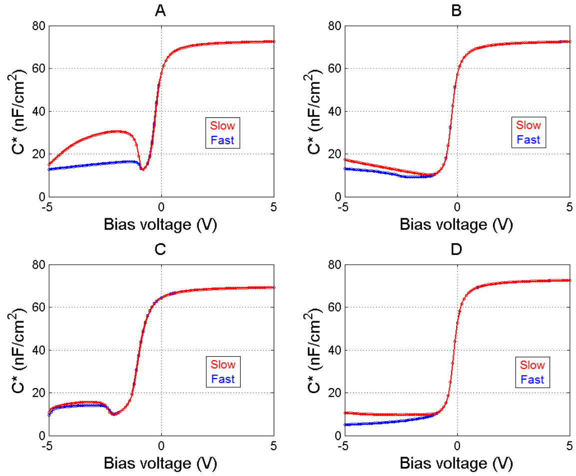

Fig. 2. Variation in CV curves as the bias voltage sweeping rate is varied between a delay of 3 (blue) and 500 ms (red). In other words, blue represents a faster sweep rate than red. All other parameters, including direction of sweep, are held constant. (A) $(100\mu m)^2$ capacitor, -5 to 5; (B) $(100\mu m)^2$ capacitor, 5 to -5; (C) $(100\mu m)^2$ non-sintered capacitor, -5 to 5; (D) $(500\mu m)^2$ capacitor, -5 to 5.

the workfunction of the doped wafer with respect to intrinsic silicon. A good theoretical discussion of these relationships can be found in [1, p. 29].

The HP-4061A CV measurement system offered several adjustable electrical settings, such as the direction of the bias voltage sweep (i.e. $-5V$ to $5V$ vs. $5V$ to $-5V$) and also the stepping rate of the sweep (3 ms vs. 500 ms delay between steps). These settings were varied to study their effects on the resulting CV curves.

The measurement system isolated the wafer under test from room lighting, and offered a feature in which N_2 gas was streamed on the wafer. Both of these parameters were investigated for their effects on the CV measurement.

III. RESULTS AND DISCUSSION

A. *Bias Voltage Sweep Direction*

The effect on the CV curve due to the bias sweep direction is shown in Figure 1. It was generally found that the accumulation portion of the CV curve (right side of graph) is robust against various parameter changes. However, the inversion regime (left side of graph) shows dependence on the sweep direction, with the 5 to -5 sweep consistently yielding a lower inversion-mode capacitance C_{inv}. The lower capacitance is a characteristic signature of the "deep-depletion" phenomenon, explained below.

The inversion mode of pMOS capacitor operation arises when, at significantly negative voltage at the aluminum gate, the MOS capacitor structure accumulates minority carriers at the substrate side of the oxide layer (the "inversion"). Simultaneously, the depletion region ceases to expand since the excess charge at the gate is matched at the inversion layer by the minority carriers. However, since minority carriers are generally not abundant in the bulk, the device may not arrive at the theoretical inversion-state equilibrium, when the applied bias voltage is varied too rapidly with respect to the minority carrier generation time. In such a case, the charge continues to accumulate in the depletion region rather than in the inversion layer. Such a charge configuration leads to a lower than expected overall capacitance, which is clearly exhibited in Figure 1C in the inversion side of the 5 to -5 sweep.

One may expect deep-depletion with the 5 to -5 sweep, since it is in this sweep direction that the device transitions *into* the inversion mode. In other words, the transient dynamics associated with inversion layer formation plays an important role in the resulting CV curves. This hypothesis is consistent with the measured data: the 5 to -5 sweeps consistently yield a lower inversion capacitance, indicating deep-depletion.

B. *Bias Voltage Sweep Rate*

The effect of the sweep rate was also considered. Figure 2 shows the resulting CV curves when the delay between each bias step is set to 3 ms and 500 ms. As with the previous case, only the portion of the curve corresponding to the inversion regime is susceptible to testing parameters. Hence, these comparisons (in particular, Figure 2D) again suggest deep-depletion.

As noted earlier, deep-depletion occurs when the capacitor is subject to conditions that are too rapidly-changing for the generation of minority carriers needed for inversion-mode equilibrium. It is then natural to suspect deep-depletion for faster bias sweeps. This prediction is confirmed by Figure 2, which shows the faster sweep to consistently yield a low capacitance. It appears then that a step deplay of 3 ms is too fast for inversion-mode equilibrium in these devices.

C. *Lighting conditions and* N_2 *flow*

The HP-4061A system provides a metallic casing which shields the device from external light sources. Additionally, nitrogen gas can be flowed over the the wafer throughout the measurement. In the presence of external light, it was found that the inversion capacitance was smaller by an order of magnitude; and the calculated results for N_D were on the order of $10^{16}cm^{-3}$, which is clearly incorrect.

However, there was no appreciable effect of N_2 flow over the substrate. It was suspected that N_2 flow could affect the CV results by changing the temperature of the device. However, according to [1, p. 54] there is only a subtle dependence of the CV curve on the temperature of the device, which lies beyond the precision of this investigation.

D. Sintered vs. Non-Sintered Devices

During the oxidation process, nonnegligible amounts of unbonded, charged silicon atoms are collected at the bulk/oxide interface. These extra charges, as well as any impurities in the fabrication process, are the so-called interface charges Q_F that cause variations in the electrical properties of the device. In particular, the flatband voltage V_{FB} (and correspondingly the other critical voltages that mark the different regimes of MOS capacitor operation) are shifted according to

$$V_{FB} = \phi_{MS} - \frac{Q_F}{C_{ox}} \tag{4}$$

where ϕ_{MS} is the intrinsic work function difference between the aluminum gate and the silicon substrate; Q_F is the amount of impurity charges present; and C_{ox} is the capacitance across the oxide layer. Hence, the presence of interface charges should be controlled in order to minimize device-to-device variations. This is achieved by sintering, in which the unbounded Si atoms are reduced by hydrogen gas.

Figure 3 illustrates the difference between the CV curves of sintered and non-sintered devices. As given by Eq. 4, the CV curve is shifted horizontally. In addition, non-sintered CV measurements appear to give an underestimated value for the semiconductor doping level. According to the direct resistivity measurements, the wafers have a doping level of approximately $10^{15}cm^{-3}$, which may serve as a benchmark for the CV results. The CV analysis of the sintered capacitors yield an average of $N_D = (1.5{\pm}0.7) \cdot 10^{15}cm^{-3}$ while the non-sintered capacitors give $N_D = (6.6 \pm 3.2) \cdot 10^{14}cm^{-3}$. This discrepancy, however, may be explained by the fact that sintered and non-sintered devices were on two different wafers whose doping levels may in fact be different. Without characterizing the specific wafer containing the devices, it is not possible to state conclusively that sintering is necessary for obtaining an accurate measurement of N_D.

In the absence of sintering, $Q_F = (5{\pm}2){\cdot}10^{-8}C/cm^2$ of interface charges were observed, corresponding to approximately $\left|\frac{Q_F}{e}\right| = 2.9 \cdot 10^{11}cm^{-2}$ unbound silicon atoms at the interface. With 15 minutes of annealing, the interface charge was reduced by an order of magnitude to $\left|\frac{Q_F}{e}\right| = 2.7 \cdot 10^{10}cm^{-2}$.

IV. CONCLUSION

Variations in CV curves were observed as a function of testing parameters. While the accumulation regime was robust, it was shown that inversion-regime measurements are highly susceptible to details such as the direction and the rate of the bias voltage sweep. In this investigation, while the dependencies were observed, it was not possible to conclusively identify the testing parameters that yield the most accurate results in structural characterization. Regardless, in order to avoid deep-depletion, a slow -5 to 5V bias sweep is recommended based on this study.

An improved scheme for optimal setting determination is as follows: the measurement of the wafer resistivity (and hence N_D) should be carried out specifically for the wafer that is used in the CV measurements. Since the estimation of N_D through CV data is highly sensitive to the inversion capacitance, one could then use the accuracy of N_D to evaluate the effect of CV testing parameters on the validity of results. Unfortunately, this was not possible with the current data, because the direct resistivity measurements were conducted on two randomly chosen wafers, and the wafers were then shuffled during the processing stages. (Note: other parameters, such as t_{ox} are not quite as useful benchmarks, since it only depends on the accumulation capacitance C_{ox} which has been shown to be robust against testing settings.)

It was demonstrated that lighting conditions can significantly alter the results. Estimates of N_D were an order of magnitude off when the wafer was exposed to external light. N_2 flow had no appreciable effect on CV testing.

Finally, the ability of interface charges to horizontally shift the CV curve was observed. Based on the degree of shift, it was possible to estimate that 15 minutes of sinter reduces the number of interface charges by an order of magnitude.

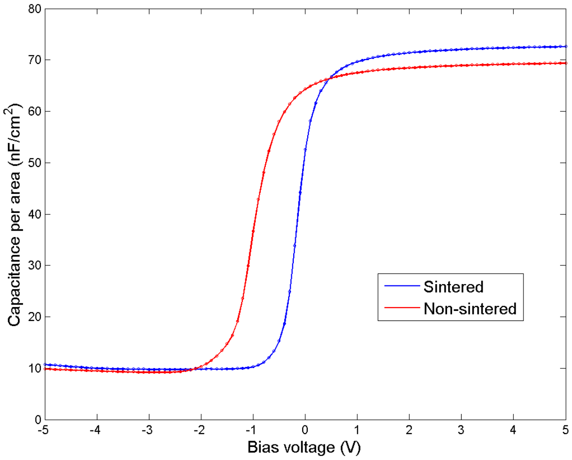

Fig. 3. Differences in CV curves between sintered and non-sintered $(100\mu m)^2$ capacitors. The bias voltage is swept from $5V$ to $-5V$ with a step delay of 500 ms. Sintering removes interface charges within the device which cause horizontal shift of the CV curve. The discrepancy in C_{ox} is ascribed to the fact that sintered and non-sintered devices are located on two different wafers whose oxide thickness vary.

REFERENCES

[1] R. Pierret, *Semiconductor Fundamentals, Volume 2: Modular Series of Solid State Devices*. Addison-Wesley, 1988.