6.152: Solar Cell Design Problem

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1 Introduction

With growing concerns about the world's ever-increasing energy consumption and its consequences, solar energy has become an attractive area of research as well as an important industry. In this report, we discuss issues concerning the design and fabrication of solar cells. Much of the information presented here is taken from the extremely insightful lecture by Dr. Jifeng Liu.

We begin by summarizing the basic operational principles of a solar cell, since we will rely on this information in the later sections.

The solar cell is a device based on the p-n diode. Recall that the p-n diode is constructed by p- and n-type materials that are brought into contact, as shown in Figure 1a. At the junction, a static, so-called "built-in" electric field is generated due to the migration of the mobile carriers.

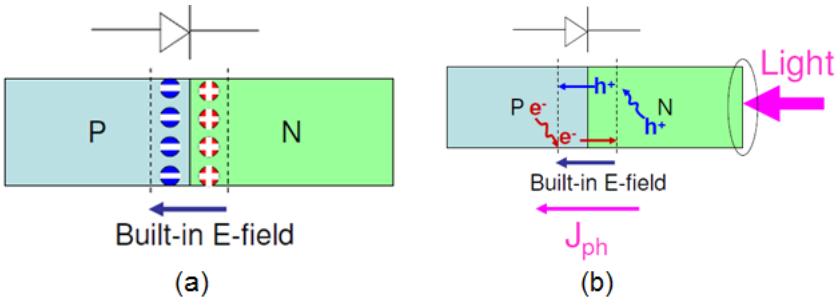

Figure 1: (a) A solar cell is a device based on the p-n diode. Note that, in the p-n diode junction, there is a "built-in" electric field due to the migration of the mobile carriers. (b) Light incident on the solar cell will generate hole-electron pairs, (some of) which then are subjected to the built-in electric field. This directional motion of charges constitute the photocurrent. Image adapted from [1].

Light incident on the solar cell will generate hole-electron pairs. These charged particles are forced to move in their respective directions by the built-in electric field, constituting a photocurrent J_{ph} (towards the anode) as shown in Fig. 1b. This current can exist even when the solar cell is forward-biased, which is the regime in which the solar-cell delivers power to other devices.

2 Solar Cell Design

We have discussed the basic principles of operation of a basic solar-cell. In this report, we discuss the more elaborate structure shown in Figure 2. As can be seen, the core of the device is a p-n junction. However, various modifications have been made in order to boost the efficiency of the device.

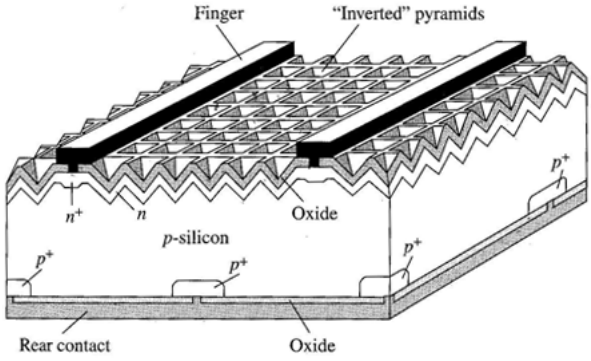

Figure 2: The solar cell discussed in this report.

A1: Why is the top surface of the solar cell patterned with a corrugation or two-dimensional array of "inverted pyramids"?

The corrugation is used in order to decrease reflection losses. As discussed in the introduction, solar electricity begins with light-induced, hole-electron pair generation in the bulk of the device. However, there is a possibility that the light will be reflected at the surface of the cell, before it gets into the bulk. The corrugated surface decreases the overall reflectivity, since the reflected light now has multiple chances to enter the device. This is illustrated in Fig. 3.

A2: Why are the top electrical contacts patterned as long strips of metal or "fingers" while the rear electrical contact is a single continuous layer on the bottom?

We require electrodes with good electrical contact to the solar cell in order to collect the photocurrent. Hence, the rear contact is a single continuous layer. However, we cannot use a similar technique at the top, since it would block off the light ("electrode

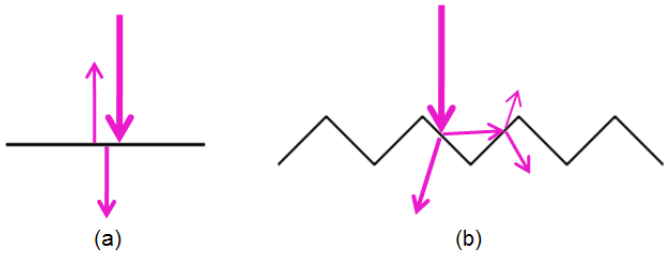

Figure 3: A possible light path for (a) flat surface, and (b) corrugated surface. Note that overall reflection loss is minimized with the corrugated surface, due to multiple opportunities for entry.

shadowing"). Hence, the design employs long strips of metal.

A3: Why is the silicon doped n^+ and p^+ in regions where the electrical contacts touch the silicon?

As shown in Fig. 1a, the generated hole-electron pair are acted upon by the built-in electric field. If, however, the pair is generated outside of the space-charge region (where the built-in electric field is), then non-directional diffusion process is responsible for the motion of the charges. Clearly, a directed drift motion is preferred over non-directional diffusion for efficient carrier transport.

Hence, the n^+ doping is used in order to increase the size of the space-charge region in the p-type bulk. We are increasing the portion of the device in which the built-in electric field exists, thereby promoting drift motion over diffusion.

The backside p^+ layer is included in order to energetically discourage electrons from entering the rear interface, where recombination rates are higher due to increased number of defect levels. (At the interface, we expect more structural irregularities.)

A4: What is the role of the oxide on the top and bottom surfaces of the silicon wafer?

The top oxide layer serves as an anti-reflection coating, again to reduce reflection losses. The bottom oxide layer is designed for higher reflectivities, so that the light remains within the bulk for a longer time, thereby increasing the chance of pair generation.

3 Fabrication Recipe

We begin with a silicon wafer. To be concrete, we have a p-type Si wafer, doped with boron at 10^{15} cm^{-3}.

We wish to build the structure in Fig. 2 with the following dimensions:

- Finger spacing: ~ 5 mm
- Finger width: ~ 100 μm
- Top and bottom contact thickness: ~ 1 μm
- Inverted pyramids: a few μm across $\rightarrow 4$ μm $\times$ 4 μm
- Depth of p-n junction below Si-oxide interface: 5 μm (i.e. thickness of n-type region)
- Oxide layer thickness: 0.5 μm.

3.1 Front-surface corrugation

In the next subsections, I will describe how to fabricate both the rear- and the front-surfaces of the device. However, both sides require ion implantation for the n^+ and p^+ regions. Since the equipment for ion implantation is not available at MIT, I will describe the preliminary work that needs to be done, after which the wafer can be sent to an implantation shop. In particular, the corrugated texture of the front surface must be generated.

We begin by obtaining the mask shown in Fig. 4.

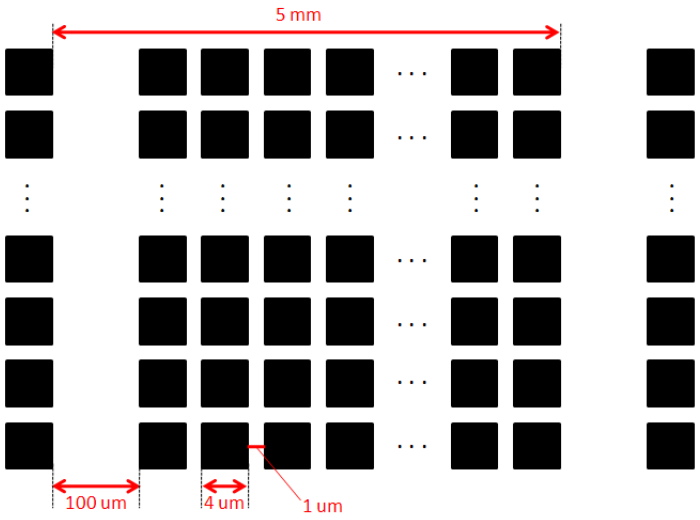

Figure 4: Mask for the definition of "inverted pyramids." The dimensions correspond to that of the specifications. Note that there will be a thousand pyramids (across) between the two fingers. The dark parts of the above mask are transparent.

In defining the pyramids, we will use the anisotropic KOH etch, exactly as in the MEMS lab. In fact, I borrow the MEMS lab procedure almost wholesale!

1. Grow 1.0 μm of silicon nitride (SiN_x) by LPCVD. We will use silicon nitride as a mask in the KOH etch, since it is completely resistant to KOH. The reaction is $3SiH_2Cl_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2$.
2. Pattern the SiN_x:
   (a) Treatment with HDMS for improving photoresist adhesion.
   (b) Apply "SPR700 1.2" positive-photoresist, spin for a few micron thickness.
   (c) Prebake at 95° for a few minutes.
   (d) Exposure to mask in Fig. 4.
   (e) Development by developer "LDD 26 W."
   (f) Post-bake at 130° for a few minuts.
   (g) Dry-etch silicon nitride. Dry etch is preferred to avoid undercut. The reaction is: Si_3N_4(s) + SF_6 + plasma $\rightarrow$ SiF_4(g) + SF_2 (g) + N_2 (g).
   (h) Remove photoresist.
3. KOH etch of underlying silicon. With 80°, 20% KOH solution, the etch rate is 86 μm/h[2]. Given 4 μm $\times$ 4 μm pockets and the angle of KOH etch, the depth of the full pyramid is 2.85 μm. The minimum etch time is then 2 minutes.
4. Etch the remaining silicon nitride (i.e. remove the mask). This can be done by a dry-etch as before, or a wet-etch. For instance, a wet-etch of silicon-nitride with boiling phosphoric acid will leave the underlying silicon intact[3].

Following these steps, we have a p-type wafer with a corrugated front surface.

3.2 Introduction of n^+, n, and p^+ type regions

We have decided to introduce the front-side n-type region by chemical vapor deposition, since the n-region thickness requirement of 5 microns is difficult to meet by ion implantation. (Note: Taking into account the extra oxide thickness, we would actually aim for 5.5 microns.) We use simultaneous CVD of silicon (Silane pyrolysis: SiH_4(g) $\rightarrow$ Si(s) + $2H_2$(g) at $\sim$ 620°C) and phosphine ($2PH_3$(g) $\rightarrow$ 2P(s) + $3H_2$(g)). The deposition rate is of silicon is $10 - 100$nm/min, hence approximately 100 minutes of CVD will generate the desired thickness. With a target P-doping level of 10^{17} cm^{-3}, the ratio of phosphorous to silicon deposition needs to be $1{:}10^5$.

NOTE: I was just informed (one hour before deadline!) by Orit that the 5 micron requirement may have been a typo. Given that the pyramid dimensions are only a

few microns, I expected this n-type region thickness to be less than a micron. If the specification was, in fact, less than a micron, then I would do the n-type doping also by ion implantation. This would be a cleaner solution than involving both CVD *and* ion implantation.

In order to define n^+ and p^+ regions, we use ion implantation. The advantage of ion implantation is that the beam can be rastered over the surface, which in this case means that a mask is unnecessary, since we do not need extremely fine control over the doping locations.

For the p^+ pockets in the rear, we use 200 keV ion-implantation of boron. This corresponds to a depth of approximately 0.6 microns. Note that we are compensating for the 0.5 microns that will be lost in a subsequent oxidation process. The geometrical requirements for the p^+ pockets were not given in the specifications. I would use the same periodicity as the front, "finger" electrodes; i.e. the p^+ pockets have 5 mm spacing. For a peak concentration of $C_B = 10^{19}$ cm^{-3}, we use a dose of $Q_B = 2.3 \times 10^{14}$ cm^{-2}.

As for the n^+ regions: At 200 keV, phosphorous penetrates 0.25 μn into silicon. With a target concentration of $C_P = 10^{19}$ cm^{-3}, we use a dose of $Q_P = 1.5 \times 10^{14}$ cm^{-2}. This beam is rastered over the "finger" regions only.

3.3 Oxide growth

Both the front and rear surfaces of the wafer require a 0.5 μm-thick oxide layer. This can be achieved by atmospheric pressure dry oxidation at 1200° degrees for six hours[4]. This oxidation process will coat the front and rear surfaces simultaneously.

3.4 Rear surface fabrication

The oxide must be patterned, in order to allow rear-electrode access to the p^+ regions. We pattern a photoresist mask (several microns) that only partially expose the p^+ pockets, as seen in Fig. 5. The oxide can be removed by HF/DI etch, which has an enormously rapid etch rate of 10 μm/min. Hence, a 3-second etch in HF/DI should be sufficient.

The rear contact can be created by physical vapor deposition of aluminum in the Endura 5500 Metal Sputtering System, as was done in the MOScap lab. We deposit 2.5 microns of Al. (I believe that for most sputtering systems, there is a crystal that monitors the amount of deposition... At least the one in my group. So, it is sufficient to specifiy the final thickness, rather than the time.)

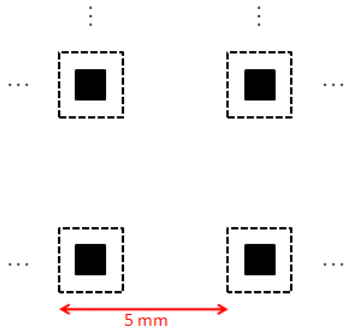

Figure 5: Mask for the rear surface. The dark parts of the above mask are transparent. The dotted structures indicate the p^+ regions below.

3.5 Front surface fabrication

We etch away strips of oxide parallel to the metallic fingers as seen in Fig. 6a. As before, a micron-thick mask should be sufficient with a three-second HF/DI etch.

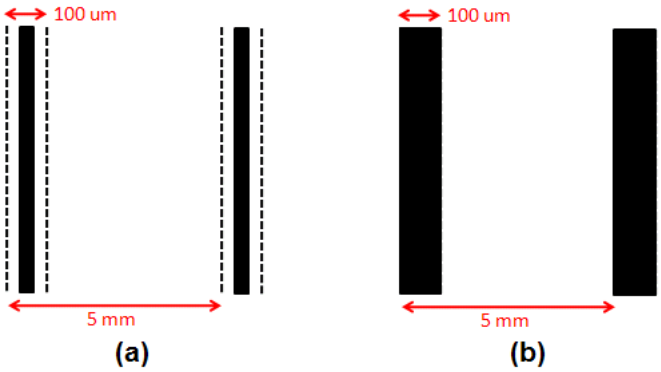

Figure 6: Two masks for the front surface. The dark parts of the above mask are transparent. (a) Mask for the oxide etch, defining a trench. The dotted lines indicate the dimensions of the electrode "fingers." (b) Mask for the patterning of the electrode fingers.

We then sputter the front surface with 2.5 microns of Al, as was done for the rear-surface. Step coverage is good for sputtered films, which is important since we are attempting to make an electrical connection into a trench.

Finally, we pattern the aluminum according to the mask in Fig. 6b. We can use the "rainbow" dry metal etcher system using $Cl_2/CHCl_3$. This dry etch is preferred since it is very anisotropic [Plummer 645].

I may also consider sintering the device (in 425°C, 75% of forming gas) at this point.

4 Design Evaluation

C: What are the potential drawbacks of the solar cell shown here, assuming the objectives are high-efficiency, large area, low-cost and ease of manufacturing?

There are numerous ways in which the current design can be further improved. The front electrodes (the "fingers") introduce electrode shadowing, which lowers the effective light-collection area of the device.

Also, the thickness of the wafer has not been optimized for maximum collection efficiency. We want to strike an optimal thickness, in order minimize recombination in the bulk, but at the same time maximizing the absorption of light.

We also know that silicon is not the optimal material for a solar-cell in terms of its bandgap energy. Materials such as GaAs have a better-tuned bandgap energy. However, this is a tradeoff for the sake of ease of manufacturing, since Si processing techniques are extremely-well developed w.r.t. other technologies.

In our processing technique, we have consistently relied on traditional lithography for pattern transfer, when other techniques such as screen-printing may be a more-economical alternative.

D: What other techniques or design approaches are available to mitigate or eliminate the drawbacks you identified in part C above?

Electrode shadowing due to the front contact can be greatly reduced by a design called the "buried contact cell." In this design (shown in Fig. 7), the electrodes are buried inside the bulk, which allows them to be thinner - and thereby take up less light-collection area - while maintaining good electrical contact to the cell. This design can reduce metal electrode shadowing from $10 - 15\%$ to $2 - 3\%$, providing an increase in efficiency by 25% without notably increasing the fabrication cost[1].

The effective area can also be increased by concentrators that focus solar energy onto a small photocell. They can be of the mirror type or even a simple lens.

Optimization of the wafer thickness can be performed experimentally. The wafers of different thicknesses can be prepared, for instance, by the string ribbon growth technique.

Lastly, we could simply change the bulk wafer to GaAs, and utilize screen-printing in the processing.

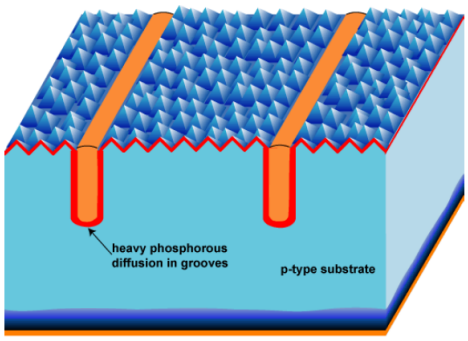

Figure 7: In the "buried contact cell" design, the front electrodes are buried inside the bulk. This allows the contacts to be thinner (and therefore take up less light-collection area) while maintaining the good electrical contact to the cell. Image adapted from [1].

5 Miscellaneous Issues

E: Below is the absorption of silicon as a function of wavelength. Also shown is the solar spectrum vs. wavelength. From these two pieces of information, it is apparent that a significant portion of the solar spectrum is not absorbed by silicon solar cells. Describe a way that more of the sun's radiation can be harnessed in a solar cell-type device.

Again, there are other materials available whose absorption coefficient is much more favorable than that of silicon. In particular $In_{0.7}Ga_{0.3}As_{0.64}P_{0.36}$ and $In_{0.53}Ga_{0.47}As$ have appreciable absorption at the long infrared tail of the solar radiation spectrum[1]. As usual, opting for such materials would be a tradeoff between performance and cost.

The Cadillac of current solar-cell designs is a "tandem-cell", which is a series of stacked solar cells, whose bandgap energies are ordered in such a way as to minimize heat loss. Each material, of course, also has a specific region of the solar spectrum which it prefers to absorb. Although tandem-cells boast the highest solar-cell efficiencies to date, they are expensive and also sensitive to the lighting conditions.

F: Suggest another way to modify the surface of the solar cell to achieve the same effect as obtained with the corrugated surface.

The purpose of the corrugated surface is to reduce reflection losses. The same goal can be achieved by anti-reflection coatings (the simplest of which we have used in our design; can construct stacked AR coatings). Fancier optics can also be used. For instance, light can be trapped in the bulk by using Bragg reflectors whose first-order reflection angle is extremely shallow with respect to the wafer body. In other words, light is "trapped" in the bulk. This technique has enhanced efficiency by 50% in very thin (2 μm) wafers[1].

Other optical tricks might include building a Fabry-Perot resonator by an introducing appropriate layers at the front- and end-surfaces of the solar cell. The Fabry-Perot can

be tuned for the wavelength which matches the bandgap energy of the material. However, I am unsure whether the enhanced coupling at this specific frequency outweighs the rejection of other frequencies that are unmatched to the cavity.

G: What are the benefits and disadvantages of using "string ribbon" crystal pulling technology to make silicon solar cells?

String ribbon crystal growth technique allows the manufacture of thin silicon wafers without having to dice from an ingot. Since material cost constitutes $\sim 50\%$ of Si-wafer based cells (and greater thickness doesn't always equal better performance), thinner wafers greatly reduce cost of manufacturing.

The string pulling technique also allows the thickness of the Si-film to be adjusted by varying the speed of the pull. This allows for experimental testing of the optimal bulk thickness, since it is easy to prepare wafers with various thicknesses.

One disadvantage of string-ribbon technique is that it produces wafers that are generally very thin. Since the absorption of light depends exponentially on the thickness, such thin wafers may not collect light very efficiently. This drawback can be mitigated by light-trapping techniques discussed in the previous section.

References

[1] Liu, Jifeng. *6.152J Lecture: Solar (Photovoltaic) Cells*. May 6th, 2009.

[2] H. Seidel, L. Csepregi, A. Hueberger, and H. Baungaertel, *The Journal of the Electrochemical Society*, 137, 3612-3626 (1990).

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