Depletion and Enhancement Mode β-Ga_2O_3 MOSFETs with ALD SiO_2 gate and near 400 V Breakdown Voltage

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Motivation

Ga_2O_3 has

- Higher Baliga's Figure of Merit (BFoM) than SiC and GaN [1].
- A mature growth technology for large area substrates [1] (Figure 1).
- Immune to various chemical etching (Figure 2).

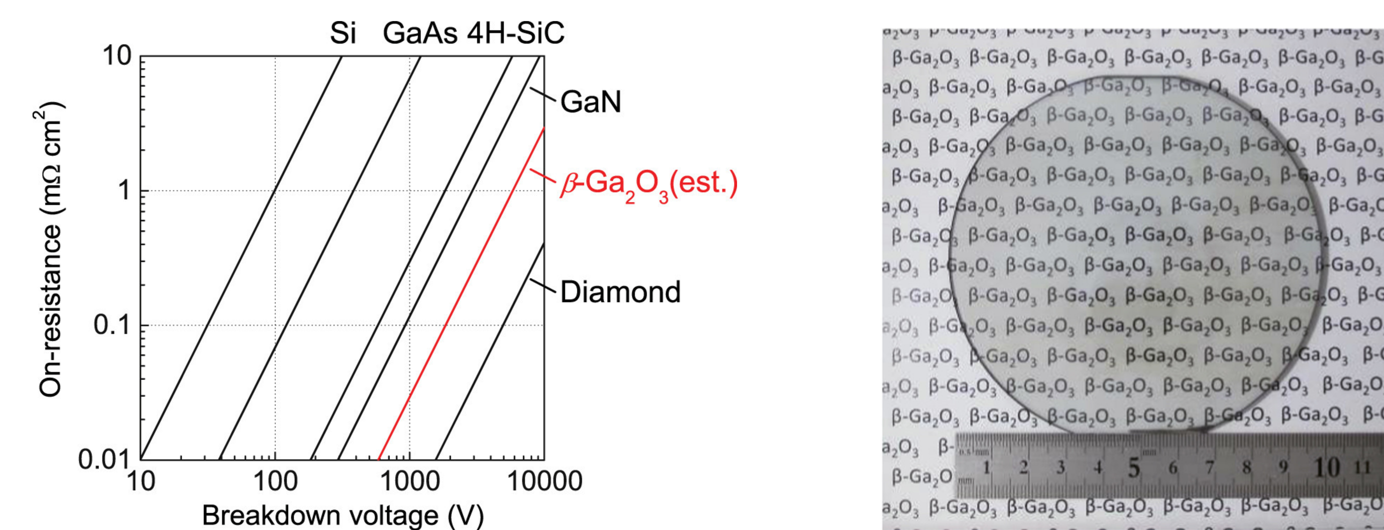

Fig. 1. Theoretical performance dependence of R_{on} on breakdown voltage (left) and photography of a 4-inch Ga_2O_3 wafer. [1]

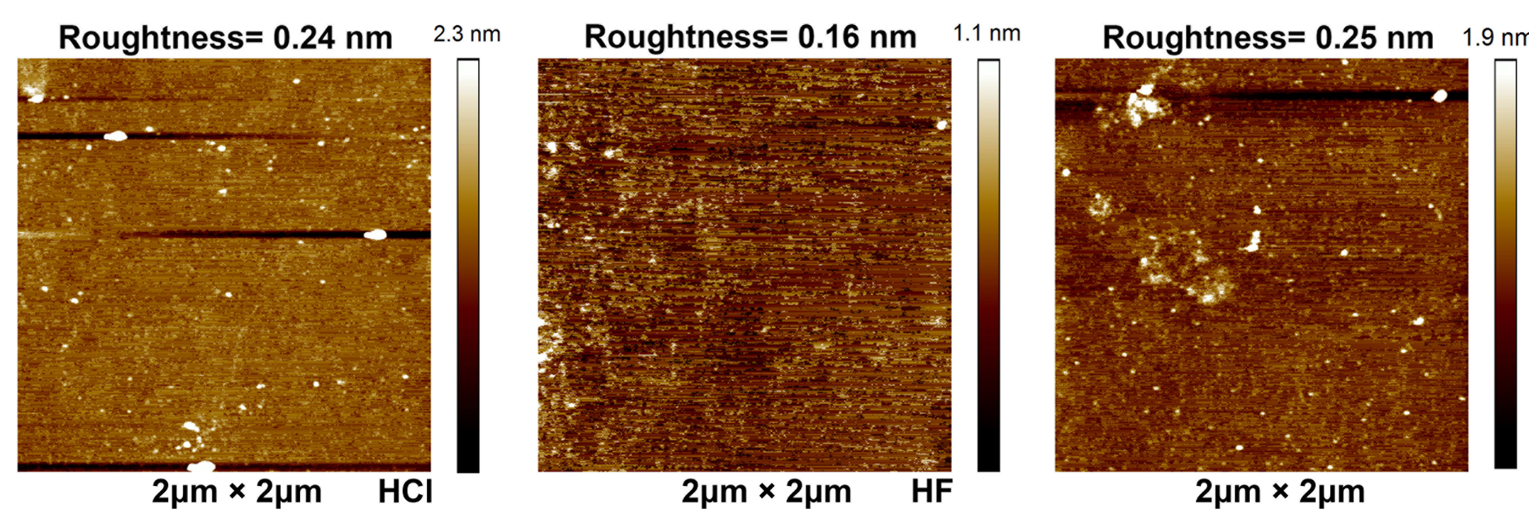

Fig. 2. AFM image of HCl, HF treated and no treatment Ga_2O_3 sample surface.

SiO_2/Ga_2O_3 interface has (Figure 3)

- Much bigger conduction band offset than that of Al_2O_3/Ga_2O_3 [2].
- Relatively low interface states density (~6 × 10^{11} $cm^{-2}eV^{-1}$) [3].

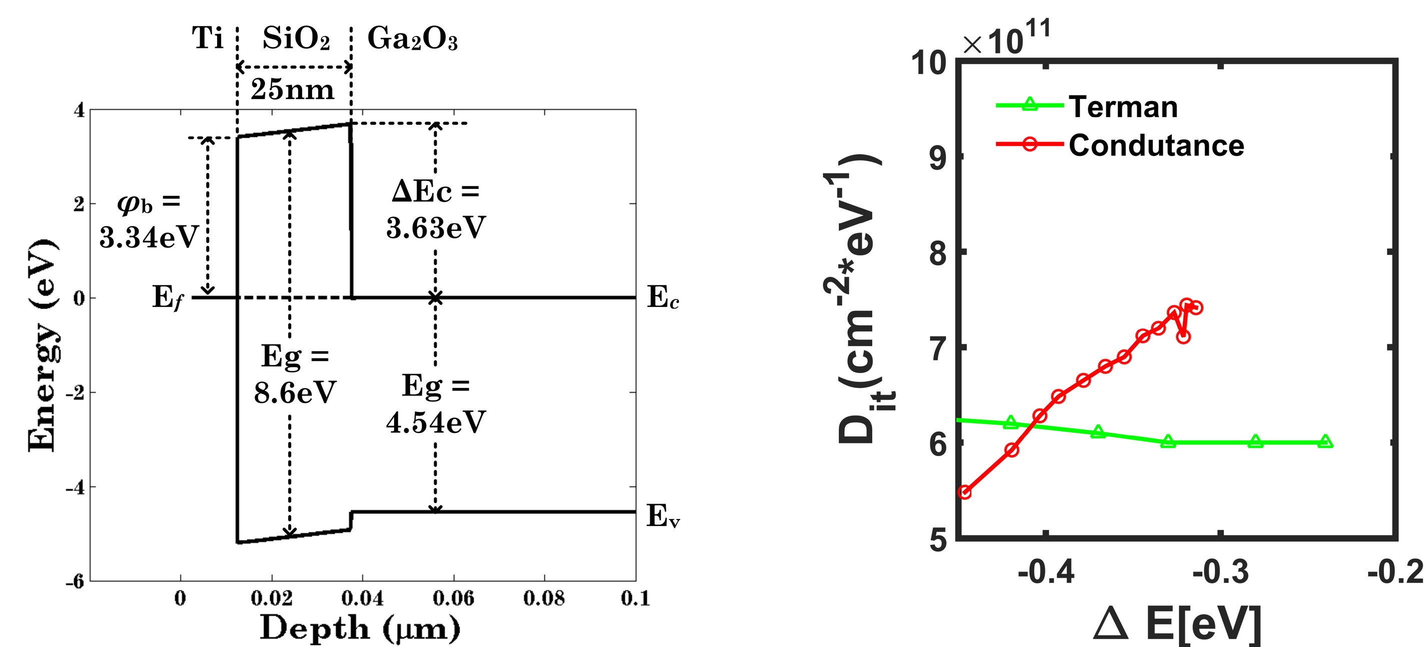

Fig. 3. Conduction band offset (left) and interface state density (right) at SiO_2/Ga_2O_3 interface.

Fabrication Process Flow

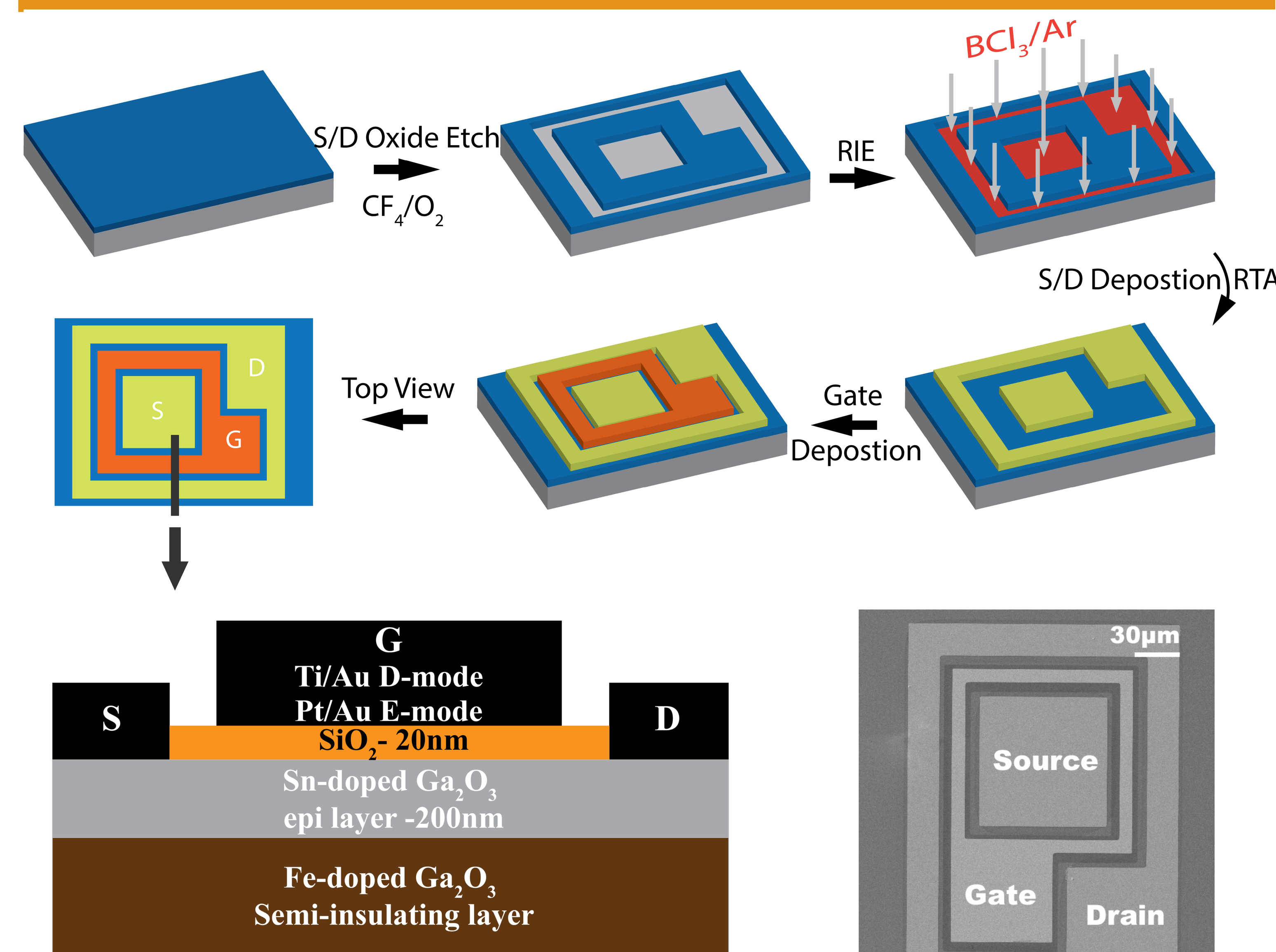

Fig. 4. Cross-section schematic of depletion and enhancement mode Ga2O3 MOSFET .

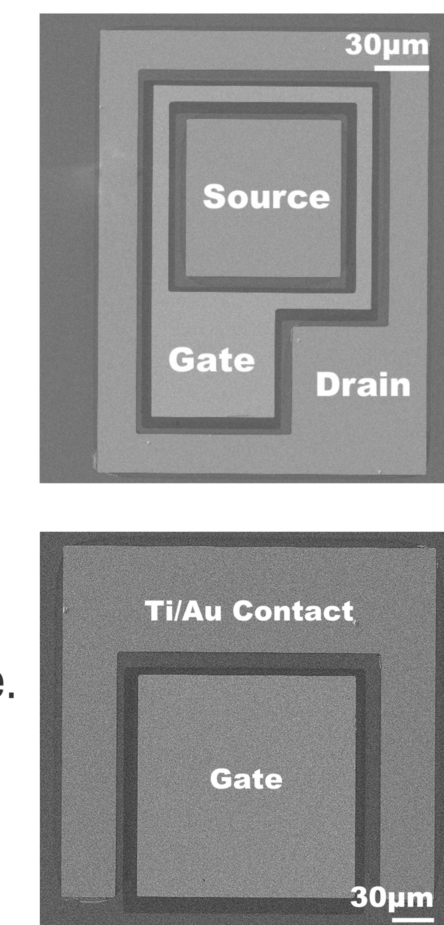

Fig. 5. SEM image of fabricated MOSFET (top) and MOSCAP (bottom).

Device Structure:

- 200 nm Ga_2O_3 epitaxial layer on SI substrate.
- EPI layer grown by ozone MBE.
- Targeted Doping = 5 × $10^{17}/cm^3$
- 20nm SiO_2 by ALD.

Ohmic Contact:

- 20nm-Ti/ 70nm- Au.
- BCl_3/Ar RIE treatment- 1 min.
- RTA: 470℃ 1min + 900℃ 1min

MOSCAP IV and CV Measurement

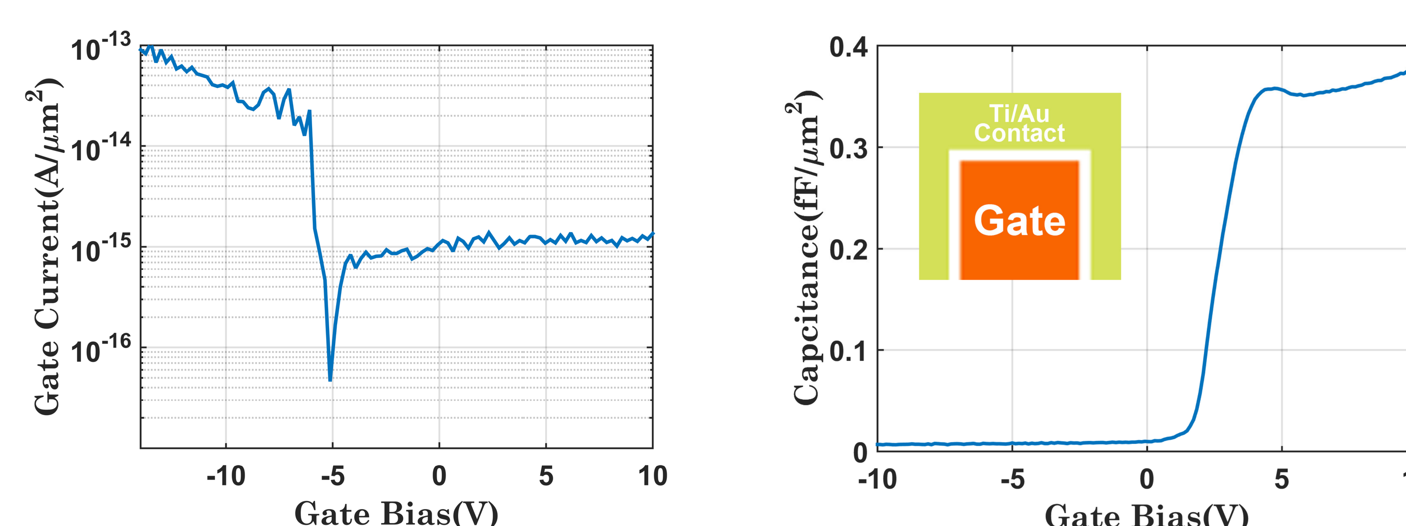

Fig. 6. Gate Leakage current and Capacitance-Voltage characteristic of MOS structure.

- Low leakage current and fast depletion indicates lower than expected N_d(doping density) ~ 6.34 × $10^{15}/cm^3$.

Depletion Mode MOSFET

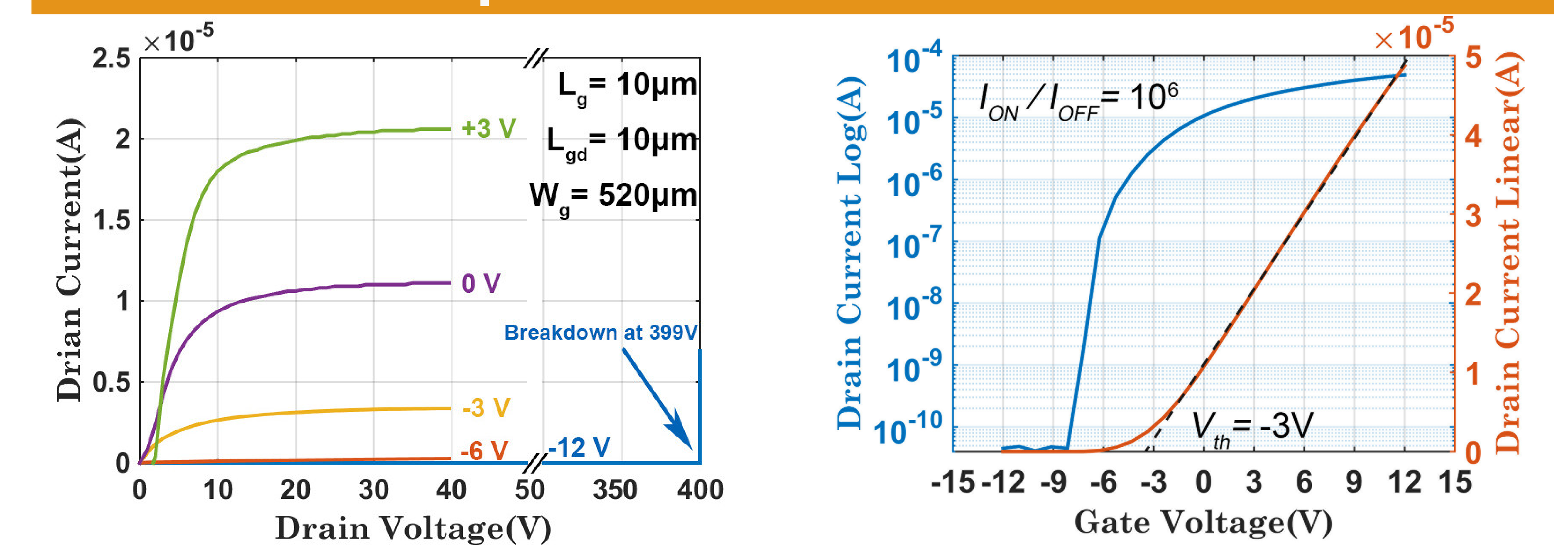

Fig. 7. Depletion mode MOSFET IV characteristic and transfer characteristic.

- Ti/Au gate metal stack.
- $V_{TH, Depletion}$ = -3V.
- I_{ON} = 48.7 μA @ V_{gs} = 12V and V_{ds} = 30V

Enhancement Mode MOSFET

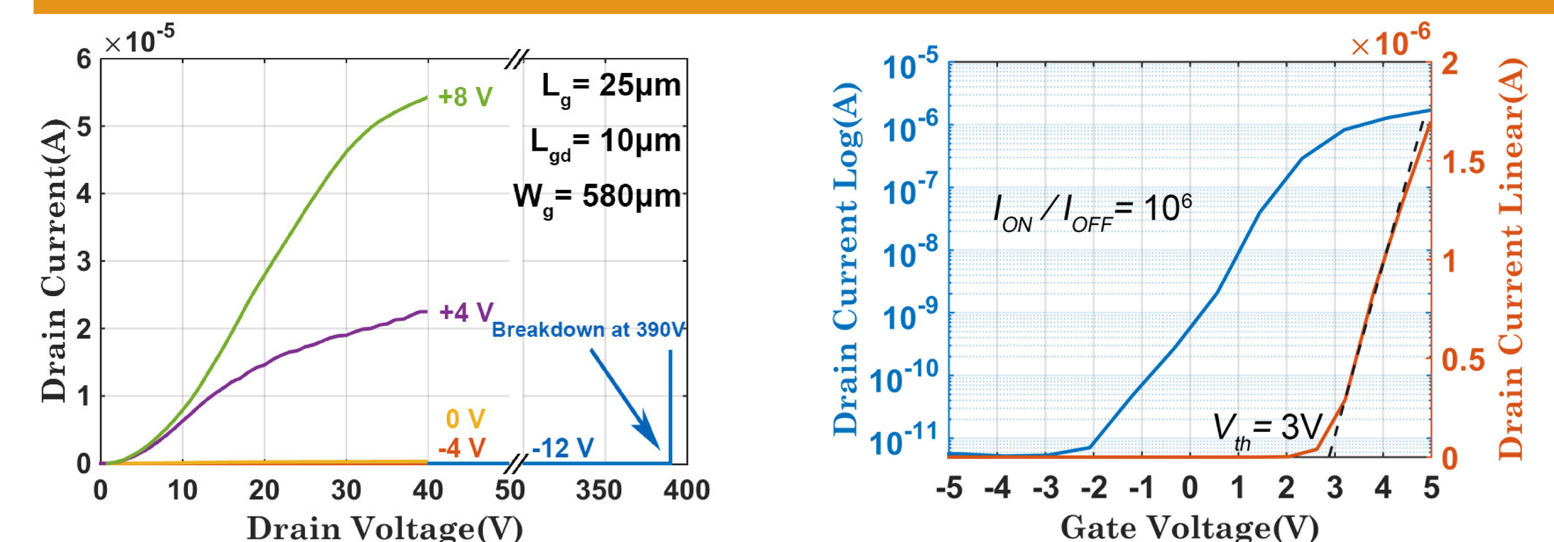

Fig. 8. Enhancement mode MOSFET IV characteristic and transfer characteristic.

- Pt/Au gate metal stack.
- $V_{TH, Enhancement}$ = 3V.
- I_{ON} = 45 μA @ V_{gs} = 8 V and V_{ds} = 30V

Conclusion and Future Work

- ✓ First demonstration of Enhancement-mode device with large ON/OFF ratio and breakdown voltage V_{br}= 400V.
- ✓ Low I_{ON} due to large parasite $R_{S/D}$ (source/drain contact resistance) and lower than expected N_d (doping density).
- ✓ E_{br} (breakdown field) = 0.4 MV/cm, far from the theoretical limit of ionization breakdown.
- ✓ Possible cause of degradation: hot electron effects in SiO_2.
- ➢ Contact doping to reduce parasitic source/drain resistance.
- ➢ Advanced gate stack structures for better channel control.
- ➢ Field plate for electric field engineering.
- ➢ Breakdown mechanism study.

References

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[2] Y. Jia et al, *Appl. Phys. Lett.*, vol. 106, no. 10, p. 102107, (2015).
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